



### GENERAL DESCRIPTION

The AK4586 is a single chip CODEC that includes two channels of ADC and six channels of DAC. The ADC outputs 24bit data and the DAC accepts up to 24bit input data. The ADC has the Enhanced Dual Bit architecture with wide dynamic range. The DAC introduces the new developed Advanced Multi-Bit architecture, and achieves wider dynamic range and lower outband noise.

The AK4586 also has a digital audio receiver (DIR) compatible with 96kHz, 24bits. The AK4586 can automatically detect a Non-PCM bit stream. The digital audio output can be selected from the ADC output or the digital input. Control may be set directly by programmed through a separate serial interface.

The AK4586 has a dynamic range of 100dB for ADC, 106dB for DAC and is well suited for digital surround for home theater and car audio. The AK4586 also has the balance volume control corresponding to the AC-3 system. The AK4586 is available in a small 44pin LQFP package which will reduce system space.

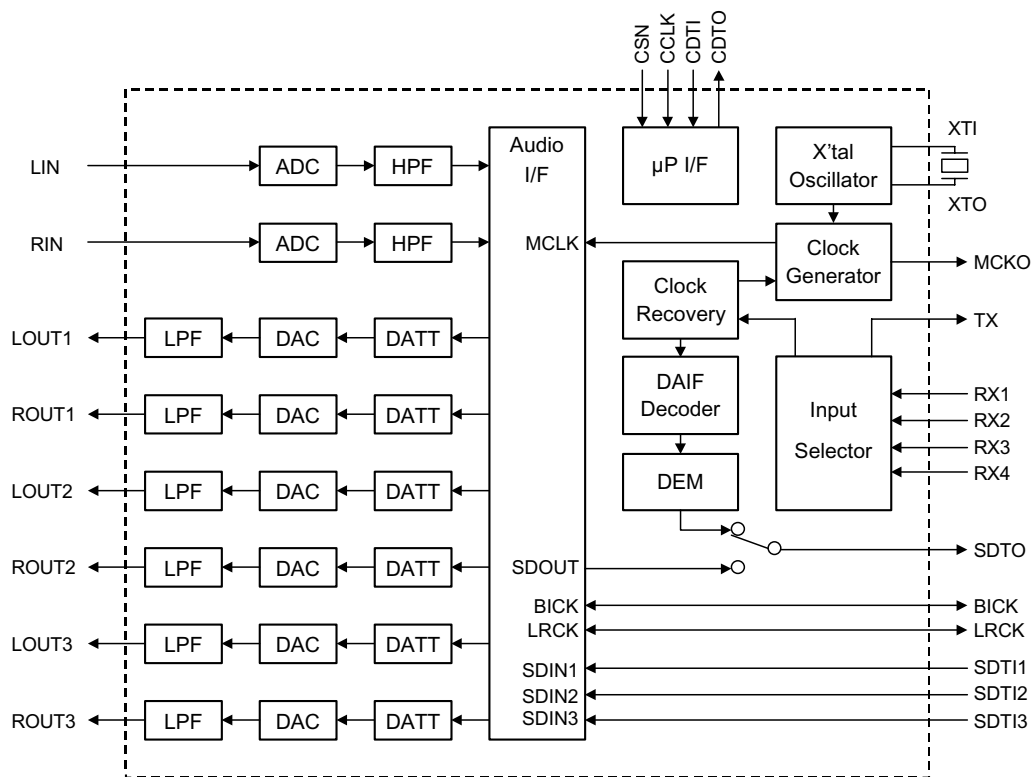
\*AC-3 is a trademark of Dolby Laboratories.

### FEATURES

- 2ch 24bit ADC
  - 64x Oversampling
  - Sampling Rate up to 96kHz
  - Linear Phase Digital Anti-Alias Filter
  - Single-Ended Input
  - S/(N+D): 90dB
  - Dynamic Range, S/N: 100dB
  - Digital HPF for offset cancellation
  - Overflow flag
- 6ch 24bit DAC
  - 128x Oversampling
  - Sampling Rate up to 96kHz
  - 24bit 8 times Digital Filter
  - Single-Ended Outputs
  - On-chip Switched-Capacitor Filter
  - S/(N+D): 90dB
  - Dynamic Range, S/N: 106dB
  - Individual channel digital volume with 256 levels and 0.5dB step
  - Soft mute
  - Zero Detect Function
- 4 inputs 24bit DIR
  - Supports IEC60958 consumer mode, S/PDIF, EIAJ CP1201 consumer mode
  - Low jitter Analog PLL
  - PLL Lock Range: 32k ~ 96kHz
  - Clock Source: PLL or X'tal
  - 4 channel Receivers input and 1 through transmission output
  - De-emphasis for 32kHz, 44.1kHz and 48kHz
  - Dedicated Detect Pins
    - Non-PCM Bit Stream Detect, DTS-CD Bit Stream Detect, Validity Flag Detect, 96kHz Sampling Detect, Unlock & Parity Error Detect, Emphasis Detect, fs change Detect
  - Supports up to 24bit Audio Data Format
  - Audio I/F: Master or Slave Mode
  - 32bits Channel Status Buffer

- Burst Preamble bit Pc, Pd Buffer for Non-PCM bit stream
- Master Clock Outputs:128fs/256fs/512fs
- I/F format: MSB justified, LSB justified(20bit,24bit), I<sup>2</sup>S or TDM
- High Jitter Tolerance
- TTL Level Digital I/F
- 4-wire Serial and I<sup>2</sup>C Bus  $\mu$ P I/F for mode setting
- External Master Clock Input:
  - 256fs, 384fs or 512fs for fs=44.1kHz to 48kHz
  - 128fs, 192fs or 256fs for fs=88.2kHz to 96kHz
- Power Supply: 4.5 to 5.5V
- Power Supply for output buffer: 2.7 to 5.5V
- Small 44pin LQFP

■ Block Diagram



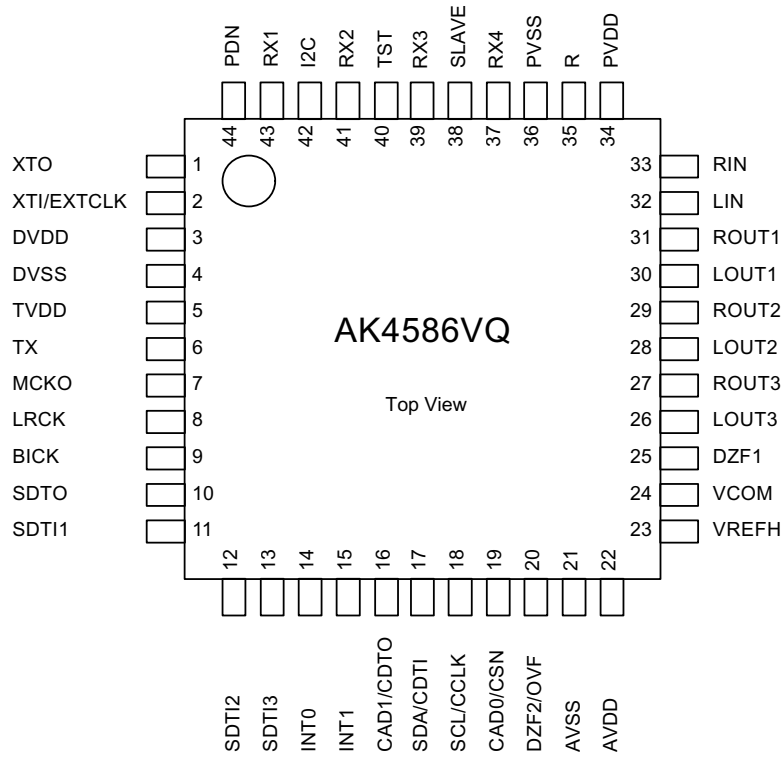
■ Ordering Guide

AK4586VQ  
AKD4586

-40 ~ +85°C  
Evaluation Board for AK4586

44pin LQFP(0.8mm pitch)

■ Pin Layout



### ■ Compatibility with AK4527B/29

| Functions                            | AK4527B/29      | AK4586        |
|--------------------------------------|-----------------|---------------|
| ADC S/(N+D)                          | 92dB            | 90dB          |
| ADC Dynamic Range, S/N               | 102dB           | 100dB         |
| DAC channel                          | 6ch/8ch         | 6ch           |
| Master mode                          | Not available   | Available     |
| Parallel mode                        | Available       | Not available |
| Read operation for internal register | Not available   | Available     |
| Chip address at 4-wire serial mode   | 2bit selectable | fixed to "00" |

### ■ Compatibility with AK4112A

| Functions                   | AK4112A       | AK4586   |
|-----------------------------|---------------|--|
| Power supply                | 2.7 ~ 3.6V    | 4.5 ~ 5.5V   |
| Rock range                  | 22k ~ 108kHz  | 32k ~ 96kHz  |
| Master clock output         | 2 pins        | 1 pin  |
| External master clock input | 256fs/512fs   | 256fs/384fs/512fs for Normal speed<br>128fs/192fs/256fs for Double speed |
| Detect pins                 | 4 pins        | 2 pins   |
| DTS-CDdetect                | Not available | Available  |
| CRC                         | Available     | Not available  |
| Parallel mode               | Available     | Not available  |
| I <sup>2</sup> C bus mode   | Not available | Available  |
| Digital input level         | CMOS          | TTL  |

| PIN/FUNCTION |          |     |   |
|--------------|----------|-----|---|
| No.          | Pin Name | I/O | Function  |
| 1            | XTO      | O   | X'tal Output Pin  |
| 2            | XTI      | I   | X'tal Input Pin   |
|              | EXTCLK   | I   | External Master Clock Input Pin   |
| 3            | DVDD     | -   | Digital Power Supply Pin, 4.5V~5.5V   |
| 4            | DVSS     | -   | Digital Ground Pin, 0V  |
| 5            | TVDD     | -   | Output Buffer Power Supply Pin, 2.7V~5.5V   |
| 6            | TX       | O   | Transmit channel (through data) Output Pin  |
| 7            | MCKO     | O   | Master Clock Output Pin   |
| 8            | LRCK     | I/O | Input/Output Channel Clock Pin  |
| 9            | BICK     | I/O | Audio Serial Data Clock Pin   |
| 10           | SDTO     | O   | Audio Serial Data Output Pin  |
| 11           | SDTI1    | I   | DAC1 Audio Serial Data Input Pin  |
| 12           | SDTI2    | I   | DAC2 Audio Serial Data Input Pin  |
| 13           | SDTI3    | I   | DAC3 Audio Serial Data Input Pin  |
| 14           | INT0     | O   | Interrupt 0 pin   |
| 15           | INT1     | O   | Interrupt 1 pin   |
| 16           | CDTO     | O   | Control Data Output Pin in 4-wire serial control mode   |
|              | CAD1     | I   | Chip Address 1 Pin in I <sup>2</sup> C bus control mode   |
| 17           | CDTI     | I   | Control Data Input Pin in 4-wire serial control mode  |
|              | SDA      | I/O | Control Data Input/Output Pin in I <sup>2</sup> C bus control mode  |
| 18           | CCLK     | I   | Control Data Clock Pin in 4-wire serial control mode  |
|              | SCL      | I   | Control Data Clock Pin in I <sup>2</sup> C bus control mode   |
| 19           | CSN      | I   | Chip Select Pin in 4-wire serial control mode   |
|              | CAD0     | I   | Chip Address 0 Pin in I <sup>2</sup> C bus control mode   |
| 20           | DZF2     | O   | Zero Input Detect 2 Pin (Note 1)<br>When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". |
|              | OVF      | O   | Analog Input Overflow Detect Pin (Note 2)<br>This pin goes to "H" if the analog input of Lch or Rch is overflows.                               |
| 21           | AVSS     | -   | Analog Ground Pin, 0V   |
| 22           | AVDD     | -   | Analog Power Supply Pin, 4.5V~5.5V  |

| No. | Pin Name | I/O | Function  |
|-----|----------|-----|---|
| 23  | VREFH    | I   | Positive Voltage Reference Input Pin, AVDD  |
| 24  | VCOM     | O   | Common Voltage Output Pin, AVDD/2<br>Large external capacitor around 2.2 $\mu$ F is used to reduce power-supply noise.  |
| 25  | DZF1     | O   | Zero Input Detect 1 Pin (Note 1)<br>When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H".   |
| 26  | LOUT3    | O   | DAC3 Lch Analog Output Pin  |
| 27  | ROUT3    | O   | DAC3 Rch Analog Output Pin  |
| 28  | LOUT2    | O   | DAC2 Lch Analog Output Pin  |
| 29  | ROUT2    | O   | DAC2 Rch Analog Output Pin  |
| 30  | LOUT1    | O   | DAC1 Lch Analog Output Pin  |
| 31  | ROUT1    | O   | DAC1 Rch Analog Output Pin  |
| 32  | LIN      | I   | Lch Analog Input Pin  |
| 33  | RIN      | I   | Rch Analog Input Pin  |
| 34  | PVDD     | -   | PLL Power Supply Pin, 4.5V~5.5V   |
| 35  | R        | -   | External Resistor Pin<br>18k $\Omega$ +/-1% resistor to PVSS externally.  |
| 36  | PVSS     | -   | PLL Ground Pin, 0V  |
| 37  | RX4      | I   | Receiver Channel 4 Pin (Internal biased pin)  |
| 38  | SLAVE    | I   | Slave Mode Pin<br>"L": Master mode or Slave mode, "H": Slave mode   |
| 39  | RX3      | I   | Receiver Channel 3 Pin (Internal biased pin)  |
| 40  | TST      | I   | Test Pin<br>This pin should be connected to DVSS.   |
| 41  | RX2      | I   | Receiver Channel 2 Pin (Internal biased pin)  |
| 42  | I2C      | I   | Control Mode Select Pin<br>"L": 4-wire Serial, "H": I <sup>2</sup> C Bus  |
| 43  | RX1      | I   | Receiver Channel 1 Pin (Internal biased pin)  |
| 44  | PDN      | I   | Power-Down & Reset Pin<br>When "L", the AK4586 is powered-down, all output pins go to "L" and the control registers are reset to default state. If the state of CAD1-0 changes, then the AK4586 must be reset by PDN. |

## Notes:

1. The group 1 and 2 can be selected by DZFM2-0 bits.
2. This pin becomes OVF pin if OVFE bit is set to "1".
3. All input pins except internal biased pins should not be left floating.

**ABSOLUTE MAXIMUM RATINGS**

(AVSS, DVSS, PVSS=0V; Note 4)

| Parameter  |                     | Symbol         | min  | max      | Units |
|--|---------------------|----------------|------|----------|-------|
| Power Supplies   | Analog              | AVDD           | -0.3 | 6.0      | V     |
|  | Digital             | DVDD           | -0.3 | 6.0      | V     |
|  | PLL                 | PVDD           | -0.3 | 6.0      | V     |
|  | Output buffer       | TVDD           | -0.3 | 6.0      | V     |
|  | AVSS-DVSS  (Note 5) | $\Delta$ GNDD1 | -    | 0.3      | V     |
|  | AVSS-PVSS  (Note 5) | $\Delta$ GNDD2 | -    | 0.3      | V     |
| Input Current (any pins except for supplies)   |                     | IIN            | -    | $\pm$ 10 | mA    |
| Analog Input Voltage   |                     | VINA           | -0.3 | AVDD+0.3 | V     |
| Digital Input Voltage<br>(XTI/EXTCLK, SDTI1-3, CDTI/SDA,<br>CCLK/SCL, CSN/CAD0 pins) |                     | VIND1          | -0.3 | DVDD+0.3 | V     |
| (LRCK, BICK, CDTO/CAD1 pins)   |                     | VIND2          | -0.3 | TVDD+0.3 | V     |
| (RX1-4, SLAVE, TST, I2C, PDN pins)   |                     | VIND3          | -0.3 | PVDD+0.3 | V     |
| Ambient Temperature (power applied)  |                     | Ta             | -40  | 85       | °C    |
| Storage Temperature  |                     | Tstg           | -65  | 150      | °C    |

Notes:

- All voltages with respect to ground.
- AVSS, DVSS and PVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS**

(AVSS, DVSS, PVSS=0V; Note 4)

| Parameter                  |               | Symbol | min | typ | max | Units |
|----------------------------|---------------|--------|-----|-----|-----|-------|
| Power Supplies<br>(Note 6) | Analog        | AVDD   | 4.5 | 5.0 | 5.5 | V     |
|                            | Digital       | DVDD   | 4.5 | 5.0 | 5.5 | V     |
|                            | PLL           | PVDD   | 4.5 | 5.0 | 5.5 | V     |
|                            | Output buffer | TVDD   | 2.7 | 5.0 | 5.5 | V     |

Notes:

- All voltages with respect to ground.
- The power up sequence between AVDD, DVDD, PVDD and TVDD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

|                               |
|-------------------------------|
| <b>ANALOG CHARACTERISTICS</b> |
|-------------------------------|

(Ta=25°C; AVDD, DVDD, PVDD, TVDD=5V; AVSS, DVSS=0V; VREFH=AVDD; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at fs=48kHz, 20Hz~40kHz at fs=96kHz; unless otherwise specified)

| Parameter                                | min                     | typ  | max  | Units  |     |
|--|-------------------------|------|------|--------|-----|
| <b>ADC Analog Input Characteristics</b>  |                         |      |      |        |     |
| Resolution                               |                         |      | 24   | Bits   |     |
| S/(N+D) (-0.5dBFS)                       | fs=48kHz                | 82   | 90   | dB     |     |
|  | fs=96kHz                | 78   | 86   | dB     |     |
| DR (-60dBFS)                             | fs=48kHz, A-weighted    | 92   | 100  | dB     |     |
|  | fs=96kHz, A-weighted    | 91   | 100  | dB     |     |
| S/N (Note 7)                             | fs=48kHz, A-weighted    | 92   | 100  | dB     |     |
|  | fs=96kHz, A-weighted    | 91   | 100  | dB     |     |
| Interchannel Isolation                   |                         | 90   | 110  | dB     |     |
| <b>DC Accuracy</b>                       |                         |      |      |        |     |
| Interchannel Gain Mismatch               |                         | 0.2  | 0.3  | dB     |     |
| Gain Drift                               |                         | 20   | -    | ppm/°C |     |
| Input Voltage                            | fs=48kHz AIN=0.62xVREFH | 2.90 | 3.10 | 3.30   | Vpp |
|  | fs=96kHz AIN=0.65xVREFH | 3.05 | 3.25 | 3.45   | Vpp |
| Input Resistance (Note 8)                |                         | 15   | 25   | kΩ     |     |
| Power Supply Rejection (Note 9)          |                         |      | 50   | dB     |     |
| <b>DAC Analog Output Characteristics</b> |                         |      |      |        |     |
| Resolution                               |                         |      | 24   | Bits   |     |
| S/(N+D)                                  | fs=48kHz                | 80   | 90   | dB     |     |
|  | fs=96kHz                | 78   | 86   | dB     |     |
| DR (-60dBFS)                             | fs=48kHz, A-weighted    | 95   | 106  | dB     |     |
|  | fs=96kHz, A-weighted    | 94   | 106  | dB     |     |
| S/N (Note 10)                            | fs=48kHz, A-weighted    | 95   | 106  | dB     |     |
|  | fs=96kHz, A-weighted    | 94   | 106  | dB     |     |
| Interchannel Isolation                   |                         | 90   | 110  | dB     |     |
| <b>DC Accuracy</b>                       |                         |      |      |        |     |
| Interchannel Gain Mismatch               |                         | 0.2  | 0.5  | dB     |     |
| Gain Drift                               |                         | 20   | -    | ppm/°C |     |
| Output Voltage AOUT=0.6xVREFH            |                         | 2.75 | 3.0  | 3.25   | Vpp |
| Load Resistance                          |                         | 5    |      | kΩ     |     |
| Power Supply Rejection (Note 9)          |                         |      | 50   | dB     |     |
| <b>Power Supplies</b>                    |                         |      |      |        |     |
| Power Supply Current                     |                         |      |      |        |     |
| Normal Operation (PDN = "H") (Note 11)   |                         |      |      |        |     |
| AVDD                                     |                         |      | 39   | 54     | mA  |
| PVDD                                     |                         |      | 9    | 14     | mA  |
| DVDD+TVDD fs=48kHz (Note 12)             |                         |      | 28   | 42     | mA  |
| fs=96kHz                                 |                         |      | 39   | 59     | mA  |
| Power-down mode (PDN = "L") (Note 13)    |                         |      | 80   | 200    | μA  |

## Notes:

7. S/N measured by CCIR-ARM is 96dB(@fs=48kHz).
8. Input resistance is 16kΩ typically at fs=96kHz.
9. PSR is applied to AVDD, DVDD, PVDD and TVDD with 1kHz, 50mVpp. VREFH pin is held a constant voltage.
10. S/N measured by CCIR-ARM is 102dB(@fs=48kHz).
11. CL=20pF, X'tal=24.576MHz, CM1-0= "10", OCKS= "10".
12. TVDD=3mA(typ).
13. In the power-down mode. RX inputs are open and all digital input pins including clock pins (MCLK, BICK, LRCK) are held DVSS.

| FILTER CHARACTERISTICS  |        |                   |     |      |       |      |      |
|---|--------|-------------------|-----|------|-------|------|------|
| (Ta=25°C; AVDD, DVDD, PVDD=4.5~5.5V; TVDD=2.7~5.5V; fs=48kHz) |        |                   |     |      |       |      |      |
| Parameter   | Symbol | min               | typ | max  | Units |      |      |
| <b>ADC Digital Filter (Decimation LPF):</b>                   |        |                   |     |      |       |      |      |
| Passband (Note 14)  |        | ±0.1dB            | PB  | 0    |       | 18.9 | kHz  |
|   |        | -0.2dB            |     | -    | 20.0  | -    | kHz  |
|   |        | -3.0dB            |     | -    | 23.0  | -    | kHz  |
| Stopband  | SB     | 29.4              |     |      |       |      | kHz  |
| Passband Ripple   | PR     |                   |     |      | ±0.1  |      | dB   |
| Stopband Attenuation  | SA     | 65                |     |      |       |      | dB   |
| Group Delay (Note 15)   | GD     |                   |     | 17.0 |       |      | 1/fs |
| Group Delay Distortion  | ΔGD    |                   |     | 0    |       |      | μs   |
| <b>ADC Digital Filter (HPF):</b>                              |        |                   |     |      |       |      |      |
| Frequency Response (Note 14)                                  |        | -3dB              | FR  |      | 1.0   |      | Hz   |
|   |        | -0.1dB            |     |      | 6.5   |      | Hz   |
| <b>DAC Digital Filter:</b>                                    |        |                   |     |      |       |      |      |
| Passband (Note 14)  |        | -0.1dB            | PB  | 0    |       | 21.8 | kHz  |
|   |        | -6.0dB            |     | -    | 24.0  | -    | kHz  |
| Stopband  | SB     | 26.2              |     |      |       |      | kHz  |
| Passband Ripple   | PR     |                   |     |      | ±0.02 |      | dB   |
| Stopband Attenuation  | SA     | 54                |     |      |       |      | dB   |
| Group Delay (Note 15)   | GD     |                   |     | 19.1 |       |      | 1/fs |
| <b>DAC Digital Filter + Analog Filter:</b>                    |        |                   |     |      |       |      |      |
| Frequency Response:   |        | 0 ~ 20.0kHz       | FR  |      | ±0.2  |      | dB   |
|   |        | 40.0kHz (Note 16) | FR  |      | ±0.3  |      | dB   |

## Notes:

14. The passband and stopband frequencies scale with fs.  
For example, 21.8kHz at -0.1dB is 0.454 x fs. The reference frequency of these responses is 1kHz.
15. The calculating delay time which occurred by digital filtering. This time is from setting the input of analog signal to setting the 24bit data of both channels to the output register for ADC.  
For DAC, this time is from setting the 20/24bit data of both channels on input register to the output of analog signal.
16. fs=96kHz.

| DC CHARACTERISTICS   |                                    |          |          |         |       |   |
|--|------------------------------------|----------|----------|---------|-------|---|
| (Ta=25°C; AVDD, DVDD, PVDD=4.5~5.5V; TVDD=2.7~5.5V)                        |                                    |          |          |         |       |   |
| Parameter  | Symbol                             | min      | typ      | max     | Units |   |
| High-Level Input Voltage (Except XTI pin)                                  | VIH                                | 2.2      | -        | -       | V     |   |
|  | (XTI pin)                          | VIH      | 70%DVDD  | -       | -     | V |
| Low-Level Input Voltage (Except XTI pin)                                   | VIL                                | -        | -        | 0.8     | V     |   |
|  | (XTI pin)                          | VIL      | -        | 30%DVDD | V     |   |
| Input Voltage at AC Coupling (Note 17)                                     | VAC                                | 40%DVDD  | -        | -       | Vpp   |   |
| High-Level Output Voltage<br>(Except TX, DZF1, DZF2/OVF pins: Iout=-400μA) | VOH                                | TVDD-0.5 | -        | -       | V     |   |
|  | (TX pin: Iout=-400μA)              | VOH      | DVDD-0.5 | -       | -     | V |
|  | (DZF1, DZF2/OVF pins: Iout=-400μA) | VOH      | AVDD-0.5 | -       | -     | V |
| Low-Level Output Voltage<br>(Except SDA pin: Iout= 400μA)                  | VOL                                | -        | -        | 0.5     | V     |   |
|  | (SDA pin: Iout= 3mA)               | VOL      | -        | 0.4     | V     |   |
| Input Leakage Current  | Iin                                | -        | -        | ±10     | μA    |   |

## Notes:

17. In case of connecting capacitance to XTI pin (refer to Figure 4).

|                                  |
|----------------------------------|
| <b>SWITCHING CHARACTERISTICS</b> |
|----------------------------------|

(Ta=25°C; AVDD, DVDD, PVDD=4.5~5.5V; TVDD=2.7~5.5V; CL=20pF)

| Parameter                        | Symbol | min     | typ   | max    | Units |
|----------------------------------|--------|---------|-------|--------|-------|
| <b>Master Clock Timing</b>       |        |         |       |        |       |
| <b>Crystal Resonator</b>         |        |         |       |        |       |
| Frequency                        | fXTAL  | 11.2896 |       | 24.576 | MHz   |
| <b>External Clock</b>            |        |         |       |        |       |
| 256fsn, 128fsd:                  | fCLK   | 11.2896 |       | 12.288 | MHz   |
| Pulse Width Low                  | tCLKL  | 27      |       |        | ns    |
| Pulse Width High                 | tCLKH  | 27      |       |        | ns    |
| 384fsn, 192fsd:                  | fCLK   | 16.9344 |       | 18.432 | MHz   |
| Pulse Width Low                  | tCLKL  | 20      |       |        | ns    |
| Pulse Width High                 | tCLKH  | 20      |       |        | ns    |
| 512fsn, 256fsd:                  | fCLK   | 22.5792 |       | 24.576 | MHz   |
| Pulse Width Low                  | tCLKL  | 15      |       |        | ns    |
| Pulse Width High                 | tCLKH  | 15      |       |        | ns    |
| <b>MCKO output</b>               |        |         |       |        |       |
| Frequency                        | fMCK   | 5.6448  |       | 24.576 | MHz   |
| Duty (Note 18)                   | dMCK   | 40      | 50    | 60     | %     |
| PLL Clock Recover Frequency      | fPLL   | 32      |       | 96     | kHz   |
| <b>LRCK Timing</b>               |        |         |       |        |       |
| <b>TDM= "0"</b>                  |        |         |       |        |       |
| LRCK frequency Normal Speed Mode | fsn    | 32      |       | 48     | kHz   |
| LRCK frequency Double Speed Mode | fsd    | 88.2    |       | 96     | kHz   |
| Duty Cycle                       | Duty   | 45      |       | 55     | %     |
| <b>TDM= "1" (Slave mode)</b>     |        |         |       |        |       |
| LRCK frequency                   | fsn    | 32      |       | 48     | kHz   |
| "H" time                         | tLRH   | 1/256fs |       |        | ns    |
| "L" time                         | tLRL   | 1/256fs |       |        | ns    |
| <b>TDM= "1" (Master mode)</b>    |        |         |       |        |       |
| LRCK frequency                   | fsn    | 32      |       | 48     | kHz   |
| "H" time (Note 19)               | tLRH   |         | 1/8fs |        | ns    |

## Notes:

18. Except the case CLKDIV= "0" for the external clock input. CL=15pF when MCKO is above 22.5792MHz.

19. "L" time at I<sup>2</sup>S format.

| Parameter                                   | Symbol | min | typ   | max | Units |
|---|--------|-----|-------|-----|-------|
| <b>Audio Interface Timing (Slave mode)</b>  |        |     |       |     |       |
| <b>TDM= "0"</b>                             |        |     |       |     |       |
| BICK Period                                 | tBCK   | 160 |       |     | ns    |
| BICK Pulse Width Low                        | tBCKL  | 65  |       |     | ns    |
| Pulse Width High                            | tBCKH  | 65  |       |     | ns    |
| LRCK Edge to BICK "↑" (Note 20)             | tLRB   | 45  |       |     | ns    |
| BICK "↑" to LRCK Edge (Note 20)             | tBLR   | 45  |       |     | ns    |
| LRCK to SDTO(MSB) (Note 21)                 | tLRS   |     |       | 40  | ns    |
| BICK "↓" to SDTO                            | tBSD   |     |       | 40  | ns    |
| SDTI1-3, DAUX Hold Time                     | tSDH   | 40  |       |     | ns    |
| SDTI1-3, DAUX Setup Time                    | tSDS   | 25  |       |     | ns    |
| <b>TDM= "1"</b>                             |        |     |       |     |       |
| BICK Period                                 | tBCK   | 81  |       |     | ns    |
| BICK Pulse Width Low                        | tBCKL  | 32  |       |     | ns    |
| Pulse Width High                            | tBCKH  | 32  |       |     | ns    |
| LRCK Edge to BICK "↑" (Note 20)             | tLRB   | 20  |       |     | ns    |
| BICK "↑" to LRCK Edge (Note 20)             | tBLR   | 20  |       |     | ns    |
| BICK "↓" to SDTO                            | tBSD   |     |       | 20  | ns    |
| SDTI1 Hold Time                             | tSDH   | 10  |       |     | ns    |
| SDTI1 Setup Time                            | tSDS   | 10  |       |     | ns    |
| <b>Audio Interface Timing (Master mode)</b> |        |     |       |     |       |
| <b>TDM= "0"</b>                             |        |     |       |     |       |
| BICK Frequency                              | fBCK   |     | 64fs  |     | Hz    |
| BICK Duty                                   | dBCK   |     | 50    |     | %     |
| BICK "↓" to LRCK Edge                       | tMBLR  | -20 |       | 20  | ns    |
| BICK "↓" to SDTO                            | tBSD   |     |       | 40  | ns    |
| SDTI1-3 Hold Time                           | tSDH   | 40  |       |     | ns    |
| SDTI1-3 Setup Time                          | tSDS   | 25  |       |     | ns    |
| <b>TDM= "1"</b>                             |        |     |       |     |       |
| BICK Frequency                              | fBCK   |     | 256fs |     | Hz    |
| BICK Duty                                   | dBCK   |     | 50    |     | %     |
| BICK "↓" to LRCK Edge                       | tMBLR  | -12 |       | 12  | ns    |
| BICK "↓" to SDTO                            | tBSD   |     |       | 20  | ns    |
| SDTI1 Hold Time                             | tSDH   | 10  |       |     | ns    |
| SDTI1 Setup Time                            | tSDS   | 10  |       |     | ns    |

## Notes:

20. BICK rising edge must not occur at the same time as LRCK edge.

21. MSB justified format.

| Parameter  | Symbol  | min  | typ | max | Units |
|--|---------|------|-----|-----|-------|
| <b>Control Interface Timing (3-wire Serial mode):</b>      |         |      |     |     |       |
| CCLK Period  | tCCK    | 200  |     |     | ns    |
| CCLK Pulse Width Low                                       | tCCKL   | 80   |     |     | ns    |
| Pulse Width High   | tCCKH   | 80   |     |     | ns    |
| CDTI Setup Time  | tCDS    | 40   |     |     | ns    |
| CDTI Hold Time   | tCDH    | 40   |     |     | ns    |
| CSN "H" Time   | tCSW    | 150  |     |     | ns    |
| CSN "↓" to CCLK "↑"  | tCSS    | 50   |     |     | ns    |
| CCLK "↑" to CSN "↑"  | tCSH    | 50   |     |     | ns    |
| CDTO Delay   | tDCD    |      |     | 45  | ns    |
| CSN "↑" to CDTO Hi-Z                                       | tCCZ    |      |     | 70  | ns    |
| <b>Control Interface Timing (I<sup>2</sup>C Bus mode):</b> |         |      |     |     |       |
| SCL Clock Frequency  | fSCL    | -    |     | 100 | kHz   |
| Bus Free Time Between Transmissions                        | tBUF    | 4.7  |     | -   | μs    |
| Start Condition Hold Time (prior to first clock pulse)     | tHD:STA | 4.0  |     | -   | μs    |
| Clock Low Time   | tLOW    | 4.7  |     | -   | μs    |
| Clock High Time  | tHIGH   | 4.0  |     | -   | μs    |
| Setup Time for Repeated Start Condition                    | tSU:STA | 4.7  |     | -   | μs    |
| SDA Hold Time from SCL Falling (Note 22)                   | tHD:DAT | 0    |     | -   | μs    |
| SDA Setup Time from SCL Rising                             | tSU:DAT | 0.25 |     | -   | μs    |
| Rise Time of Both SDA and SCL Lines                        | tR      | -    |     | 1.0 | μs    |
| Fall Time of Both SDA and SCL Lines                        | tF      | -    |     | 0.3 | μs    |
| Setup Time for Stop Condition                              | tSU:STO | 4.0  |     | -   | μs    |
| Pulse Width of Spike Noise Suppressed by Input Filter      | tSP     | 0    |     | 50  | ns    |
| <b>Power-down &amp; Reset Timing</b>                       |         |      |     |     |       |
| PDN Pulse Width (Note 23)                                  | tPD     | 150  |     |     | ns    |
| PDN "↑" to SDTO valid (Note 24)                            | tPDV    |      | 522 |     | 1/fs  |

## Notes:

22. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
23. The AK4586 can be reset by bringing PDN "L" to "H" upon power-up.
24. These cycles are the number of LRCK rising from PDN rising.
25. I<sup>2</sup>C is a registered trademark of Philips Semiconductors.

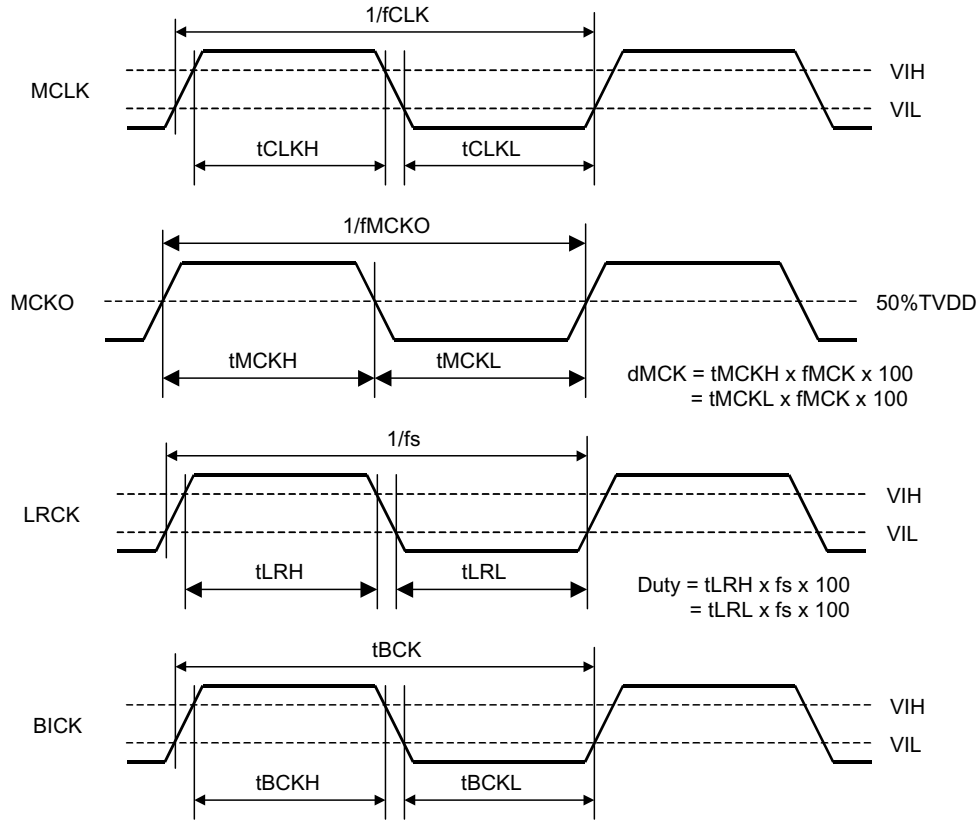
Purchase of Asahi Kasei Microsystems Co., Ltd I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system, provided the system conform to the I<sup>2</sup>C specifications defined by Philips.

### S/PDIF RECEIVER CHARACTERISTICS

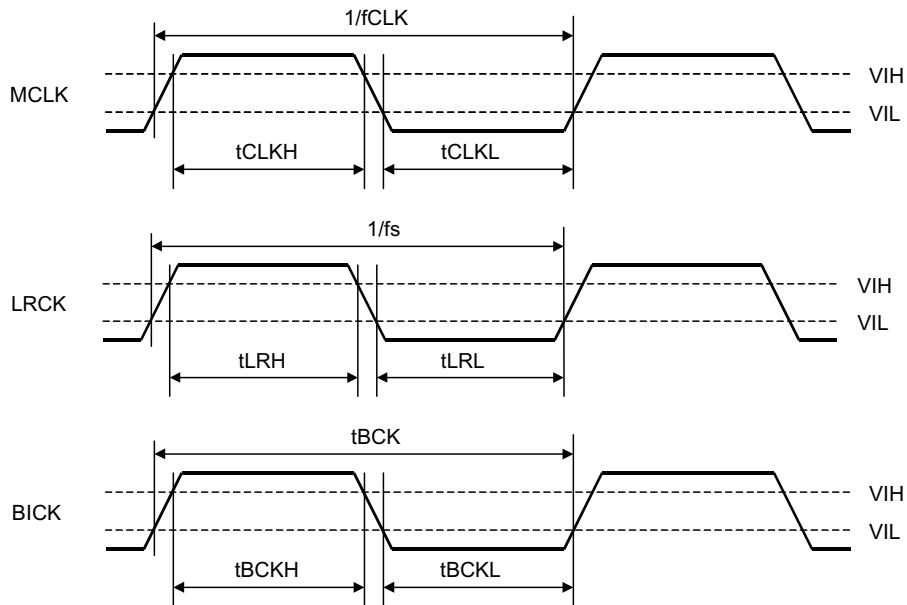
(Ta=25°C; AVDD, DVDD, PVDD=4.5~5.5V; TVDD=2.7~5.5V)

| Parameter              | Symbol | min | typ | max | Units |
|------------------------|--------|-----|-----|-----|-------|
| Input Resistance       | Zin    |     | 10  |     | kΩ    |
| Input Voltage          | VTH    | 200 |     |     | mVpp  |
| Input Hysteresis       | VHY    | -   | 50  |     | mV    |
| Input Sample Frequency | fs     | 32  | -   | 96  | kHz   |

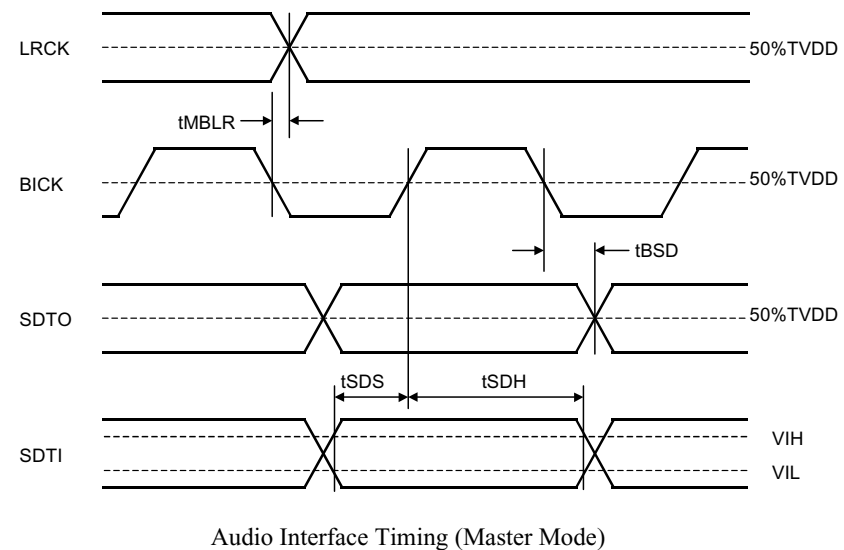
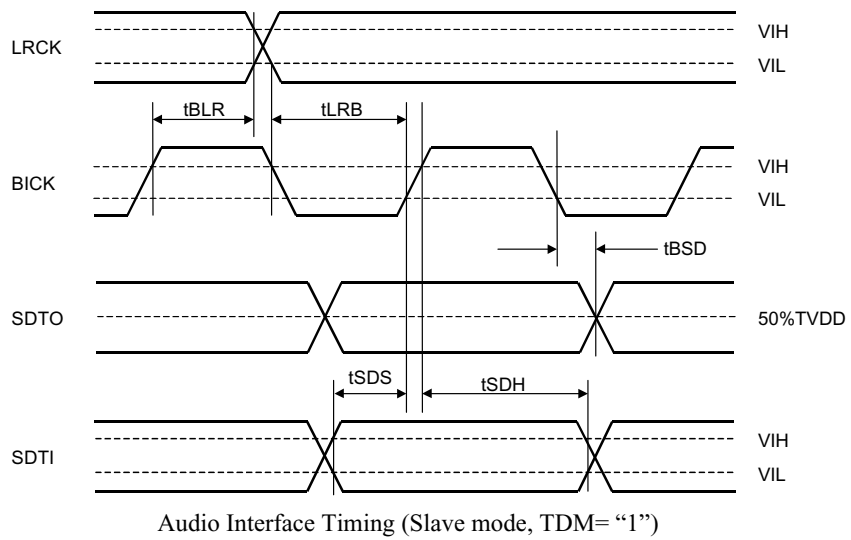
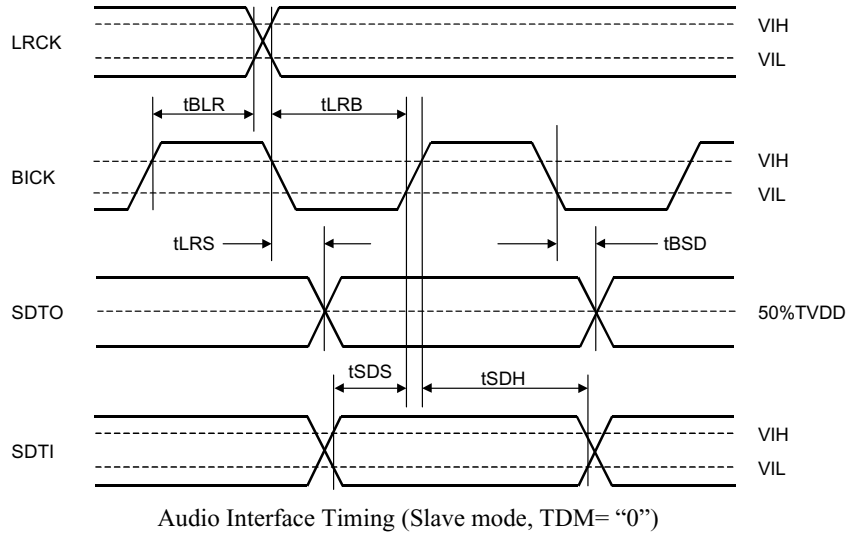
■ Timing Diagram

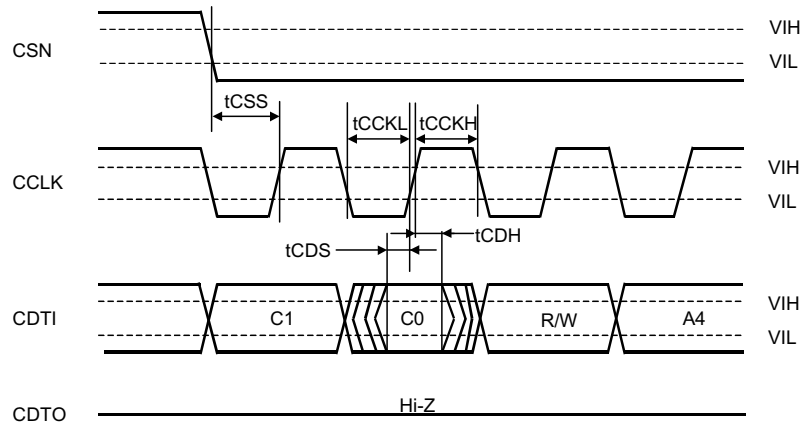


Clock Timing (TDM= "0")

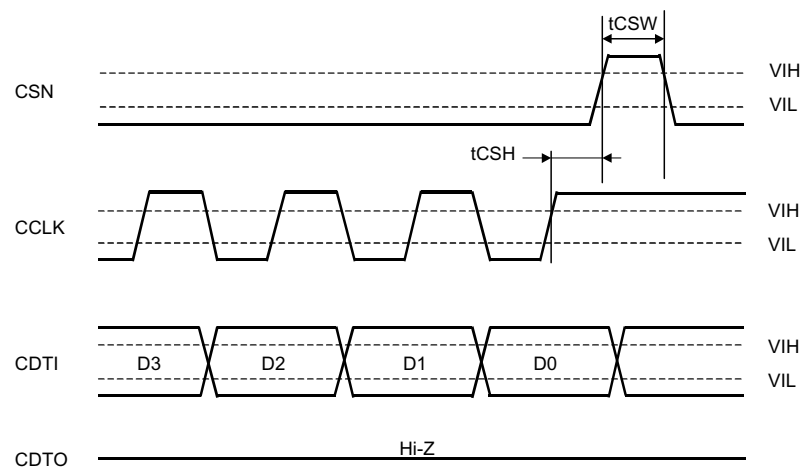


Clock Timing (TDM= "1")

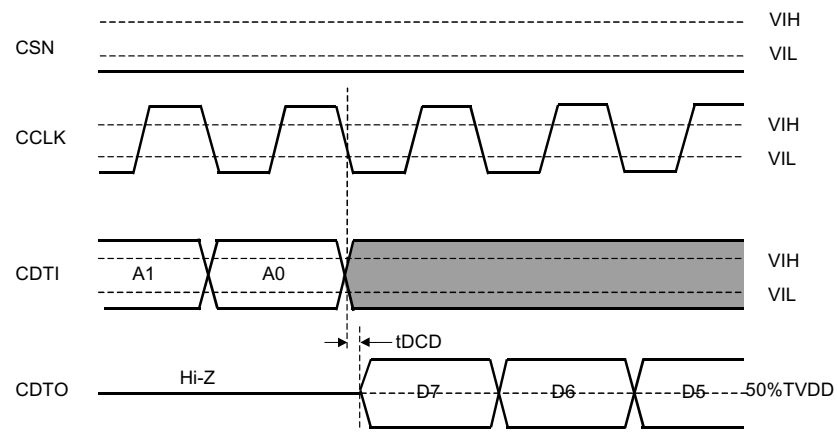




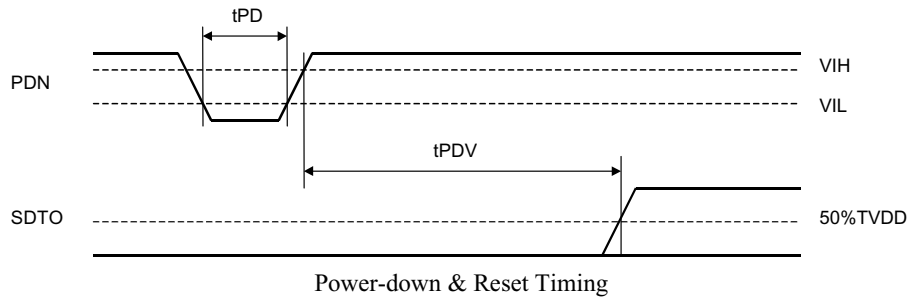
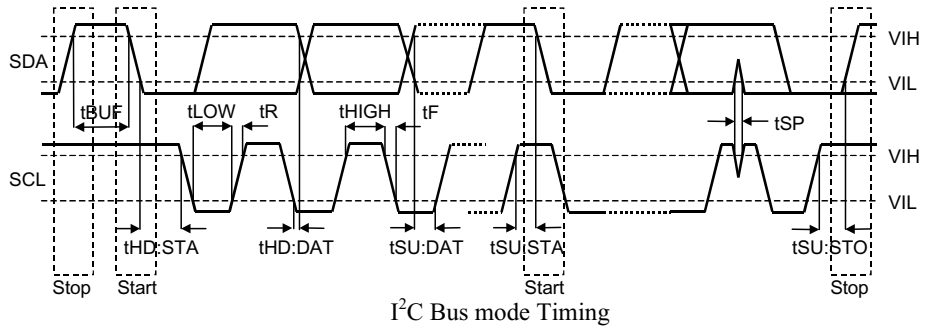
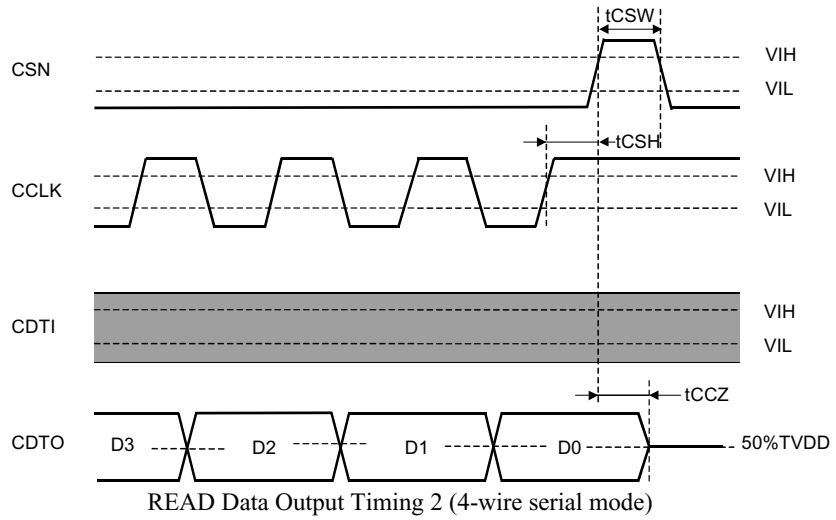
WRITE/READ Command Input Timing (4-wire serial mode)



WRITE Data Input Timing (4-wire serial mode)



READ Data Output Timing 1 (4-wire serial mode)



|                           |
|---------------------------|
| <b>OPERATION OVERVIEW</b> |
|---------------------------|

### ■ Non-PCM (AC-3, MPEG, etc.), DTS-CD Bitstream Detect

The AK4586 has the Non-PCM stream auto detect function. When the 32bit mode Non-PCM preamble based on Dolby “AC-3 Data Stream in IEC60958 Interface” is detected, the AUTO bit goes to “1”. The 16bit mode Non-PCM preamble is not detected. The AUTO bit remains “0” at that time. The 96bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the AUTO bit “1”. Once the AUTO is set to “1”, it will remain “1” until 4096 frames pass through the chip without additional sync pattern being detected. When those preambles are detected, the burst preambles Pc and Pd that follow those sync codes are stored to registers 0DH-10H. The AK4586 also has the DTS-CD stream auto detect function. When the AK4586 detects the DTS-CD bitstreams, the DTSCD bit goes to “1”. When the next sync code does not come within 4096 frames, the DTSCD bit goes to “0” until the AK4586 detects the stream again.

### ■ Clock Recovery and 96kHz Detect

On chip low jitter PLL has a wide lock range with 32kHz to 96kHz and the lock time is less than 20ms. The 96kHz detect bit RFS96 goes to “1” when the sampling rate is 88.2kHz or more and “0” at 48kHz or less. PLL loses lock when the received sync interval is incorrect.

### ■ Clock Operation Mode

The CM0 and CM1 bits select the clock source of MCKO and the data source of SDTO (Table 1). In mode 2, the clock source is switched from PLL to X'tal when PLL goes to the unlock state. In mode 3, the clock source is fixed to X'tal, but PLL is also operating and the recovered data such as C bits can be monitored.

| Mode | CM1 | CM0 | UNLOCK | PLL | X'tal | Clock source | SDTO |
|------|-----|-----|--------|-----|-------|--------------|------|
| 0    | 0   | 0   | -      | ON  | OFF   | PLL          | RX   |
| 1    | 0   | 1   | -      | OFF | ON    | X'tal        | ADC  |
| 2    | 1   | 0   | 0      | ON  | ON    | PLL          | RX   |
|      |     |     | 1      | ON  | ON    | X'tal        | ADC  |
| 3    | 1   | 1   | -      | ON  | ON    | X'tal        | ADC  |

Default

ON: Oscillation (Power-up), OFF: STOP (Power-down)

Table 1. Clock Operation Mode Select

### ■ System Clock

The AK4586 has the master clock output pin, MCKO. This clock is derived from either the recovered clock or from the crystal oscillator. In the PLL mode, the frequency of the master clock output (MCKO) is set by OCKS0 and OCKS1 bits as shown in Table 2. 96kHz sampling is not supported at mode 2. MCKO goes to “L” when the AK4586 detect 96kHz sampling at mode 2. Sampling speed mode is set by RFS96 or XFS96 bit (Table 3). In the x'tal mode, the x'tal frequency rate to fs is set by ICKS1-0 bits (Table 4). In the x'tal mode, the frequency of the MCKO pin becomes half of the crystal oscillator if the CLKDIV bit is set to “1” (Table 5). ICKS1-0 and XFS96 bits should be changed while RSTN bit is “0”. If the external clocks are not present, the AK4586 should be in the power-down mode (PDN= “L”) or in the reset mode (RSTN= “0”).

| Mode | OCKS1 | OCKS0 | MCKO     | fs          |
|------|-------|-------|----------|-------------|
| 0    | 0     | 0     | 256fs    | 32kHz~96kHz |
| 1    | 0     | 1     | 128fs    | 32kHz~96kHz |
| 2    | 1     | 0     | 512fs    | 32kHz~48kHz |
| 3    | 1     | 1     | Reserved |             |

Default

Table 2. Master Clock Output Frequency Select (PLL mode)

| Clock mode | AFS96 | RFS96 | XFS96 | Sampling Speed (fs) |                   |
|------------|-------|-------|-------|---------------------|-------------------|
|            |       |       |       | Normal Speed Mode   | Double Speed Mode |
| X'tal mode | x     | x     | 0     | Normal Speed Mode   | 44.1kHz~48kHz     |
|            |       |       | 1     | Double Speed Mode   | 88.2kHz~96kHz     |
| PLL mode   | 0     | x     | 0     | Normal Speed Mode   | 32kHz~48kHz       |
|            |       |       | 1     | Double Speed Mode   | 88.2kHz~96kHz     |
|            | 1     | 0     | x     | Normal Speed Mode   | 32kHz~48kHz       |
|            |       |       | 1     | x                   | Double Speed Mode |

Table 3. Sampling Speed Mode (x: Don't care)

| Mode | ICKS1 | ICKS0 | Normal | Double | Default |
|------|-------|-------|--------|--------|---------|
| 0    | 0     | 0     | 256fs  | 128fs  |         |
| 1    | 0     | 1     | 384fs  | 192fs  |         |
| 2    | 1     | 0     | 512fs  | 256fs  |         |
| 3    | 1     | 1     | 256fs  | 256fs  |         |

Table 4. Master Clock Input Frequency Select (X'tal mode)  
 (In the x'tal mode, ADC is automatically powered down at 128fs and 192fs in the double speed mode.)

| CLKDIV | MCKO     | Default |
|--------|----------|---------|
| 0      | XTI x1   |         |
| 1      | XTI x1/2 |         |

Table 5. Master Clock Output Select (X'tal mode)

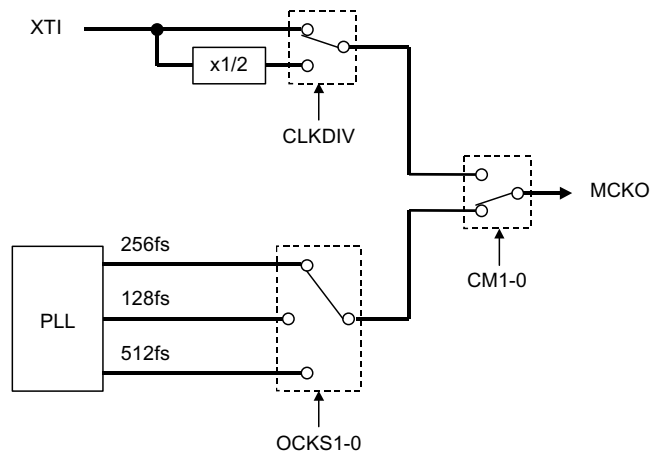


Figure 1. Master Clock Output Select

■ Clock Source

The following circuits are available to feed the clock to XTI pin of AK4586.

1) X'tal

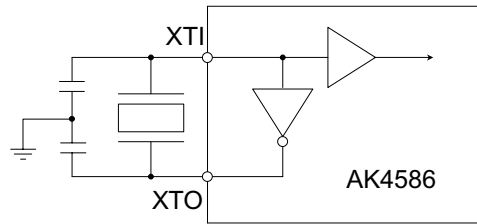


Figure 2. X'tal mode

Note: External capacitance depends on the crystal oscillator (Typ. 10-40pF)

2) External clock

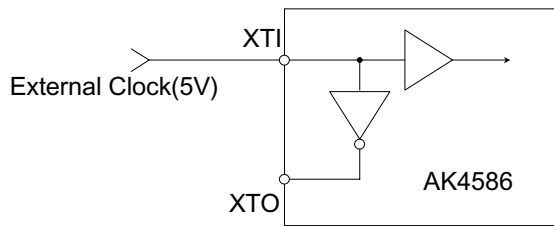


Figure 3. External clock mode(5V)

Note: Input clock must not exceed DVDD.

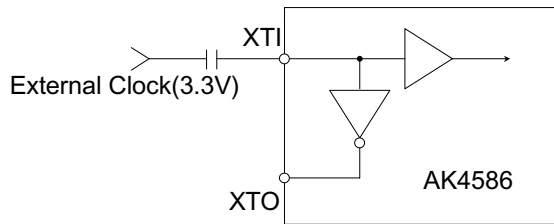


Figure 4. External clock mode(3.3V)

Note: 3.3V external clock should be AC coupled.

The amplitude of the clock should be larger than 40%DVDD.

3) Fixed to the Clock Operation Mode 0

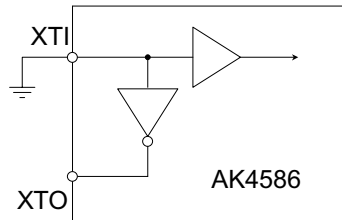


Figure 5. Off mode

### ■ Sampling Frequency and Pre-emphasis Detect

The AK4586 outputs the encoded information of sampling frequency and pre-emphasis in channel status to FS0, FS1 and PEM bits in control register. These information are output from channel 1 at default. It can be switched to channel 2 by CS12 bit in control register.

| FS1 | FS0 | fs       | Byte 3<br>Bits 0-3 |
|-----|-----|----------|--------------------|
| 0   | 0   | 44.1kHz  | 0000               |
| 0   | 1   | Reserved | all others         |
| 1   | 0   | 48kHz    | 0100               |
| 1   | 1   | 32kHz    | 1100               |

Table 6. Sampling frequency information in Consumer Mode

| PEM | Pre-emphasis | Byte 0<br>Bits 3-5 |
|-----|--------------|--------------------|
| 0   | OFF          | ≠ 0X100            |
| 1   | ON           | 0X100              |

Table 7. Pre-emphasis information in Consumer Mode

## ■ De-emphasis Filter Control

The AK4586 includes the digital de-emphasis filter ( $t_c=50/15\mu s$ ) by IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz). When DEAU bit = "1", the de-emphasis filter is enabled automatically by sampling frequency and pre-emphasis information in the channel status. The AK4586 goes to this mode at default and the de-emphasis filter is controlled by the status bits in channel 1 (Table 8). DEM1-0 and DFS bits can control the de-emphasis filter when DEAU is "0" (Table 9). The internal de-emphasis filter is bypassed and the recovered data is output without any change if either pre-emphasis or de-emphasis mode is OFF. The internal de-emphasis filter is bypassed if the Non-PCM or the DTS-CD bitstream is detected at DEAU= "1". The internal de-emphasis filter is bypassed if bit 0 of the channel status byte 0 is "1".

| RFS96 | FS1 | FS0 | DEM     |
|-------|-----|-----|---------|
| 0     | 0   | 0   | 44.1kHz |
| 0     | 0   | 1   | OFF     |
| 0     | 1   | 0   | 48kHz   |
| 0     | 1   | 1   | 32kHz   |
| 1     | 0   | 0   | OFF     |
| 1     | 0   | 1   | OFF     |
| 1     | 1   | 0   | OFF     |
| 1     | 1   | 1   | OFF     |

Default

Table 8. De-emphasis Auto Control at DEAU="1" and PEM="1"

| Sampling Speed | DEM1 | DEM0 | DEM     |
|----------------|------|------|---------|
| Normal Speed   | 0    | 0    | 44.1kHz |
| Normal Speed   | 0    | 1    | OFF     |
| Normal Speed   | 1    | 0    | 48kHz   |
| Normal Speed   | 1    | 1    | 32kHz   |
| Double Speed   | 0    | 0    | OFF     |
| Double Speed   | 0    | 1    | OFF     |
| Double Speed   | 1    | 0    | OFF     |
| Double Speed   | 1    | 1    | OFF     |

Default

Table 9. De-emphasis Manual Control at DEAU="0" and PEM="1"

## ■ System Reset and Power-Down

The AK4586 has a power-down mode for all circuits by PDN pin or can be partially powered-down by internal register. The AK4586 should be reset once by bringing PDN pin = "L" upon power-up. ADC, DAC and PLL are powered-down at PWVRN= "0".

| PDN | PWADN | PWDAN | PWVRN | RSTN | CM1-0 | Function         | Register initialization |
|-----|-------|-------|-------|------|-------|------------------|-------------------------|
| L   | x     | x     | x     | x    | x     | All power down   | Yes                     |
| x   | 0     | x     | x     | x    | x     | ADC power down   | No                      |
| x   | x     | 0     | x     | x    | x     | DAC power down   | No                      |
| x   | x     | x     | 0     | x    | x     | VREF power down  | No                      |
| x   | x     | x     | x     | 0    | x     | Timing Reset     | No                      |
| x   | x     | x     | x     | x    | 00    | X'tal power down | No                      |
| x   | x     | x     | x     | x    | 01    | PLL power down   | No                      |

Table 10. Reset & Power Down

■ **Biphase Input and Through Output**

Four receiver inputs (RX1-4) are available. Each input includes amplifier corresponding to unbalance mode and can accept the signal of 200mV or more. IPS1-0 selects the receiver channel (Table 11), and OPS1-0 selects the source of the bit stream driving the transmit channel (TX, Table 12). The TX output can be stopped by setting TXE bit “0”.

| IPS1 | IPS0 | INPUT Data |
|------|------|------------|
| 0    | 0    | RX1        |
| 0    | 1    | RX2        |
| 1    | 0    | RX3        |
| 1    | 1    | RX4        |

Default

Table 11. Recovery data select

| OPS1 | OPS0 | INPUT Data |
|------|------|------------|
| 0    | 0    | RX1        |
| 0    | 1    | RX2        |
| 1    | 0    | RX3        |
| 1    | 1    | RX4        |

Default

Table 12. Output data select

■ Biphase signal input/output circuit

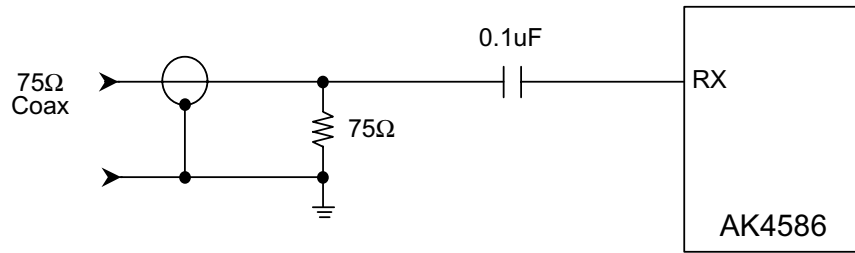


Figure 6. Consumer Input Circuit (Coaxial Input)

- Note 1: In case of coaxial input, if a coupling level to this input from the next RX input line pattern exceeds 50mV, there is a possibility to occur an incorrect operation. In this case, it is possible to lower the coupling level by adding this decoupling capacitor.
- Note 2: Ground of RCA connector and terminator should be connected to PVSS of the AK4586 with low impedance on PC board.

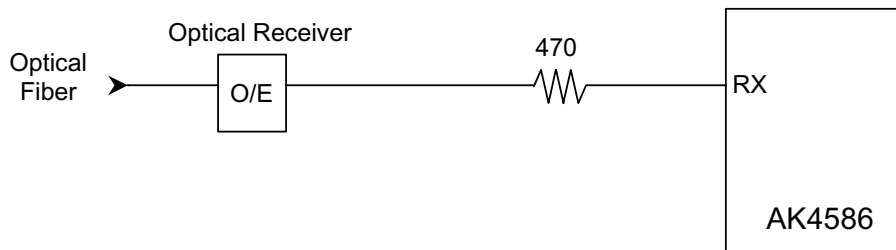


Figure 7. Consumer Input Circuit (Optical Input)

In case of coaxial input, as the input level of RX line is small, be careful not to crosstalk among RX input lines. For example, by inserting the shield pattern among them.

The AK4586 includes the TX output buffer. The output level meets combination 0.5V+/-20% using the external resistor network. The T1 in Figure 8 is a transformer of 1:1.

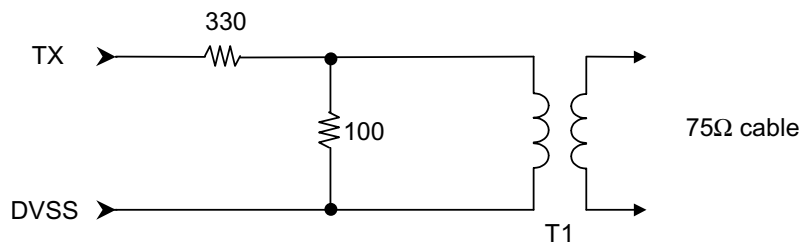


Figure 8. TX External Resistor Network

■ Error Handling

There are the following eight factors which INT1-0 pins go to “H”.

1. UNLOCK: “1” when the PLL goes UNLOCK state.  
The AK4586 loses lock when the distance between two preambles is not correct or when those preambles are not correct.
2. PAR: “1” when parity error or biphas coding error is detected.  
Updated every sub-frame cycle. Reading this register resets itself.
3. AUTO: “1” when Non-PCM Bit Stream is detected.
4. DTSCD: “1” when DTS-CD Bit Stream is detected.
5. AUDION: “1” when the “AUDIO” bit in recovered channel status indicates “1”.
6. STC: “1” when FS1, FS0 or PEM bit changes. Reading this register resets itself.
7. V: “1” when validity flag is detected.
8. RFS96: “1” when fs=88.2kHz or more (RFS96 bit is set by XFS96 bit at x’tal mode or AFS96= “0”).

INT1-0 pins output the ORed signal among those eight factors. However, each factor can be masked by each mask bit. When each bit masks those factors, the factor does not affect INT1-0 pins operation (those masks do not affect those registers (UNLOCK, PAR, etc.) themselves). Once INT0 pin goes to “H”, it maintains “H” for 1024 cycles (this value can be changed by EFH1-0 bits) after the all factors are removed. Once the PAR bit goes to “1”, it holds “1” until reading the register. While the AK4586 loses lock, the channel status bits are not updated and hold the previous data. At initial state, INT0 outputs the ORed signal between UNLOCK and PAR. INT1 outputs the ORed signal among AUTO, DTSCD, AUDION and V. INT1-0 pins are “L” when the PLL is OFF (Clock Operation Mode 1).

| Register |     |      |       |        |     |   |       | Pin           |        |
|----------|-----|------|-------|--------|-----|---|-------|---------------|--------|
| UNLOCK   | PAR | AUTO | DTSCD | AUDION | STC | V | RFS96 | SDTO          | TX     |
| 1        | x   | x    | x     | x      | x   | x | x     | “L”           | Output |
| 0        | 1   | x    | x     | x      | x   | x | x     | Previous Data | Output |
| 0        | 0   | 1    | x     | x      | x   | x | x     | Output        | Output |
| 0        | 0   | x    | 1     | x      | x   | x | x     | Output        | Output |
| 0        | 0   | x    | x     | 1      | x   | x | x     | Output        | Output |
| 0        | 0   | x    | x     | x      | 1   | x | x     | Output        | Output |
| 0        | 0   | x    | x     | x      | x   | 1 | x     | Output        | Output |
| 0        | 0   | x    | x     | x      | x   | x | 1     | Output        | Output |

Table 13. Error handling

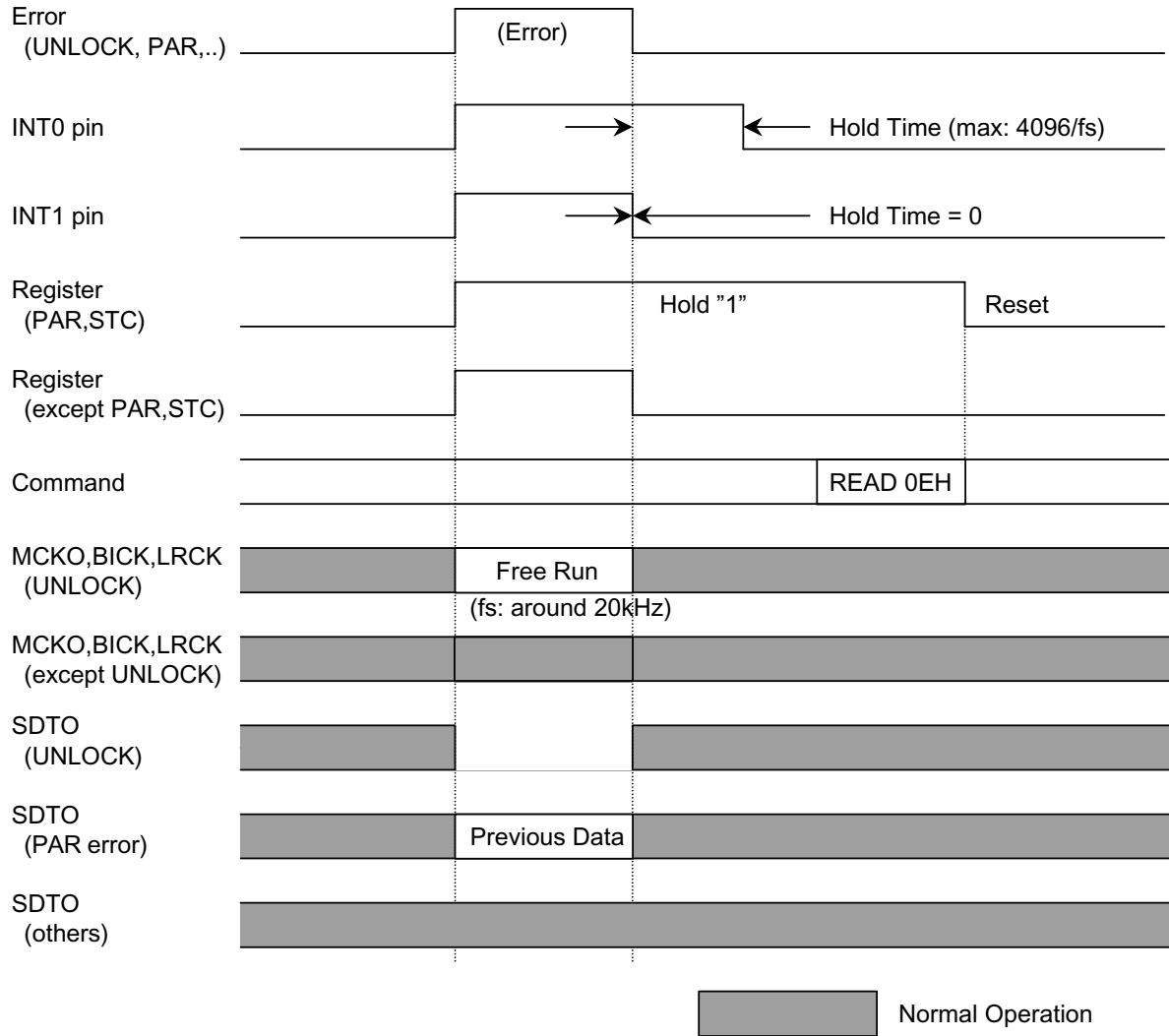


Figure 9. INT0/1 pin timing

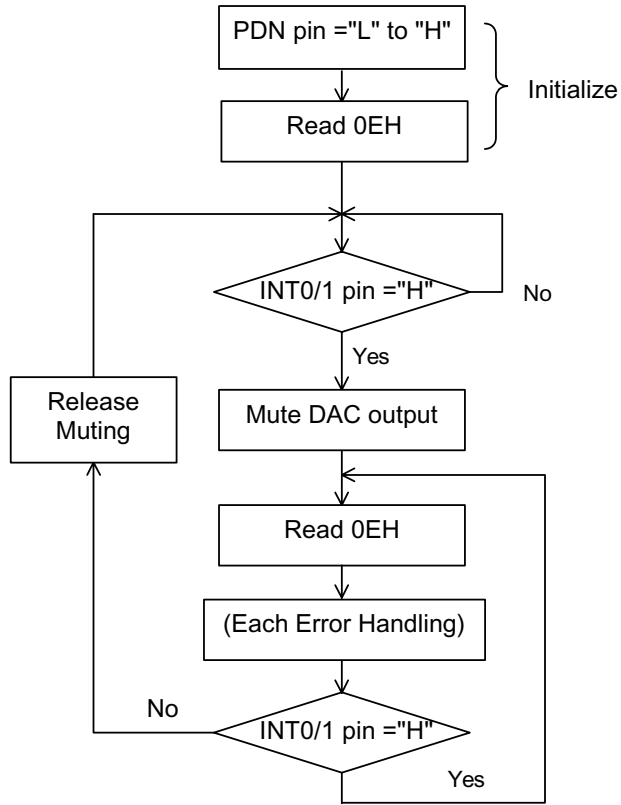


Figure 10. Error Handling Sequence Example

■ Audio Serial Interface Format

Eight serial data formats can be selected by the DIF2-0 bits as shown in Table 14 at the SLAVE pin “L”. If the SLAVE pin is “H”, the AK4586 is fixed in the slave mode and two serial data format can be selected by the DIF0 bit. In all formats the serial data is MSB-first, 2’s compliment format. The SDTO is clocked out on the falling edge of BICK and the SDTI1-3 are latched on the rising edge of BICK. BICK outputs 64fs clock in Mode 0-5. Mode 6-7 are the slave mode, and BICK is available up to 128fs at fs=48kHz. In the format equal or less than 20bit (mode 0-2), LSBs in sub-frame are truncated. In mode 3-7, the last 4LSBs are auxiliary data (see Figure 11).

When the Parity Error or Biphase Error occurs in a sub-frame, the AK4586 continues to output the last normal sub-frame data from SDTO repeatedly until the error is removed. When the Unlock Error occurs, the AK4586 outputs “0” from SDTO.

Mode 4, 5, 6 and 7 in SDTI input formats can be used for 16-20bit data by zeroing the unused LSBs.

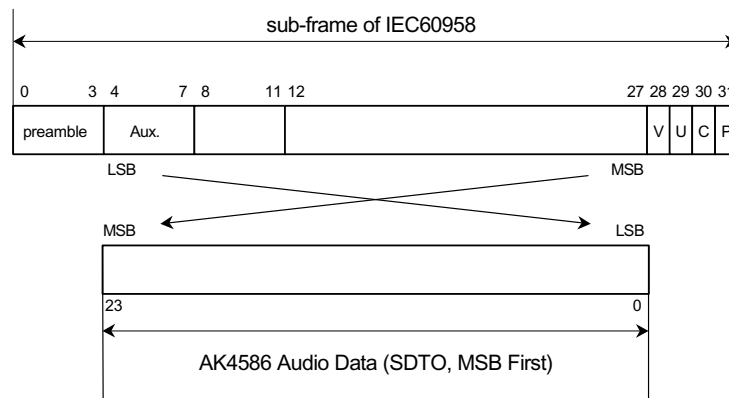


Figure 11. Bit configuration

| Mode | SLAVE | DIF |   |                         | SDTO                    | SDTI1-3                 | LRCK |          | BICK     |   |
|------|-------|-----|---|-------------------------|-------------------------|-------------------------|------|----------|----------|---|
|      |       | 2   | 1 | 0                       |                         |                         | I/O  | I/O      |          |   |
| 0    | 0     | 0   | 0 | 0                       | 16bit, Right justified  | 16bit, Right justified  | H/L  | O        | 64fs     | O |
| 1    |       | 0   | 0 | 1                       | 18bit, Right justified  | 18bit, Right justified  | H/L  | O        | 64fs     | O |
| 2    |       | 0   | 1 | 0                       | 20bit, Right justified  | 20bit, Right justified  | H/L  | O        | 64fs     | O |
| 3    |       | 0   | 1 | 1                       | 24bit, Right justified  | 24bit, Right justified  | H/L  | O        | 64fs     | O |
| 4    |       | 1   | 0 | 0                       | 24bit, Left justified   | 24bit, Left justified   | H/L  | O        | 64fs     | O |
| 5    |       | 1   | 0 | 1                       | 24bit, I <sup>2</sup> S | 24bit, I <sup>2</sup> S | L/H  | O        | 64fs     | O |
| 6    |       | 1   | 1 | 0                       | 24bit, Left justified   | 24bit, Left justified   | H/L  | I        | 64-128fs | I |
| 7    | 1     | 1   | 1 | 24bit, I <sup>2</sup> S | 24bit, I <sup>2</sup> S | L/H                     | I    | 64-128fs | I        |   |
| 6    | 1     | x   | x | 0                       | 24bit, Left justified   | 24bit, Left justified   | H/L  | I        | 64-128fs | I |
| 7    |       | x   | x | 1                       | 24bit, I <sup>2</sup> S | 24bit, I <sup>2</sup> S | L/H  | I        | 64-128fs | I |

Default

Table 14. Audio Data Format (TDM= “0”)

The audio serial interface format becomes the TDM I/F format if TDM bit is set to “1”. In the TDM mode, the serial data of all DAC (six channels) is input to the SDTI1 pin. The input data to SDTI2-3 pins is ignored. BICK should be fixed to 256fs. In the slave mode, “H” time and “L” time of LRCK should be 1/256fs at least. In the master mode, “H” time (“L” time at I<sup>2</sup>S mode) of LRCK is 1/8fs typically. LOOP1-0 should be set to “00” at the TDM mode. TDM mode cannot be used in double speed mode.

| Mode | SLAVE | DIF |   |   | SDTO                    | SDTI1-3                 | LRCK |     | BICK  |   |
|------|-------|-----|---|---|-------------------------|-------------------------|------|-----|-------|---|
|      |       | 2   | 1 | 0 |                         |                         | I/O  | I/O |       |   |
| 8    | 0     | 0   | 0 | 0 | 16bit, Right justified  | 16bit, Right justified  | ↑    | O   | 256fs | O |
| 9    |       | 0   | 0 | 1 | 18bit, Right justified  | 18bit, Right justified  | ↑    | O   | 256fs | O |
| 10   |       | 0   | 1 | 0 | 20bit, Right justified  | 20bit, Right justified  | ↑    | O   | 256fs | O |
| 11   |       | 0   | 1 | 1 | 24bit, Right justified  | 24bit, Right justified  | ↑    | O   | 256fs | O |
| 12   |       | 1   | 0 | 0 | 24bit, Left justified   | 24bit, Left justified   | ↑    | O   | 256fs | O |
| 13   |       | 1   | 0 | 1 | 24bit, I <sup>2</sup> S | 24bit, I <sup>2</sup> S | ↓    | O   | 256fs | O |
| 14   |       | 1   | 1 | 0 | 24bit, Left justified   | 24bit, Left justified   | ↑    | I   | 256fs | I |
| 15   |       | 1   | 1 | 1 | 24bit, I <sup>2</sup> S | 24bit, I <sup>2</sup> S | ↓    | I   | 256fs | I |
| 14   | 1     | x   | x | 0 | 24bit, Left justified   | 24bit, Left justified   | ↑    | I   | 256fs | I |
| 15   |       | x   | x | 1 | 24bit, I <sup>2</sup> S | 24bit, I <sup>2</sup> S | ↓    | I   | 256fs | I |

Table 15. Audio Data Format (TDM= “1”)

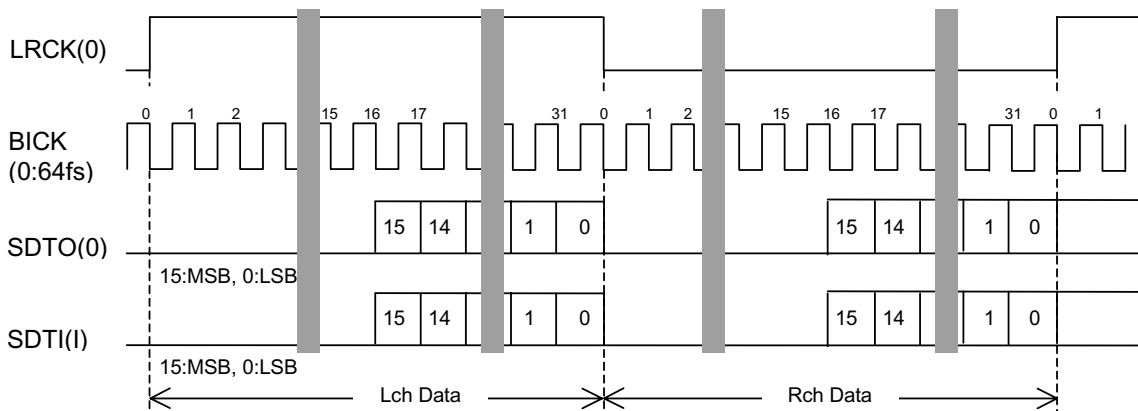


Figure 12. Mode 0 Timing

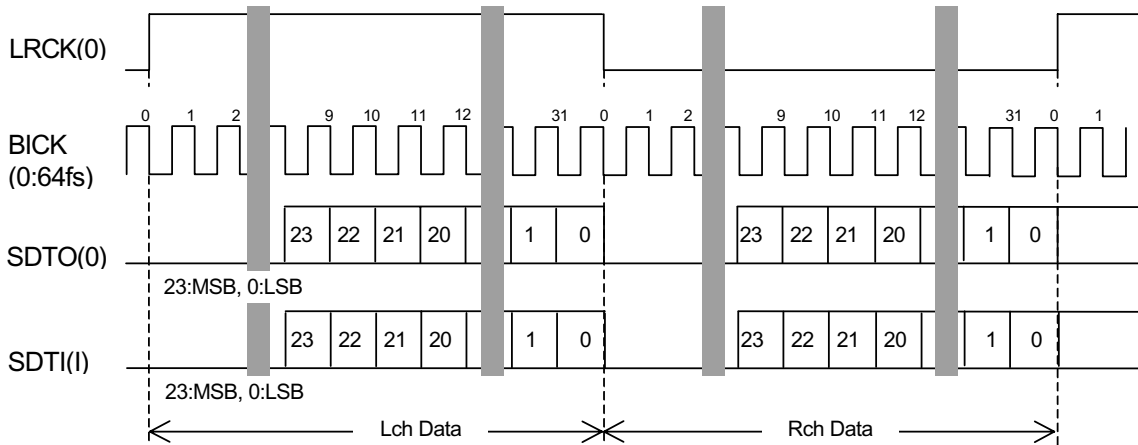


Figure 13. Mode 3 Timing

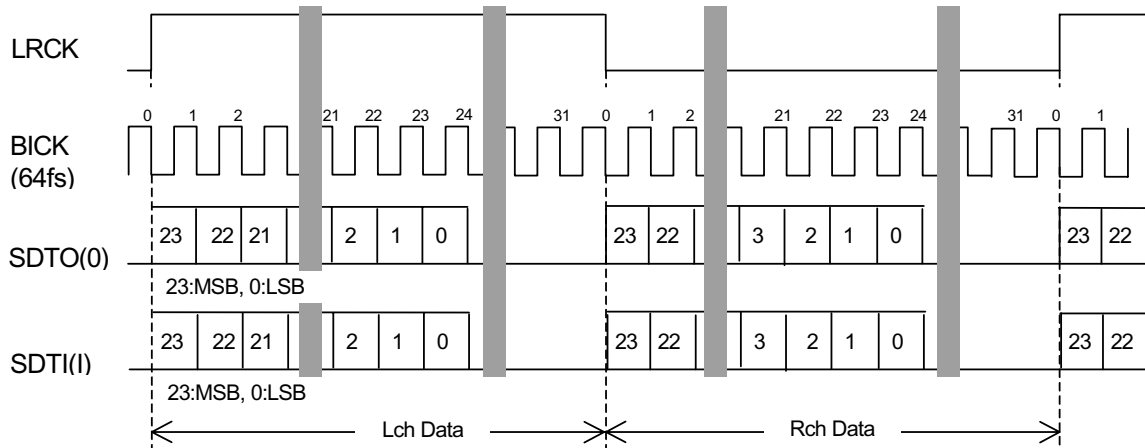


Figure 14. Mode 4, 6 Timing  
 Mode 4: LRCK, BICK: Output  
 Mode 6: LRCK, BICK: Input

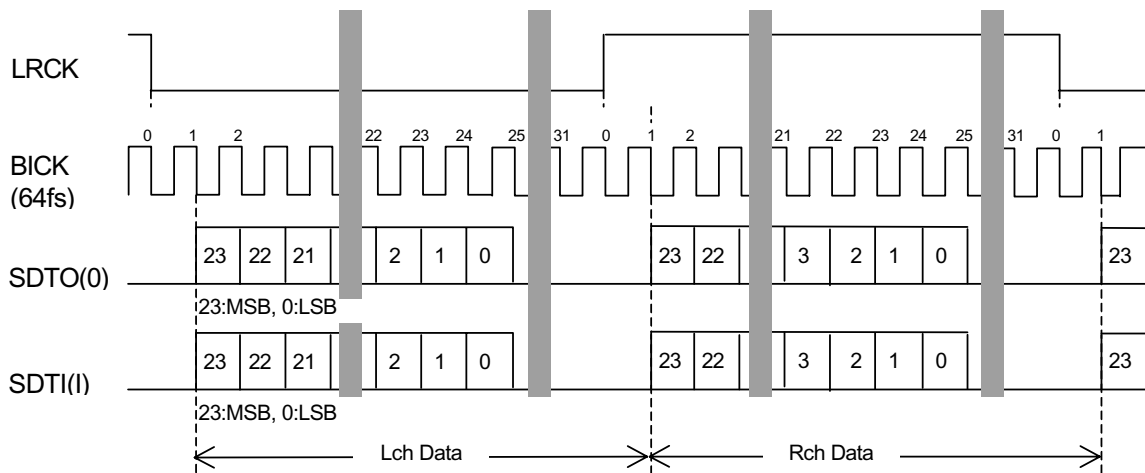


Figure 15. Mode 5, 7 Timing  
 Mode 5: LRCK, BICK: Output  
 Mode 7: LRCK, BICK: Input

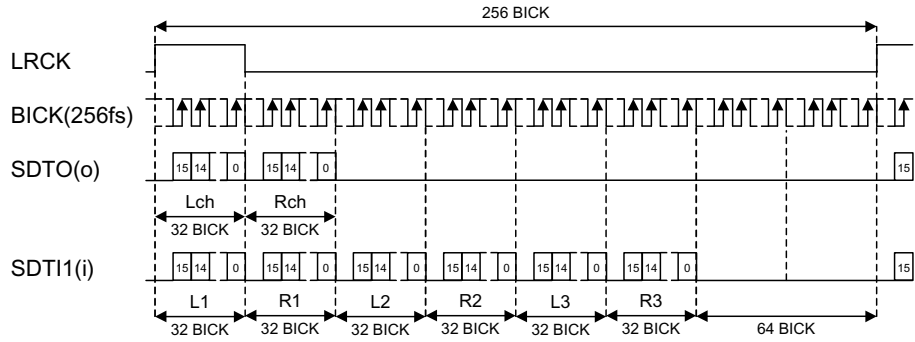


Figure 16. Mode 8 Timing

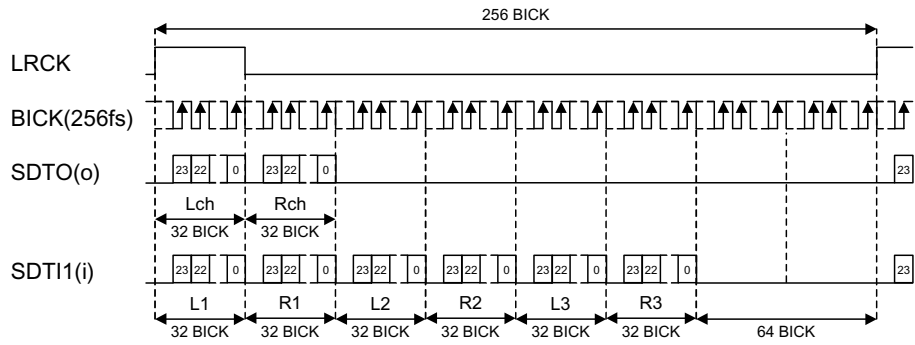
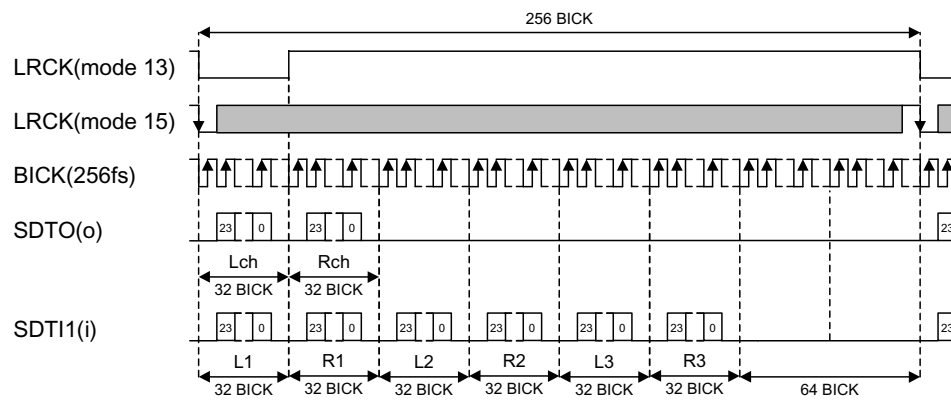
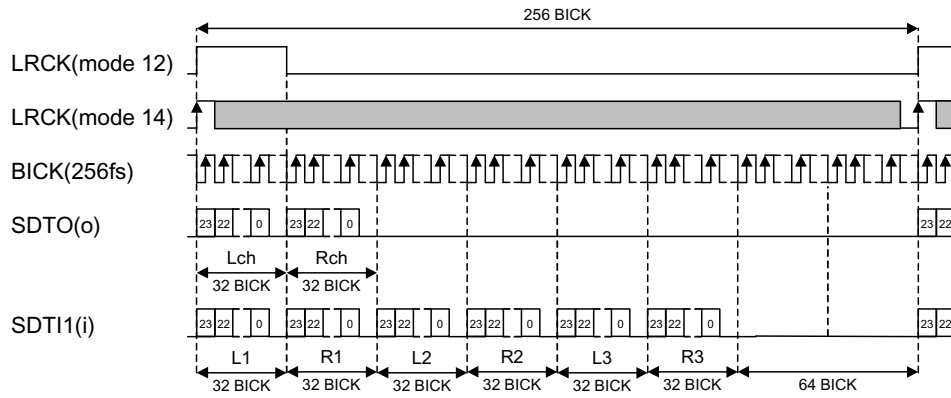


Figure 17. Mode 11 Timing



### ■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 1.0Hz at  $f_s=48\text{kHz}$  and also scales with sampling rate ( $f_s$ ).

### ■ Overflow Detection

The AK4586 has overflow detect function for analog input. Overflow detect function is enable if OVFE bit is set to “1”. OVF pin goes to “H” if analog input of Lch or Rch overflows (more than -0.3dBFS). OVF output for overflowed analog input has the same group delay as ADC ( $GD = 17.0/f_s = 354\mu\text{s}@f_s=48\text{kHz}$ ). OVF is “L” for  $522/f_s (=10.9\text{ms}@f_s=48\text{kHz})$  after PDN = “↑”, and then overflow detection is enabled.

### ■ Zero detection

The AK4586 has two pins for zero detect flag outputs. Channel grouping can be selected by DZFM2-0 bits (Table 16). DZF1 pin corresponds to the group 1 channels and DZF2 pin corresponds to the group 2 channels. However DZF2 pin becomes OVF pin if OVFE bit is set to “1”. For example, DZF1 is AND of all six channels and DZF2 is disabled (“L”) at mode 0.

When the input data of all channels in the group 1(group 2) are continuously zeros for 8192 LRCK cycles, DZF1(DZF2) pin goes to “H”. DZF1(DZF2) pin immediately goes to “L” if input data of any channels in the group 1(group 2) is not zero after going DZF1(DZF2) “H”.

| Mode | DZFM |   |   | AOUT                      |      |      |      |      |      |         |
|------|------|---|---|---------------------------|------|------|------|------|------|---------|
|      | 2    | 1 | 0 | L1                        | R1   | L2   | R2   | L3   | R3   |         |
| 0    | 0    | 0 | 0 | DZF1                      | DZF1 | DZF1 | DZF1 | DZF1 | DZF1 |         |
| 1    | 0    | 0 | 1 | DZF1                      | DZF1 | DZF1 | DZF1 | DZF1 | DZF2 |         |
| 2    | 0    | 1 | 0 | DZF1                      | DZF1 | DZF1 | DZF1 | DZF2 | DZF2 |         |
| 3    | 0    | 1 | 1 | DZF1                      | DZF1 | DZF1 | DZF2 | DZF2 | DZF2 |         |
| 4    | 1    | 0 | 0 | DZF1                      | DZF1 | DZF2 | DZF2 | DZF2 | DZF2 |         |
| 5    | 1    | 0 | 1 | DZF1                      | DZF2 | DZF2 | DZF2 | DZF2 | DZF2 |         |
| 6    | 1    | 1 | 0 | DZF2                      | DZF2 | DZF2 | DZF2 | DZF2 | DZF2 |         |
| 7    | 1    | 1 | 1 | disable (DZF1=DZF2 = “L”) |      |      |      |      |      | Default |

Table 16. Zero detect control

## ■ Digital Attenuator

The AK4586 has channel-independent digital attenuator (256 levels, 0.5dB step). Attenuation level of each channel can be set by each ATT7-0 bits (Table 17).

| ATT7-0 | Attenuation Level  |
|--------|--------------------|
| 00H    | 0dB                |
| 01H    | -0.5dB             |
| 02H    | -1.0dB             |
| :      | :                  |
| FDH    | -126.5dB           |
| FEH    | -127.0dB           |
| FFH    | MUTE ( $-\infty$ ) |

Default

Table 17. Attenuation level of digital attenuator

Transition time between set values of ATT7-0 bits can be selected by ATS1-0 bits (Table 18).

| Mode | ATS1 | ATS0 | ATT speed |
|------|------|------|-----------|
| 0    | 0    | 0    | 7424/fs   |
| 1    | 0    | 1    | 1061/fs   |
| 2    | 1    | 0    | 256/fs    |
| 3    | 1    | 1    | Reserved  |

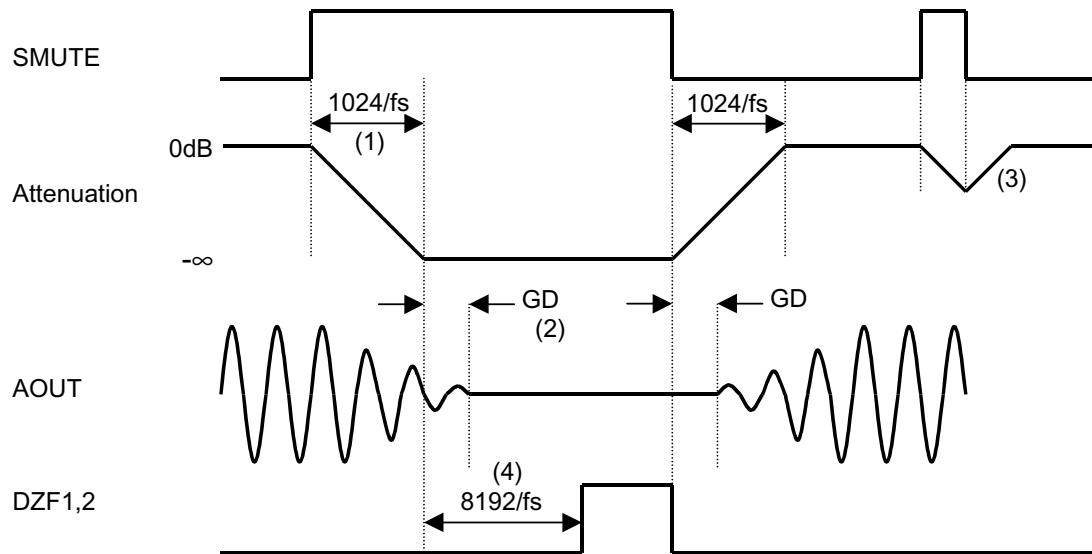
Default

Table 18. Transition time between set values of ATT7-0 bits

The transition between set values is soft transition of 7425 levels in mode 0. It takes 7424/fs (155ms@fs=48kHz) from 00H(0dB) to FFH(MUTE) in mode 0. If PDN pin goes to “L”, the ATTs are initialized to 00H. The ATTs are 00H when RSTN = “0”. When RSTN return to “1”, the ATTs fade to their current value. Digital attenuator is independent of soft mute function.

### ■ Soft mute operation

Soft mute operation is performed at digital domain. When the SMUTE bit goes to “1”, the output signal is attenuated by  $-\infty$  during 1024 LRCK cycles. When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

- (1) The output signal is attenuated by  $-\infty$  during 1024 LRCK cycles ( $1024/f_s$ ).
- (2) Analog output corresponding to digital input have the group delay (GD).
- (3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.
- (4) When the input data of all channels in the group are continuously zeros for 8192 LRCK cycles, DZF pin corresponding to the group goes to “H”. DZF pin immediately goes to “L” if input data of any channel in the group is not zero after going DZF “H”.

Figure 20. Soft mute and zero detection

■ Serial Control Interface

(1) 4-wire Serial Control Mode (I2C = "L")

The internal registers may be either written or read by the 4-wire  $\mu$ P interface pins: CSN, CCLK, CDTI & CDTO. The data on this interface consists of Chip address (2bits, CAD1-0 are fixed to "00"), Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. For read operations, the CDTO output goes high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. PDN= "L" resets the registers to their default values.

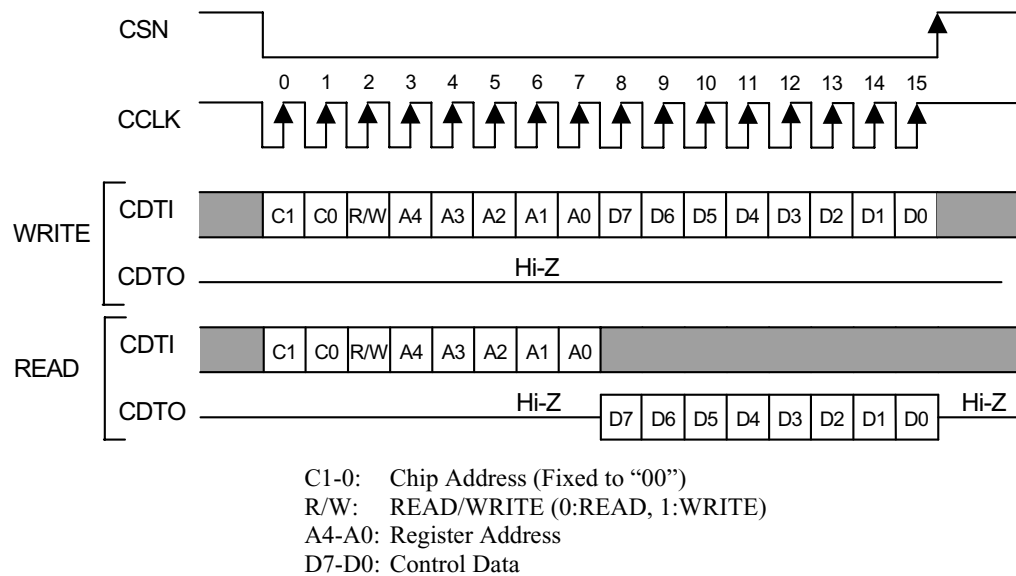


Figure 21. 4-wire Serial Control I/F Timing

(2) I<sup>2</sup>C-bus Control Mode (I2C= "H")

AK4586 supports the standard-mode I<sup>2</sup>C-bus (max:100kHz). Then AK4586 cannot be incorporated in a fast-mode I<sup>2</sup>C-bus system (max:400kHz).

(2)-1. WRITE Operations

Figure 22 shows the data transfer sequence at the I<sup>2</sup>C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 28). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The hard-wired input pins (CAD1 pin and CAD0 pin) set them (Figure 23). If the slave address match that of the AK4586, the AK4586 generates the acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 29). A "1" for R/W bit indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the address for control registers of the AK4586. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 24). Those data after the second byte contain control data. The format is MSB first, 8bits (Figure 25). The AK4586 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 28).

The AK4586 is capable of more than one byte write operation by one sequence. After receipt of the third byte, the AK4586 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 1FH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 30) except for the START and the STOP condition.

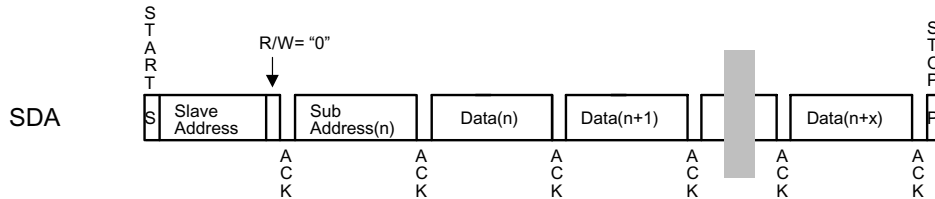


Figure 22. Data transfer sequence at the I<sup>2</sup>C-bus mode

|   |   |   |   |   |      |      |     |
|---|---|---|---|---|------|------|-----|
| 0 | 0 | 1 | 0 | 0 | CAD1 | CAD0 | R/W |
|---|---|---|---|---|------|------|-----|

(Those CAD1/0 should match with CAD1/0 pins)

Figure 23. The first byte

|   |   |   |    |    |    |    |    |
|---|---|---|----|----|----|----|----|
| 0 | 0 | 0 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|----|----|----|----|----|

Figure 24. The second byte

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

Figure 25. Byte structure after the second byte

(2)-2. READ Operations

Set R/W bit = "1" for the READ operation of the AK4586. After transmission of a data, the master can read next address's data by generating the acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 1FH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4586 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4586 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4586 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4586 discontinues transmission

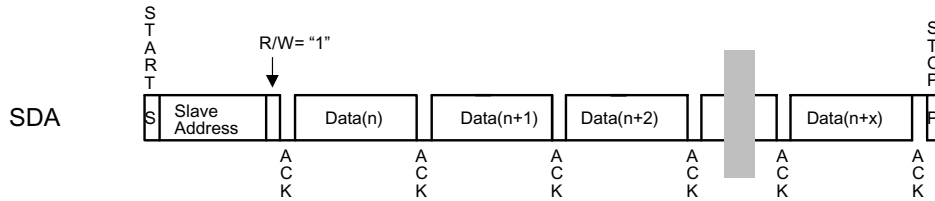


Figure 26. CURRENT ADDRESS READ

(2)-3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues the start condition, slave address(R/W="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4586 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4586 discontinues transmission.

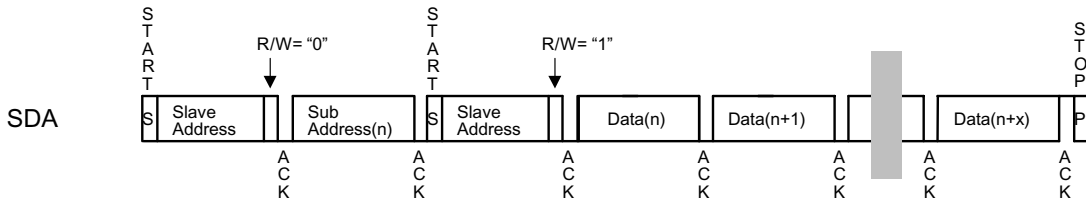


Figure 27. RANDOM ADDRESS READ

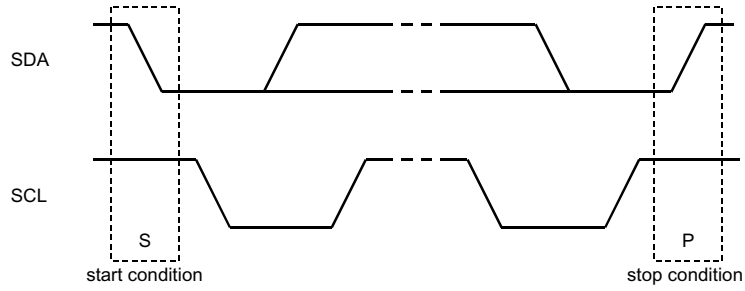


Figure 28. START and STOP conditions

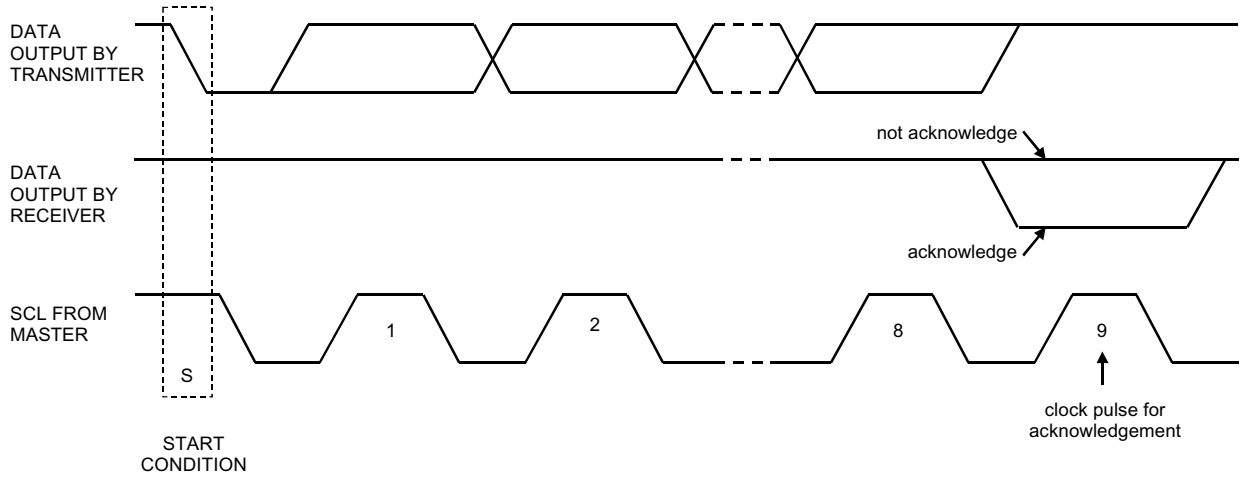


Figure 29. Acknowledge on the I<sup>2</sup>C-bus

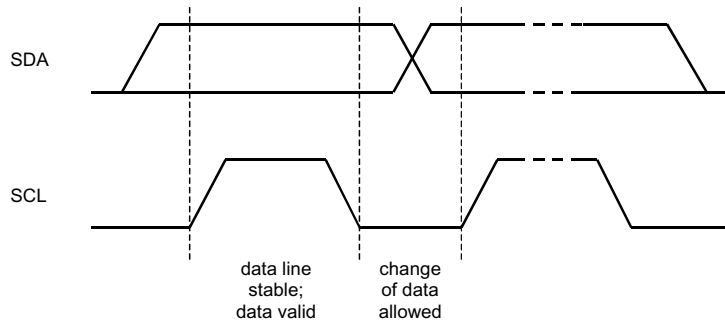


Figure 30. Bit transfer on the I<sup>2</sup>C-bus

### ■ Mapping of Program Registers

| Addr | Register Name            | D7    | D6     | D5    | D4     | D3    | D2    | D1    | D0     |
|------|--------------------------|-------|--------|-------|--------|-------|-------|-------|--------|
| 00H  | Power Down & Reset       | 0     | 0      | 0     | 0      | PWVRN | PWADN | PWDAN | RSTN   |
| 01H  | Path Control             | 0     | 0      | LOOP1 | LOOP0  | IPS1  | IPS0  | OPS1  | OPS0   |
| 02H  | Clock Mode Control       | 0     | CLKDIV | OCKS1 | OCKS0  | ICKS1 | ICKS0 | CM1   | CM0    |
| 03H  | Output Control           | 0     | SMUTE  | TXE   | BCU    | OVFE  | DZFM2 | DZFM1 | DZFM0  |
| 04H  | Receiver Control         | XFS96 | AFS96  | CS12  | EFH1   | EFH0  | DEAU  | DEM1  | DEM0   |
| 05H  | I/F Format & ATT Speed   | 0     | 0      | ATS1  | ATS0   | TDM   | DIF2  | DIF1  | DIF0   |
| 06H  | LOUT1 Volume Control     | ATT7  | ATT6   | ATT5  | ATT4   | ATT3  | ATT2  | ATT1  | ATT0   |
| 07H  | ROUT1 Volume Control     | ATT7  | ATT6   | ATT5  | ATT4   | ATT3  | ATT2  | ATT1  | ATT0   |
| 08H  | LOUT2 Volume Control     | ATT7  | ATT6   | ATT5  | ATT4   | ATT3  | ATT2  | ATT1  | ATT0   |
| 09H  | ROUT2 Volume Control     | ATT7  | ATT6   | ATT5  | ATT4   | ATT3  | ATT2  | ATT1  | ATT0   |
| 0AH  | LOUT3 Volume Control     | ATT7  | ATT6   | ATT5  | ATT4   | ATT3  | ATT2  | ATT1  | ATT0   |
| 0BH  | ROUT3 Volume Control     | ATT7  | ATT6   | ATT5  | ATT4   | ATT3  | ATT2  | ATT1  | ATT0   |
| 0CH  | INT0 Mask                | MRFS0 | MV0    | MSTC0 | MAUD0  | MDTS0 | MAUT0 | MPAR0 | MUNL0  |
| 0DH  | INT1 Mask                | MRFS1 | MV1    | MSTC1 | MAUD1  | MDTS1 | MAUT1 | MPAR1 | MUNL1  |
| 0EH  | Receiver Status 0        | RFS96 | V      | STC   | AUDION | DTSCD | AUTO  | PAR   | UNLOCK |
| 0FH  | Receiver Status 1        | 0     | 0      | 0     | 0      | 0     | PEM   | FS1   | FS0    |
| 10H  | Channel Status Byte 0    | C7    | C6     | C5    | C4     | C3    | C2    | C1    | C0     |
| 11H  | Channel Status Byte 1    | C15   | C14    | C13   | C12    | C11   | C10   | C9    | C8     |
| 12H  | Channel Status Byte 2    | C23   | C22    | C21   | C20    | C19   | C18   | C17   | C16    |
| 13H  | Channel Status Byte 3    | C31   | C30    | C29   | C28    | C27   | C26   | C25   | C24    |
| 14H  | Burst Preamble Pc Byte 0 | PC7   | DTSCD  | PC5   | PC4    | PC3   | PC2   | PC1   | PC0    |
| 15H  | Burst Preamble Pc Byte 1 | PC15  | PC14   | PC13  | PC12   | PC11  | PC10  | PC9   | PC8    |
| 16H  | Burst Preamble Pd Byte 0 | PD7   | PD6    | PD5   | PD4    | PD3   | PD2   | PD1   | PD0    |
| 17H  | Burst Preamble Pd Byte 1 | PD15  | PD14   | PD13  | PD12   | PD11  | PD10  | PD9   | PD8    |

Note: For addresses from 18H to 1FH, data is not written.

When PDN goes to “L”, the registers are initialized to their default values.

When RSTN bit goes to “0”, the internal timing is reset and DZF1-2 pins go to “H”, but registers are not initialized to their default values.

All data can be written to the register even if PWVRN, PWADN or PWDAN bit is “0”.

## ■ Register Definitions

| Addr | Register Name      | D7 | D6 | D5 | D4 | D3    | D2    | D1    | D0   |
|------|--------------------|----|----|----|----|-------|-------|-------|------|
| 00H  | Power Down & Reset | 0  | 0  | 0  | 0  | PWVRN | PWADN | PWDAN | RSTN |
|      | R/W                | RD | RD | RD | RD | R/W   | R/W   | R/W   | R/W  |
|      | Default            | 0  | 0  | 0  | 0  | 1     | 1     | 1     | 1    |

RSTN: Internal timing reset

0: Reset. DZF1-2 pins go to “H”, but registers are not initialized.

1: Normal operation

PWDAN: Power-down control of DAC1-3

0: Power-down

1: Normal operation

PWADN: Power-down control of ADC

0: Power-down

1: Normal operation

PWVRN: Power-down control of reference voltage

0: Power-down. ADC, DAC and PLL are powered-down.

1: Normal operation

| Addr | Register Name | D7 | D6 | D5    | D4    | D3   | D2   | D1   | D0   |
|------|---------------|----|----|-------|-------|------|------|------|------|
| 01H  | Path Control  | 0  | 0  | LOOP1 | LOOP0 | IPS1 | IPS0 | OPS1 | OPS0 |
|      | R/W           | RD | RD | R/W   | R/W   | R/W  | R/W  | R/W  | R/W  |
|      | Default       | 0  | 0  | 0     | 0     | 0    | 0    | 0    | 0    |

OPS1-0: Output Through Data Select (Table 12)

Default: “00”, RX1

IPS1-0: Input Recovery Data Select (Table 11)

Default: “00”, RX1

LOOP1-0: Loopback mode enable

00: Normal (No loop back)

01: LIN → LOUT1, LOUT2, LOUT3, LOUT4

RIN → ROUT1, ROUT2, ROUT3, ROUT4

The ADC digital output (RX data in the PLL mode) is connected to the digital DAC input. In this mode, the input DAC data to SDTI1-3 is ignored.

10: SDTI1(L) → SDTI2(L), SDTI3(L)

SDTI1(R) → SDTI2(R), SDTI3(R)

In this mode the input DAC data to SDTI2-3 is ignored.

11: N/A

LOOP1-0 should be set to “00” at TDM bit “1”.

| Addr | Register Name      | D7 | D6     | D5    | D4    | D3    | D2    | D1  | D0  |
|------|--------------------|----|--------|-------|-------|-------|-------|-----|-----|
| 02H  | Clock Mode Control | 0  | CLKDIV | OCKS1 | OCKS0 | ICKS1 | ICKS0 | CM1 | CM0 |
|      | R/W                | RD | R/W    | R/W   | R/W   | R/W   | R/W   | R/W | R/W |
|      | Default            | 0  | 0      | 0     | 0     | 0     | 0     | 0   | 0   |

CM1-0: Master Clock Operation Mode Select (Table 1)

Default: "00", mode 0

OCKS1-0: Master Clock Output Frequency Select at PLL mode (Table 2)

Default: "00", mode 0

ICKS1-0: Master Clock Input Frequency Select at X'tal mode (Table 4)

Default: "00", mode 0

CLKDIV: Master Clock Output Select at X'tal mode (Table 5)

0: Same frequency as crystal oscillator

1: Half frequency of crystal oscillator

| Addr | Register Name  | D7 | D6    | D5  | D4  | D3   | D2    | D1    | D0    |
|------|----------------|----|-------|-----|-----|------|-------|-------|-------|
| 03H  | Output Control | 0  | SMUTE | TXE | BCU | OVFE | DZFM2 | DZFM1 | DZFM0 |
|      | R/W            | RD | R/W   | R/W | R/W | R/W  | R/W   | R/W   | R/W   |
|      | Default        | 0  | 0     | 1   | 0   | 0    | 1     | 1     | 1     |

DZFM2-0: Zero detect mode select (Table 16)

Initial: “111”, disable

OVFE: Overflow detection enable

0: Disable, pin#20 becomes DZF2 pin.

1: Enable, pin#20 becomes OVF pin.

BCU: Block Start and C/U/V Output Mode

When BCU=1, the 4 output pins change another function.

DZF1 Pin → Block start signal

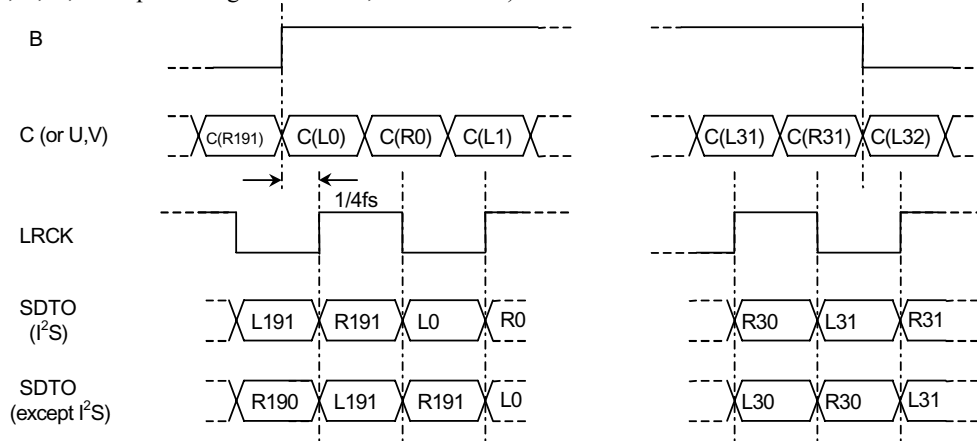
DZF2 Pin → C bit

INT1 Pin → U bit

TX Pin → V bit

The block signal goes high at the start of frame 0 and remains high until the end of frame 31.

(B, C, U, V output timing at RX mode, master mode)



TXE: TX Output Enable

0: Disable. TX output is “L”.

1: Enable

SMUTE: Soft Mute Enable (Figure 20)

0: Normal operation

1: All DAC outputs soft-muted

| Addr | Register Name    | D7    | D6    | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------------------|-------|-------|------|------|------|------|------|------|
| 04H  | Receiver Control | XFS96 | AFS96 | CS12 | EFH1 | EFH0 | DEAU | DEM1 | DEM0 |
|      | R/W              | R/W   | R/W   | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |
|      | Default          | 0     | 1     | 0    | 0    | 1    | 1    | 0    | 1    |

DEM1-0: De-emphasis Control (Table 9)

The setting of DEM1-0 bits is ignored at DEAU bit "1".

Default: "01", OFF

DEAU: De-emphasis Auto Detect Enable

0: Disable

1: Enable

EFH1-0: Interrupt 0 Pin Hold Count Select

00: 512 LRCK

01: 1024 LRCK (default)

10: 2048 LRCK

11: 4096 LRCK

CS12: Channel Status Select

0: Channel 1

1: Channel 2

Selects which channel status is used to derive C-bit buffers, AUDION, PEM, FS1 and FS0.

AFS96: Sampling Speed Mode Auto Setting Mode Enable (Table 3)

0: Disable, sampling mode is set by XFS96 bit.

1: Enable, sampling mode is automatically set by the register value of RFS96 bit at PLL mode.

XFS96: ADC and DAC Sampling Speed Mode Select (X'tal Mode or AFS96= "0", Table 3)

0: Normal speed mode

1: Double speed mode

The sampling speed mode is defined by RFS96 and the setting of XFS96 is ignored at AFS96 bit "1" in the PLL mode.

| Addr | Register Name          | D7 | D6 | D5   | D4   | D3  | D2   | D1   | D0   |
|------|------------------------|----|----|------|------|-----|------|------|------|
| 05H  | I/F Format & ATT Speed | 0  | 0  | ATS1 | ATS0 | TDM | DIF2 | DIF1 | DIF0 |
|      | R/W                    | RD | RD | R/W  | R/W  | R/W | R/W  | R/W  | R/W  |
|      | Default                | 0  | 0  | 0    | 0    | 0   | 1    | 0    | 0    |

DIF2-0: Audio Data Format Control (Table 14, Table 15)

Default: "100", mode 4

TDM: TDM Format Select

0: Normal format

1: TDM format

ATS1-0: Digital attenuator transition time setting (Table 18)

Default: "00", mode 0

| Addr    | Register Name        | D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|---------|----------------------|------|------|------|------|------|------|------|------|
| 06H     | LOUT1 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 07H     | ROUT1 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 08H     | LOUT2 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 09H     | ROUT2 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 0AH     | LOUT3 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 0BH     | ROUT3 Volume Control | ATT7 | ATT6 | ATT5 | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| R/W     |                      | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |
| Default |                      | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

ATT7-0: Attenuation Level (Table 17)  
 Default: all "0" (0dB)

| Addr | Register Name | D7    | D6  | D5    | D4    | D3    | D2    | D1    | D0    |
|------|---------------|-------|-----|-------|-------|-------|-------|-------|-------|
| 0CH  | INT0 Mask     | MRFS0 | MV0 | MSTC0 | MAUD0 | MDTS0 | MAUT0 | MPAR0 | MUNL0 |
|      | R/W           | R/W   | R/W | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
|      | Default       | 1     | 1   | 1     | 1     | 1     | 1     | 0     | 0     |

MULK0: Mask Enable for UNLOCK bit (Default: 0)

0: Mask disable 1: Mask enable

MPAR0: Mask Enable for PAR bit (Default: 0)

0: Mask disable 1: Mask enable

MAUT0: Mask Enable for AUTO bit (Default: 1)

0: Mask disable 1: Mask enable

MDTS0: Mask Enable for DTSCD bit (Default: 1)

0: Mask disable 1: Mask enable

MAUD0: Mask Enable for AUDIO bit (Default: 1)

0: Mask disable 1: Mask enable

MSTC0: Mask Enable for STC bit (Default: 1)

0: Mask disable 1: Mask enable

MV0: Mask Enable for V bit (Default: 1)

0: Mask disable 1: Mask enable

MRFS0: Mask Enable for RFS96 bit (Default: 1)

0: Mask disable 1: Mask enable

| Addr | Register Name | D7    | D6  | D5    | D4    | D3    | D2    | D1    | D0    |
|------|---------------|-------|-----|-------|-------|-------|-------|-------|-------|
| 0DH  | INT1 Mask     | MRFS1 | MV1 | MSTC1 | MAUD1 | MDTS1 | MAUT1 | MPAR1 | MUNL1 |
|      | R/W           | R/W   | R/W | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
|      | Default       | 1     | 0   | 1     | 0     | 0     | 0     | 1     | 1     |

MULK1: Mask Enable for UNLOCK bit (Default: 1)

0: Mask disable 1: Mask enable

MPAR1: Mask Enable for PAR bit (Default: 1)

0: Mask disable 1: Mask enable

MAUT1: Mask Enable for AUTO bit (Default: 0)

0: Mask disable 1: Mask enable

MDTS1: Mask Enable for DTSCD bit (Default: 0)

0: Mask disable 1: Mask enable

MAUD1: Mask Enable for AUDIO bit (Default: 0)

0: Mask disable 1: Mask enable

MSTC1: Mask Enable for STC bit (Default: 1)

0: Mask disable 1: Mask enable

MV1: Mask Enable for V bit (Default: 0)

0: Mask disable 1: Mask enable

MRFS1: Mask Enable for RFS96 bit (Default: 1)

0: Mask disable 1: Mask enable



| Addr    | Register Name         | D7              | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|---------|-----------------------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| 10H     | Channel Status Byte 0 | C7              | C6  | C5  | C4  | C3  | C2  | C1  | C0  |
| 11H     | Channel Status Byte 1 | C15             | C14 | C13 | C12 | C11 | C10 | C9  | C8  |
| 12H     | Channel Status Byte 2 | C23             | C22 | C21 | C20 | C19 | C18 | C17 | C16 |
| 13H     | Channel Status Byte 3 | C31             | C30 | C29 | C28 | C27 | C26 | C25 | C24 |
| R/W     |                       | RD              |     |     |     |     |     |     |     |
| Default |                       | Not initialized |     |     |     |     |     |     |     |

C31-0: Channel Status Byte 3-0

| Addr    | Register Name            | D7              | D6   | D5   | D4   | D3   | D2   | D1  | D0  |
|---------|--------------------------|-----------------|------|------|------|------|------|-----|-----|
| 14H     | Burst Preamble Pc Byte 0 | PC7             | PC6  | PC5  | PC4  | PC3  | PC2  | PC1 | PC0 |
| 15H     | Burst Preamble Pc Byte 1 | PC15            | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 |
| 16H     | Burst Preamble Pd Byte 0 | PD7             | PD6  | PD5  | PD4  | PD3  | PD2  | PD1 | PD0 |
| 17H     | Burst Preamble Pd Byte 1 | PD15            | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| R/W     |                          | RD              |      |      |      |      |      |     |     |
| Default |                          | Not initialized |      |      |      |      |      |     |     |

PC15-0: Burst Preamble Pc Byte 0 and 1

PD15-0: Burst Preamble Pd Byte 0 and 1

■ Burst Preambles in Non-PCM Bitstreams

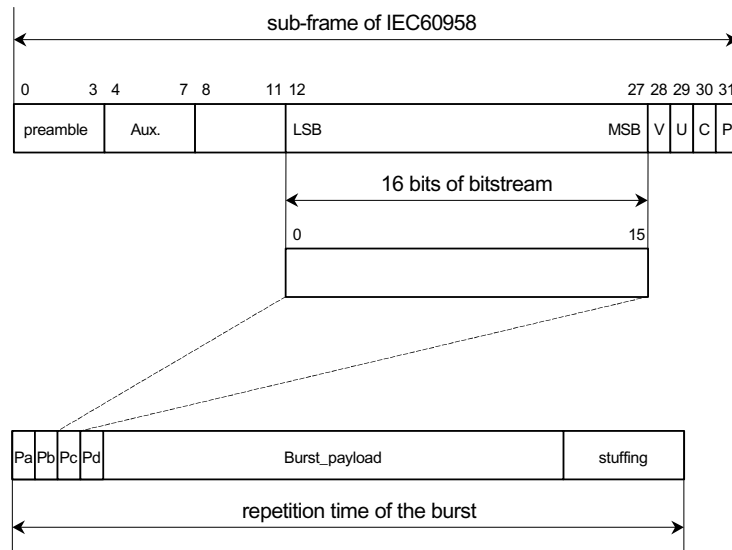


Figure 31. Data structure in IEC60958

| Preamble word | Length of field | Contents    | Value           |
|---------------|-----------------|-------------|-----------------|
| Pa            | 16 bits         | sync word 1 | 0xF872          |
| Pb            | 16 bits         | sync word 2 | 0x4E1F          |
| Pc            | 16 bits         | Burst info  | see Table 20    |
| Pd            | 16 bits         | Length code | numbers of bits |

Table 19. Burst preamble words

| Bits of Pc | Value                          | Contents  | Repetition time of burst in IEC60958 frames |
|------------|--------------------------------|---|---|
| 0-4        |                                | data type   |   |
|            | 0                              | NULL data   | ≤4096                                       |
|            | 1                              | Dolby AC-3 data   | 1536  |
|            | 2                              | reserved  |   |
|            | 3                              | PAUSE   |   |
|            | 4                              | MPEG-1 Layer1 data  | 384   |
|            | 5                              | MPEG-1 Layer2 or 3 data or MPEG-2 without extension             | 1152  |
|            | 6                              | MPEG-2 data with extension                                      | 1152  |
|            | 7                              | reserved  |   |
|            | 8                              | MPEG-2, Layer1 Low sample rate                                  | 384   |
|            | 9                              | MPEG-2, Layer2 or 3 Low sample rate                             | 1152  |
|            | 10                             | reserved  |   |
|            | 11                             | DTS type I  | 512   |
|            | 12                             | DTS type II   | 1024  |
|            | 13                             | DTS type III  | 2048  |
|            | 14                             | ATRAC   | 512   |
|            | 15                             | ATRAC2/3  | 1024  |
| 16-26      | reserved                       |   |   |
| 27         | (reserved for MPEG-4 AAC data) | 512   |   |
| 28         | MPEG-2 AAC data                | 1024  |   |
| 29-31      | reserved                       |   |   |
| 5, 6       | 0                              | reserved, shall be set to "0"                                   |   |
| 7          | 0                              | error-flag indicating a valid burst_payload                     |   |
|            | 1                              | error-flag indicating that the burst_payload may contain errors |   |
| 8-12       |                                | data type dependent info  |   |
| 13-15      | 0                              | bit stream number, shall be set to "0"                          |   |

Table 20. Fields of burst info Pc

■ Non-PCM Bitstream timing

1) When Non-PCM preamble is not coming within 4096 frames,

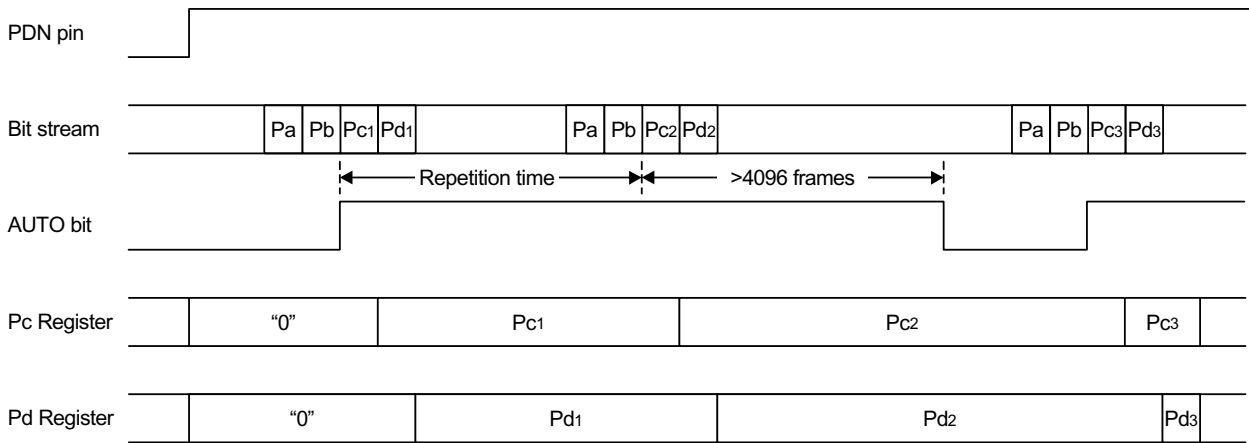


Figure 32. Timing example 1

2) When Non-PCM bitstream stops (when MULK0=0),

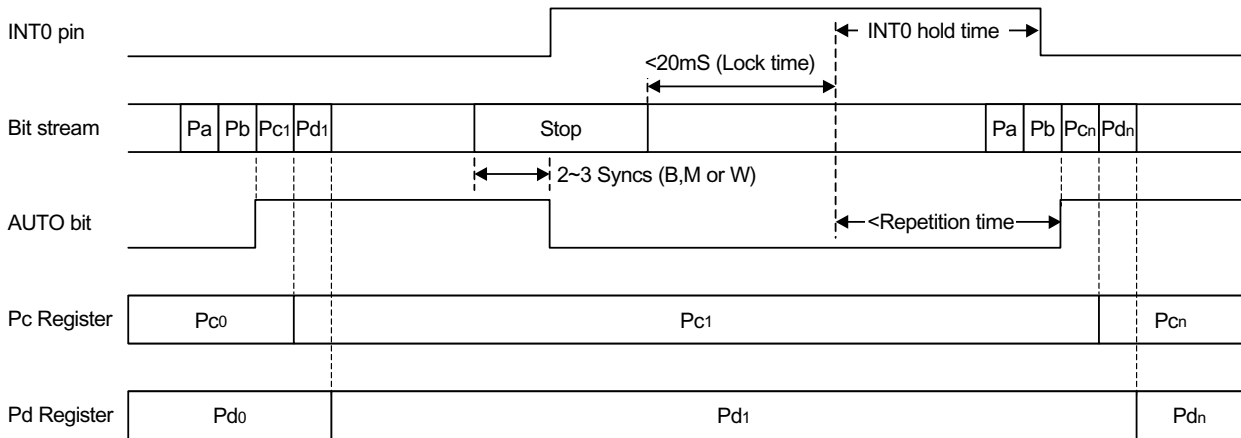


Figure 33. Timing example 2

**SYSTEM DESIGN**

Figure 34 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

Condition: TVDD=3.3V, Master mode, 4-wire serial control mode, DZFM2-0 = "100"

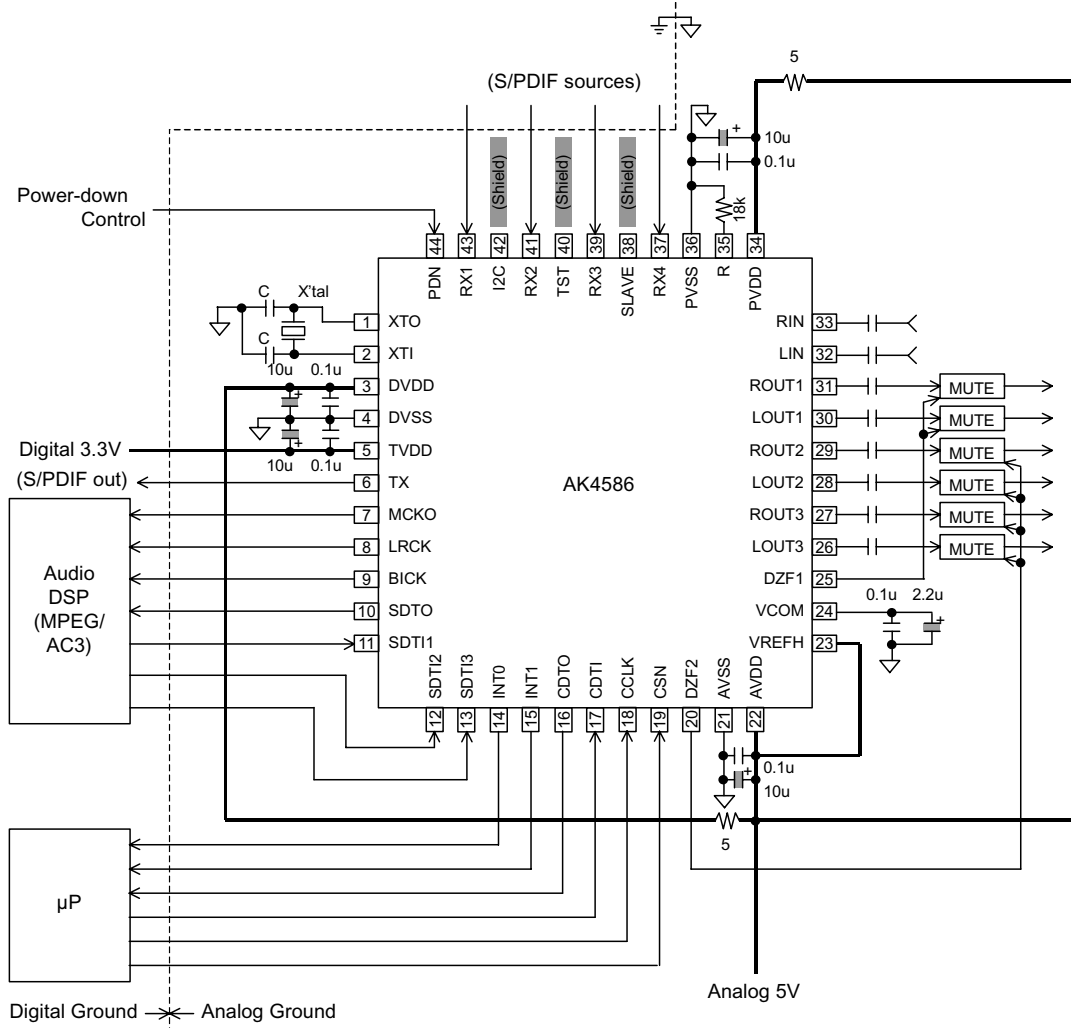


Figure 34. Typical Connection Diagram

Notes:

- "C" depends on the crystal.
- AVSS, DVSS and PVSS must be connected the same analog ground plane.
- Digital signals, especially clocks, should be kept away from the R pin in order to avoid an effect to the clock jitter performance.
- In case of coaxial input, ground of RCA connector and terminator should be connected to PVSS of the AK4586 with low impedance on PC board.

## 1. Grounding and Power Supply Decoupling

The AK4586 requires careful attention to power supply and grounding arrangements. AVDD, DVDD and PVDD are usually supplied from analog supply in system. Alternatively if AVDD, DVDD and PVDD are supplied separately, the power up sequence is not critical. **AVSS, DVSS and PVSS of the AK4586 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4586 as possible, with the small value ceramic capacitor being the nearest.

## 2. Voltage Reference Inputs

The voltage of VREFH sets the analog input/output range. VREFH pin is normally connected to AVDD with a 0.1 $\mu$ F ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 2.2 $\mu$ F parallel with a 0.1 $\mu$ F ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH and VCOM pins in order to avoid unwanted coupling into the AK4586.

## 3. Analog Inputs

ADC inputs are single-ended and internally biased to VCOM. The input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp (typ). The ADC output data format is 2's complement. The DC offset is removed by the internal HPF.

The AK4586 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK4586 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

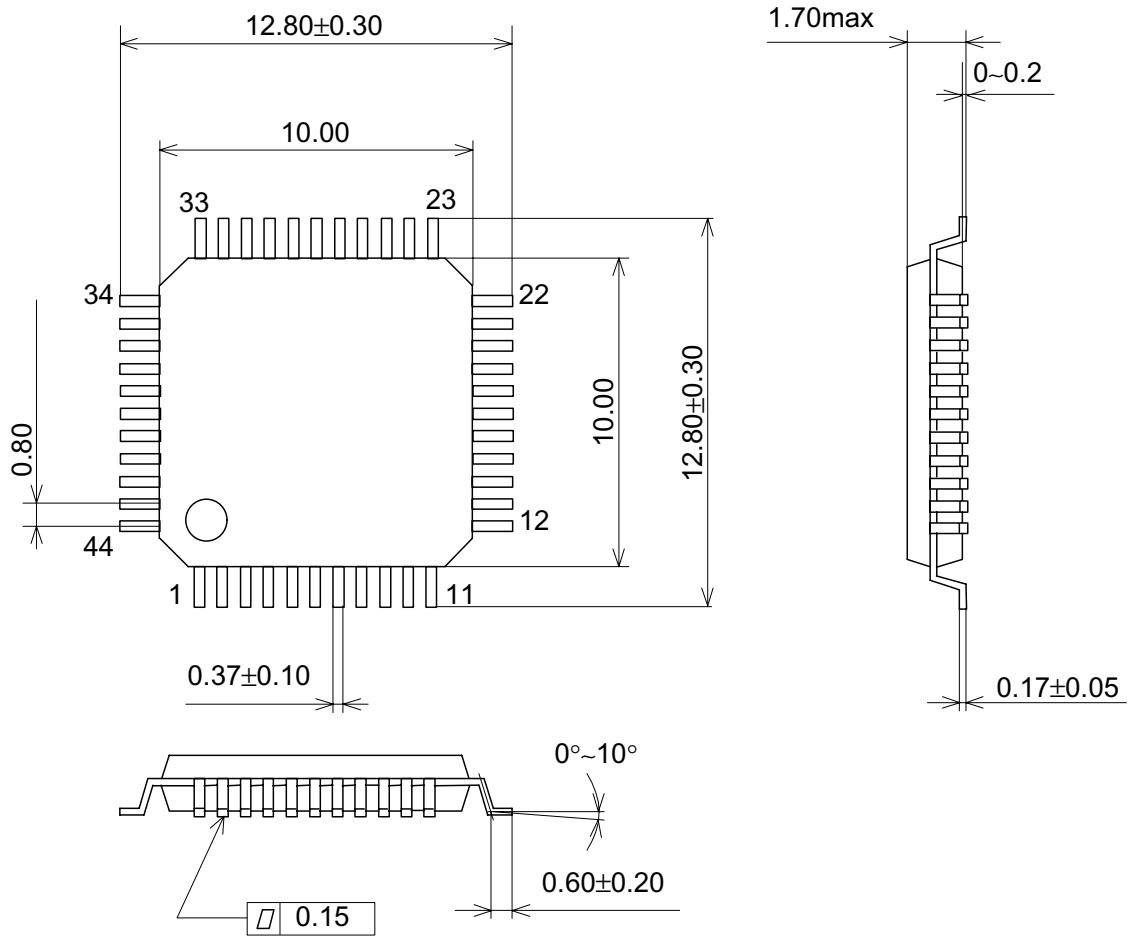
## 4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

PACKAGE

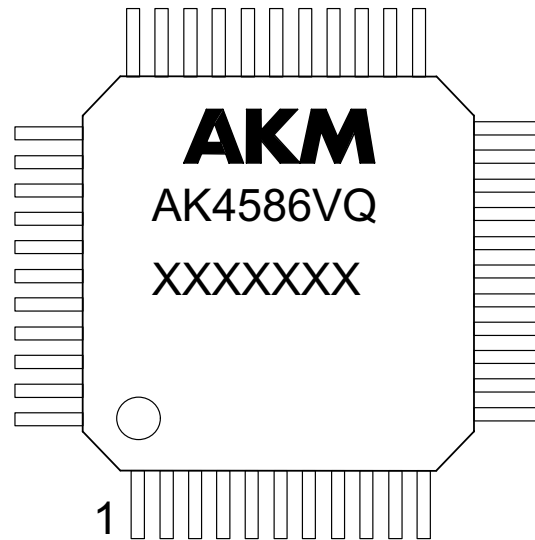
44pin LQFP (Unit: mm)



■ Package & Lead frame material

|                               |              |
|-------------------------------|--------------|
| Package molding compound:     | Epoxy        |
| Lead frame material:          | Cu           |
| Lead frame surface treatment: | Solder plate |

|                |
|----------------|
| <b>MARKING</b> |
|----------------|



- 1) Pin #1 indication
- 2) Date Code: XXXXXXX(7 digits)
- 3) Marking Code: AK4586VQ
- 4) Asahi Kasei Logo

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