AK4368EG
DAC with built-in PLL & HP-AMP

GENERAL DESCRIPTION

The AK4368 is 24-bit DAC with an integrated PLL and headphone amplifier. The PLL input frequency is synchronized to typical mobile phone clock frequencies. The AK4368 features an analog mixing circuit that allows easy interfacing in mobile phone and portable communication designs. The AK4368 includes a 3-D stereo enhancement circuit that operates with both the headphone amplifier and the stereo lineout. The integrated headphone amplifier features "pop-free" power-on/off, a mute control, and it delivers 50mW of power into 16Ω. The AK4368 is packaged in a 41-pin BGA package, deal for portable applications.

FEATURE

- **Multi-bit ΔΣ DAC**
- **Sampling Rate**
  - **8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz and 48kHz**
- **On chip perfect filtering 8 times FIR interpolator**
  - **Passband: 20kHz**
  - **Passband Ripple: ±0.02dB**
  - **Stopband Attenuation: 54dB**
- **Digital De-emphasis Filter: 32kHz, 44.1kHz and 48kHz**
- **PLL:**
  - **Input Frequency: 27MHz, 26MHz, 19.8MHz, 19.68MHz, 19.2MHz, 15.36MHz, 14.4MHz, 13MHz, 12MHz and 11.2896MHz**
  - **Input Level: AC Couple Input Available**
- **Audio I/F Format: MSB First, 2's Compliment**
  - **I^2S, 24bit MSB justified, 24bit/20bit/16bit LSB justified**
  - **Master/Slave Mode**
- **Mixing: LR, LL, RR, (L+R)/2**
- **Digital ALC**
- **Digital ATT**
- **Analog Mixing Circuit**
- **3D Stereo Enhancement**
- **Stereo Lineout**
- **μP Interface: 3-wire/I^2C**
- **Bass Boost Function**
- **Headphone Amplifier**
  - **Output Power: 50mW x 2ch @16Ω, 3.3V**
  - **S/N: 92dB@3.3V**
  - **Pop Noise Free at Power-ON/OFF and Mute**
- **Power Supply: 1.6V ~ 3.6V**
- **Power Supply Current: 4.0mA @2.4V (HP-AMP no output)**
- **Ta: –30 ~ 85°C**
- **Small Package: 41pin BGA (4mm x 4mm, 0.5mm pitch)**

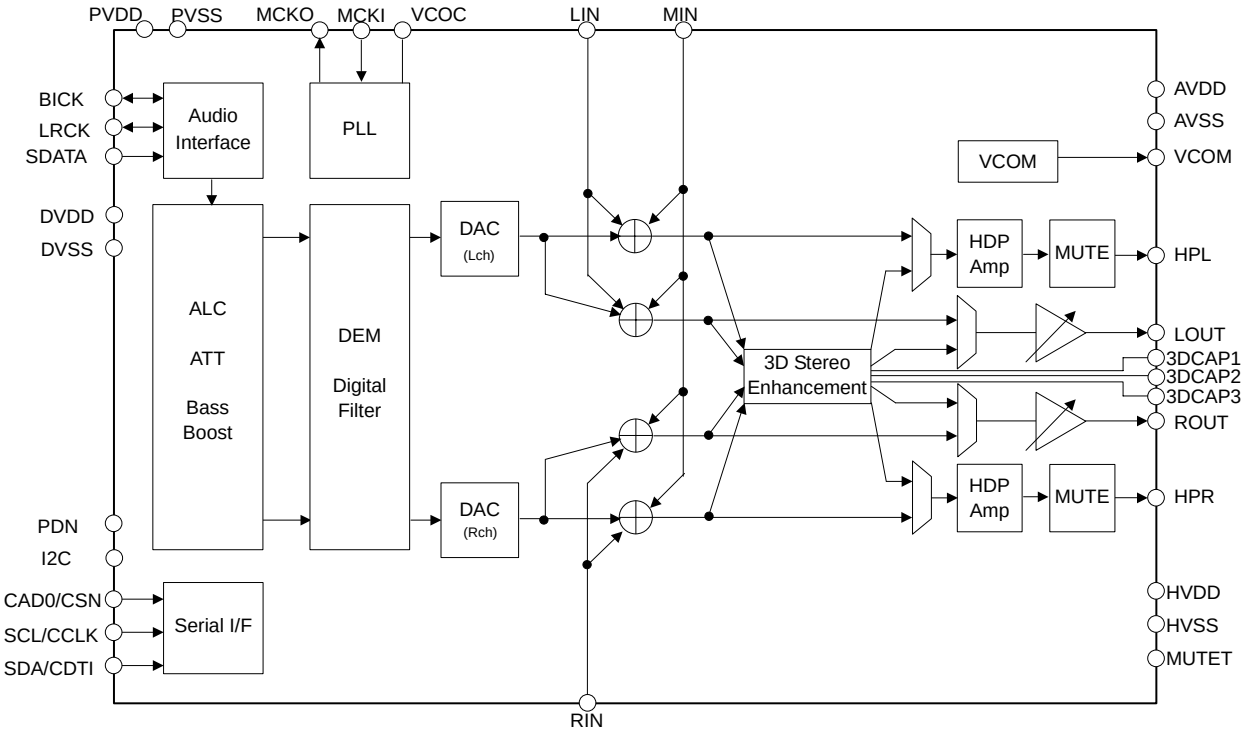
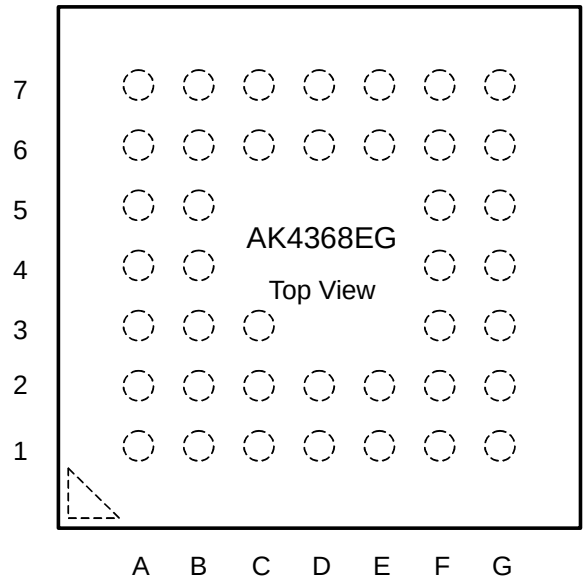


Figure 1. Block Diagram

■ Ordering Information

AK4368EG	–30 ~ +85°C	41pin BGA (0.5mm pitch)
AKD4368	Evaluation board for AK4368	

■ Pin Layout



7	NC	HPR	HVDD	AVDD	VCOM	LOUT	NC
6	HPL	HVSS	AVSS	MUTET	ROUT	3DCAP2	3DCAP3
5	MIN	NC	Top View			NC	3DCAP1
4	RIN	NC				PDN	NC
3	VCOC	LIN	NC			NC	CAD0/ CSN
2	PVDD	PVSS	DVSS	I2C	LRCK	SDATA	SCL/ CCLK
1	NC	MCKO	DVDD	MCKI	BICK	SDA/ CDTI	NC
	A	B	C	D	E	F	G

■ Comparison with AK4365 and AK4367

Parameter	AK4365	AK4367	AK4368
PLL Input Frequency	19.8/19.68/19.2/15.36/ 14.4/13/12/11.2896MHz	N/A	27/26/19.8/19.68/19.2/ 15.36/14.4/13/12/11.2896 MHz
Sampling Frequency at PLL mode	8/11.025/16/22.05/24/32/ 44.1/48kHz	N/A	8/11.025/12/16/22.05/24/3 2/44.1/48kHz
Audio I/F Format	20bit Right justified 16/20bit Left justified I^2S	24bit Right justified 16/20/24bit Left justified I^2S	←
Master mode	Available	N/A	Available
ALC	N/A	N/A	Available
3D Stereo Enhancement	N/A	N/A	Available
Line Output	Mono	Mono	Stereo
μP I/F	3-wire	3-wire/I^2C	←
Bass Boost	+6dB	+16dB	←
Mixing	(L+R)/2	(L+R)/2	LL, RR, (L+R)/2
HP-Amp Output Power	10mW	50mW	50mW
Power Supply Voltage	2.7 ~ 3.3V	2.2 ~ 3.6V	1.6 ~ 3.6V
Package	28QFN(5.2mm x 5.2mm)	20QFN(4.2mm x 4.2mm)	41BGA(4mm x 4mm)

PIN/FUNCTION

No.	Pin Name	I/O	Function
B1	MCKO	O	Master Clock Output
C2	DVSS	-	Digital Ground
C1	DVDD	-	Digital Power Supply
D2	I2C	I	Control Mode Select "H": I^2C Bus, "L": 3-wire Serial
D1	MCKI	I	Master Clock Input
E2	LRCK	I/O	L/R Clock This clock determines which audio channel is currently being input on SDATA pin.
E1	BICK	I/O	Serial Bit Clock This clock is used to latch audio data.
F2	SDATA	I	Audio Serial Data Input
F1	SDA	I/O	Control Data Input/Output (I2C pin = "H")
	CDTI	I	Control Data Input (I2C pin = "L")
G2	SCL	I	Control Data Clock (I2C pin = "H")
	CCLK	I	Control Data Clock (I2C pin = "L")
G3	CAD0	I	Chip Address 0 Select (I2C pin = "H")
	CSN	I	Control Data Chip Select (I2C pin = "L")
F4	PDN	I	Power-down & Reset When "L", the AK4368 is in power-down mode and is held in reset. The AK4368 should always be reset upon power-up.
G5	3DCAP1	O	Capacitor Connect Pin 1 for 3D Stereo Enhancement Connected to 3DCAP2 pin with 4.7nF capacitor in series.
F6	3DCAP2	O	Capacitor Connect Pin 2 for 3D Stereo Enhancement Connected to 3DCAP1 pin with 4.7nF capacitor in series and connected to 3DCAP3 pin with 470nF capacitor in series.
G6	3DCAP3	O	Capacitor Connect Pin 1 for 3D Stereo Enhancement Connected to 3DCAP2 pin with 470nF capacitor in series.
F7	LOUT	O	Lch Analog Output
E6	ROUT	O	Rch Analog Output
E7	VCOM	O	Common Voltage Output Normally connected to AVSS pin with a 2.2μF electrolytic capacitor.
D7	AVDD	-	Analog Power Supply
C6	AVSS	-	Analog Ground
D6	MUTET	O	Mute Time Constant Control Connected to AVSS pin with a capacitor for mute time constant.
C7	HVDD	-	Power Supply Pin for Headphone Amp
B6	HVSS	-	Ground for Headphone Amp
B7	HPR	O	Rch Headphone Amp Output
A6	HPL	O	Lch Headphone Amp Output
A5	MIN	I	Mono Analog Input
A4	RIN	I	Rch Analog Input
B3	LIN	I	Lch Analog Input
A3	VCOC	O	Output for Loop Filter of PLL Circuit This pin should be connected to AVSS with one resistor and one capacitor in series.
B2	PVSS	-	Ground for PLL. Connected to AVSS.
A2	PVDD	-	Power Supply for PLL. Normally connected to AVDD.

No.	Pin Name	I/O	Function
A1 A7 B4 B5 C3 F3 F5 G1 G4 G7	NC	-	No Connect Pin No internal bonding. These pins should be connected to ground or open.

Note: All digital input pins (I2C, SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCKI, PDN) must not be left floating.
Note: MCKI pin can be left floating only when PDN pin = "L".

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LOUT, ROUT, MUTET, HPR, HPL, MIN, RIN, LIN	These pins should be open.
Digital	CAD0	This pin should be connected to DVSS.
	MCKO	This pin should be open.

ABSOLUATE MAXIMUM RATING

(AVSS, DVSS, HVSS, PVSS=0V; Note 1)

Parameter		Symbol	Min	max	Units
Power Supplies	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	PLL	PVDD	–0.3	4.6	V
	HP-Amp	HVDD	–0.3	4.6	V
	|AVSS – DVSS| (Note 2)	ΔGND1	-	0.3	V
	|AVSS – HVSS| (Note 2)	ΔGND2	-	0.3	V
	|AVSS – PVSS| (Note 2)	ΔGND3	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	–0.3	AVDD+0.3 or 4.6	V
Digital Input Voltage (Note 4)		VIND	–0.3	DVDD+0.3 or 4.6	V
Ambient Temperature		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS, HVSS and PVSS must be connected to the same analog ground plane.
Note 3. MIN, LIN and RIN pins.
Note 4. SDA/CDTI, SCL/CCLK, CAD0/CSN, SDATA, LRCK, BICK, MCKI, PDN and I2C pins.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(AVSS, DVSS, HVSS, PVSS=0V; Note 1)

Parameter		Symbol	min	typ	Max	Units
Power Supplies	Analog	AVDD	1.6	2.4	3.6	V
	Digital	DVDD	1.6	2.4	AVDD	V
	PLL	PVDD	1.6	2.4	3.6	V
	HP-Amp	HVDD	1.6	2.4	3.6	V
	Difference1	AVDD–PVDD	–0.3	0	+0.3	V
	Difference2	AVDD–HVDD	–0.3	0	+0.3	V

Note 1. All voltages with respect to ground.

* AKM assumes no responsibility for usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=PVDD=DVDD=HVDD=2.4V, AVSS=PVSS=DVSS=HVSS=0V; fs=44.1kHz; EXT mode; BOOST OFF; Slave Mode; Signal Frequency =1kHz; Measurement band width=20Hz ~ 20kHz; Headphone-Amp: Load impedance is a serial connection with R_L =16Ω and C_L=220μF. (Refer to Figure 48); unless otherwise specified)

Parameter			min	typ	Max	Units
DAC Resolution			-	-	24	bit
Headphone-Amp: (HPL/HPR pins) (Note 5)						
Analog Output Characteristics						
THD+N		–3dBFS Output, 2.4V, Po=10mW@16Ω	-	–50	–40	dB
		–4.8dBFS Output, 3.3V, Po=50mW@16Ω HPG bit="1"	-	–20	-	dB
D-Range		–60dBFS Output, A-weighted	82	90	-	dB
		–60dBFS Output, A-weighted, 3.3V	-	92	-	dB
S/N		A-weighted, 2.4V	82	90	-	dB
		A-weighted, 3.3V	-	92	-	dB
Interchannel Isolation			60	80	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.3	0.5	dB
Gain Drift			-	200	-	ppm/°C
Load Resistance (Note 6)			16	-	-	Ω
Load Capacitance			-	-	300	pF
Output Voltage		–3dBFS Output (Note 7)	1.01	1.13	1.25	Vpp
		–4.8dBFS Output, 3.3V, Po=50mW@16Ω HPG bit="1"	-	0.89	-	Vrms
Stereo Line Output: (LOUT/ROUT pins, R_L=10kΩ) (Note 8)						
Analog Output Characteristics:						
THD+N		0dBFS Output	-	–60	–50	dB
S/N		A-weighted	80	87	-	dB
DC Accuracy						
Gain Drift			-	200	-	ppm/°C
Load Resistance (Note 6)			10	-	-	kΩ
Load Capacitance			-	-	25	pF
Output Voltage		0dBFS Output (Note 9)	1.32	1.47	1.61	Vpp
Output Volume: (LOUT/ROUT pins)						
Step Size			1	2	3	dB
Gain Control Range			–30	-	0	dB

Note 5. DACHL=DACHR bits = "1", MINHL=MINHR=LINHL=RINHR bits = "0".
Note 6. AC load.
Note 7. Output voltage is proportional to AVDD voltage. Vout = 0.47 x AVDD(typ)@–3dBFS.
Note 8. DACL=DACR bits = "1", MINL=MINR=LINL=RINR bits = "0".
Note 9. Output voltage is proportional to AVDD voltage. Vout = 0.61 x AVDD(typ)@0dBFS.

Parameter	min	typ	max	Units
LINEIN: (LIN/RIN/MIN pins)				
Analog Input Characteristics				
Input Resistance (See Figure 23, Figure 24.)				
LIN pin				
LINHL bit = "1", LINL bit = "1"	35	50	-	kΩ
LINHL bit = "1", LINL bit = "0"	-	100	-	kΩ
LINHL bit = "0", LINL bit = "1"	-	100	-	kΩ
RIN pin				
RINHR bit = "1", RINR bit = "1"	35	50	-	kΩ
RINHR bit = "1", RINR bit = "0"	-	100	-	kΩ
RINHR bit = "0", RINR bit = "1"	-	100	-	kΩ
MIN pin				
MINHL=MINHR=MINL=MINR bits = "1"	17	25	-	kΩ
MINHL bit = "1", MINHR=MINL=MINR bits = "0"	-	100	-	kΩ
MINHR bit = "1", MINHL=MINL=MINR bits = "0"	-	100	-	kΩ
MINL bit = "1", MINHL=MINHR=MINR bits = "0"	-	100	-	kΩ
MINR bit = "1", MINHL=MINHR=MINL bits = "0"	-	100	-	kΩ
Gain				
LIN/MIN→LOUT, RIN/MIN→ROUT	–1	0	+1	dB
LIN/MIN→HPL, RIN/MIN→HPR	–0.24	+0.76	+1.76	dB
Power Supplies				
Power Supply Current				
Normal Operation (PDN pin = "H") (Note 10)				
AVDD+PVDD+DVDD	-	3.8	5.5	mA
HVDD	-	1.2	2.5	mA
Power-Down Mode (PDN pin = "L") (Note 11)	-	1	100	μA

Note 10. PMDAC=PMHPL=PMHPR=PMLO bits = "1", MUTEN bit = "1", MCKO bit = "0" and HP-Amp output is off. When PMDAC=PMHPL=PMHPR bits = "1" and PMLO bit= "0", total power supply current (AVDD+PVDD+DVDD+HVDD) is 4.0mA.

Note 11. All digital input pins including clock pins (MCKI, BICK and LRCK) are held at DVSS.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PVDD, HVDD=1.6 ~ 3.6V; fs=44.1kHz; De-emphasis = "OFF")

Parameter			Symbol	min	typ	max	Units
DAC Digital Filter: (Note 12)							
Passband (Note 13)		–0.05dB	PB	0	-	20.0	kHz
		–6.0dB		-	22.05	-	kHz
Stopband (Note 13)			SB	24.1	-	-	kHz
Passband Ripple			PR	-	-	±0.02	dB
Stopband Attenuation			SA	54	-	-	dB
Group Delay (Note 14)			GD	-	22	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	μs
DAC Digital Filter + Analog Filter: (Note 12) (Note 15)							
Frequency Response	0 ~ 20.0kHz		FR	-	±0.5	-	dB
Analog Filter: (Note 16)							
Frequency Response	0 ~ 20.0kHz		FR	-	±1.0	-	dB
BOOST Filter: (Note 15) (Note 17)							
Frequency Response	MIN	20Hz	FR	-	5.76	-	dB
		100Hz		-	2.92	-	dB
		1kHz		-	0.02	-	dB
	MID	20Hz	FR	-	10.80	-	dB
		100Hz		-	6.84	-	dB
		1kHz		-	0.13	-	dB
	MAX	20Hz	FR	-	16.06	-	dB
		100Hz		-	10.54	-	dB
		1kHz		-	0.37	-	dB

Note 12. BOOST OFF (BST1-0 bit = "00")

Note 13. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.05dB), SB=0.546*fs(@–54dB).

Note 14. This is the calculated delay time caused by digital filtering. This time is measured from the setting of the 24bit data of both channels to the input registers to the output of the analog signal.

Note 15. DAC → HPL, HPR, LOUT, ROUT

Note 16. MIN → HPL/HPR/LOUT/ROUT, LIN → HPL/LOUT, RIN → HPR/ROUT

Note 17. These frequency responses scale with fs. If high-level signal is input, the output clips at low frequency.

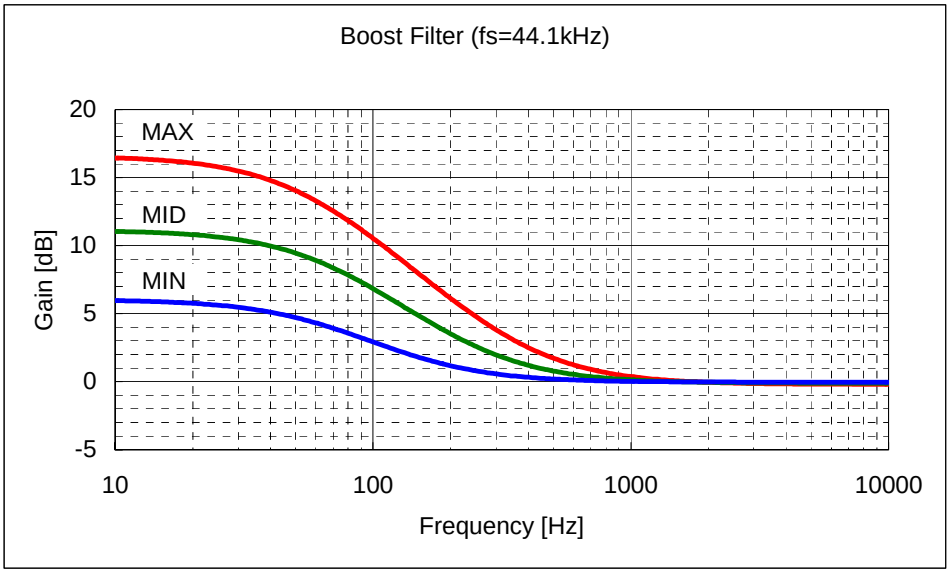


Figure 2. Boost Frequency (fs=44.1kHz)

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PVDD, HVDD=1.6 ~ 3.6V)

Parameter		Symbol	Min	typ	max	Units
High-Level Input Voltage	2.2V≤DVDD≤3.6V	VIH	70%DVDD	-	-	V
	1.6V≤DVDD<2.2V	VIH	80%DVDD	-	-	V
Low-Level Input Voltage	2.2V≤DVDD≤3.6V	VIL	-	-	30%DVDD	V
	1.6V≤DVDD<2.2V	VIL	-	-	20%DVDD	V
Input Voltage at AC Coupling (Note 18)		VAC	0.4	-	-	Vpp
High-Level Output Voltage (Iout=−200μA)		VOH	DVDD−0.2	-	-	V
Low-Level Output Voltage						
(Except SDA pin: Iout=200μA)		VOL	-	-	0.2	V
(SDA pin: Iout=3mA)		VOL	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	μA

Note 18. Only MCKI pin. (Figure 48)

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, PVDD, HVDD=1.6 ~ 3.6V; CL = 20pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
Master Clock Input Timing					
Frequency (PLL mode)	fCLK	11.2896	-	27	MHz
(EXT mode)	fCLK	2.048	-	12.288	MHz
Pulse Width Low (Note 19)	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High (Note 19)	tCLKH	0.4/fCLK	-	-	ns
AC Pulse Width (Note 20)	tACW	18.5	-	-	ns
LRCK Timing					
Frequency	fs	8	44.1	48	kHz
Duty Cycle: Slave Mode	Duty	45	-	55	%
Master Mode	Duty	-	50	-	%
MCKO Output Timing (PLL mode)					
Frequency	fCLKO	0.256	-	12.288	MHz
Duty Cycle (Except fs=32kHz, PS1-0= "00")	dMCK	40	-	60	%
(fs=32kHz, PS1-0= "00")	dMCK	-	33	-	%
Serial Interface Timing (Note 21)					
Slave Mode (M/S bit = "0"):					
BICK Period	tBCK	312.5	-	-	ns
BICK Pulse Width Low	tBCKL	100	-	-	ns
Pulse Width High	tBCKH	100	-	-	ns
LRCK Edge to BICK "↑" (Note 22)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 22)	tBLR	50	-	-	ns
SDATA Hold Time	tSDH	50	-	-	ns
SDATA Setup Time	tSDS	50	-	-	ns
Master Mode (M/S bit = "1"):					
BICK Frequency (BF bit = "1")	fBCK	-	64fs	-	Hz
(BF bit = "0")	fBCK	-	32fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–50	-	50	ns
SDATA Hold Time	tSDH	50	-	-	ns
SDATA Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↑" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns

Note 19. Except AC coupling.

Note 20. Pulse width to ground level when MCKI is connected to a capacitor in series and a resistor is connected to ground. (Refer to Figure 3.)

Note 21. Refer to "Serial Data Interface".

Note 22. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus mode): (Note 23)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-		μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 24)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 25)	tPD	150	-	-	ns

Note 23. I^2C is a registered trademark of Philips Semiconductors.
Note 24. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 25. The AK4368 can be reset by bringing PDN pin = “L” to “H” only upon power up.

■ Timing Diagram

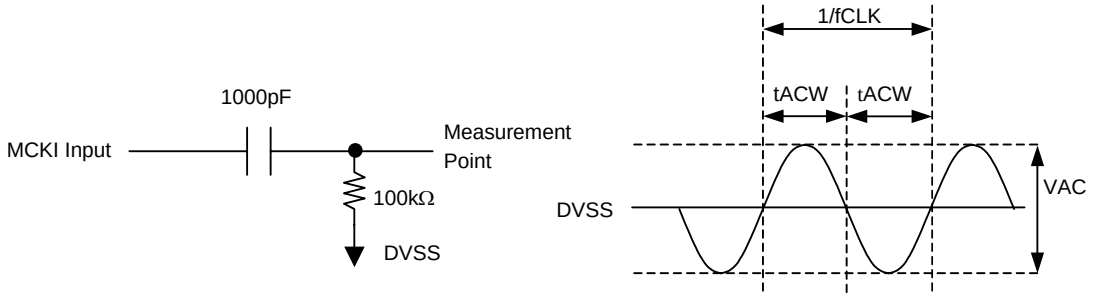


Figure 3. MCKI AC Coupling Timing

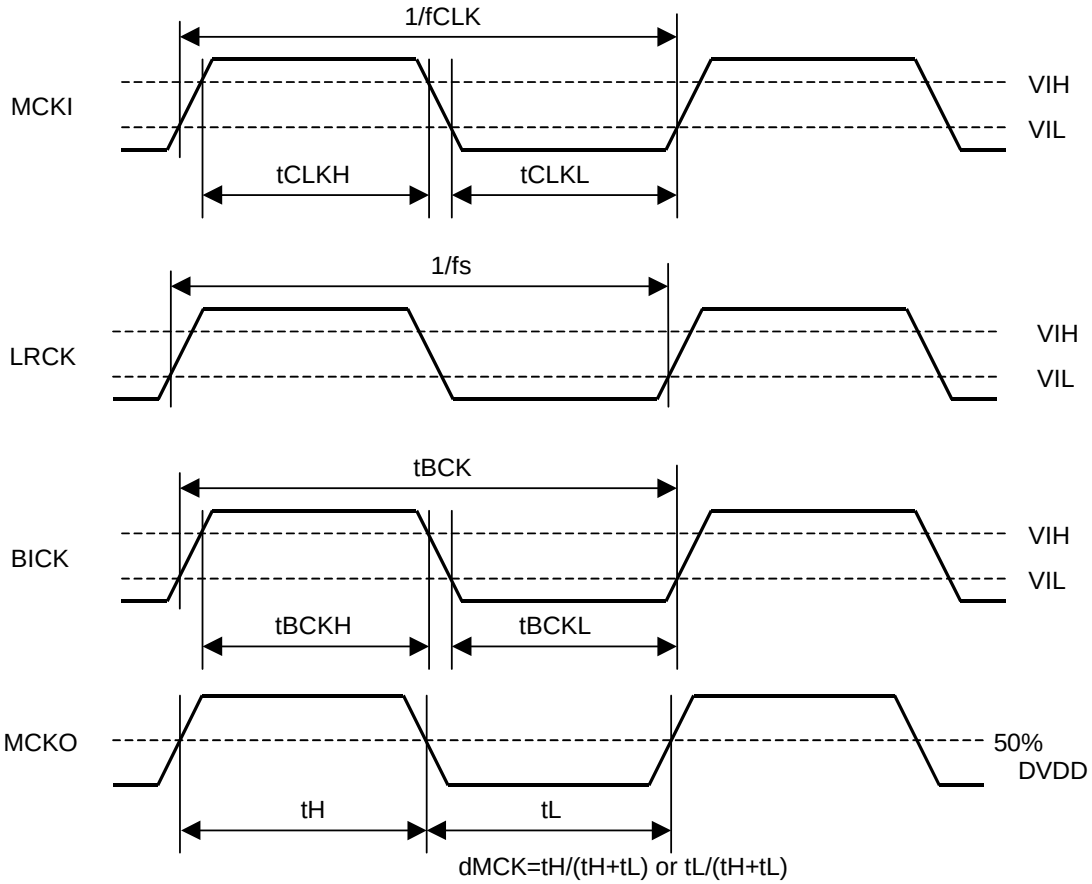


Figure 4. Clock Timing

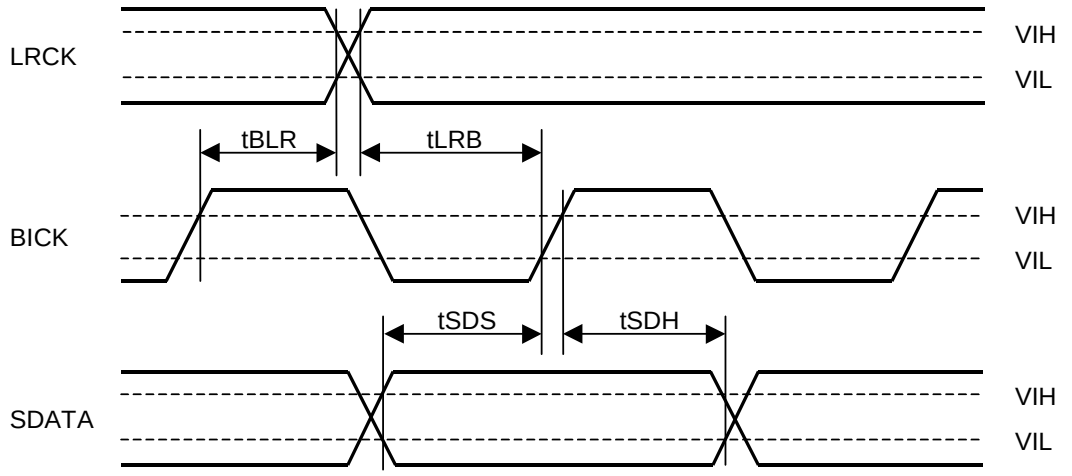


Figure 5. Serial Interface Timing (Slave Mode)

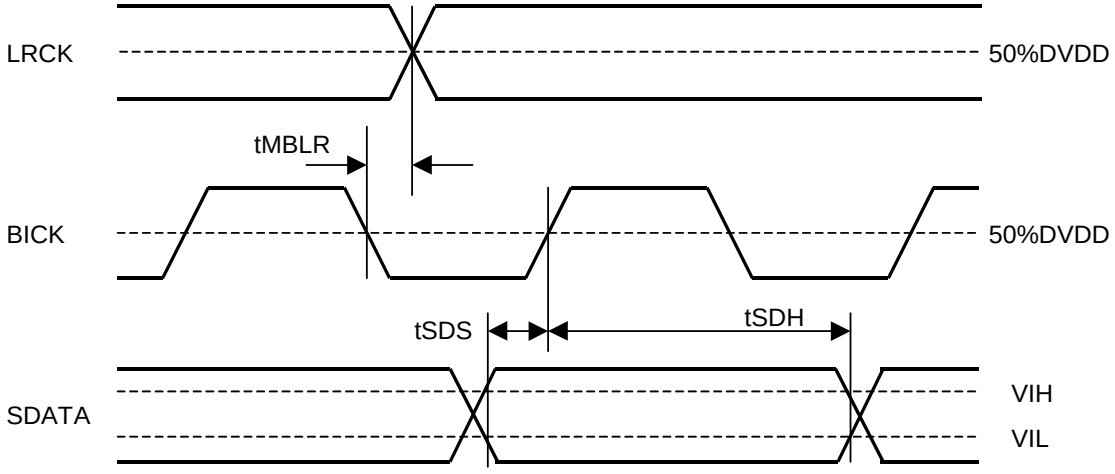


Figure 6. Serial Interface Timing (Master mode)

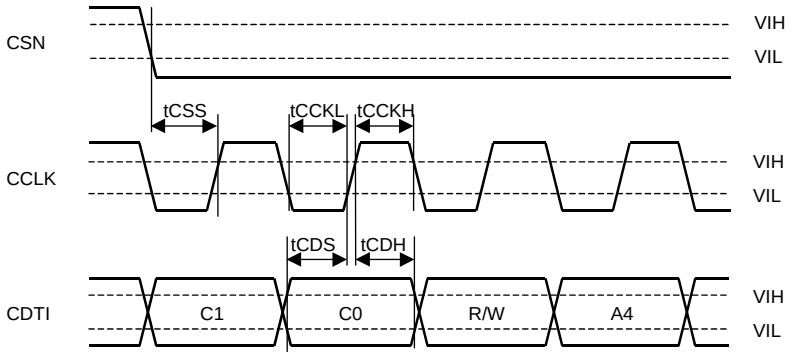


Figure 7. WRITE Command Input Timing

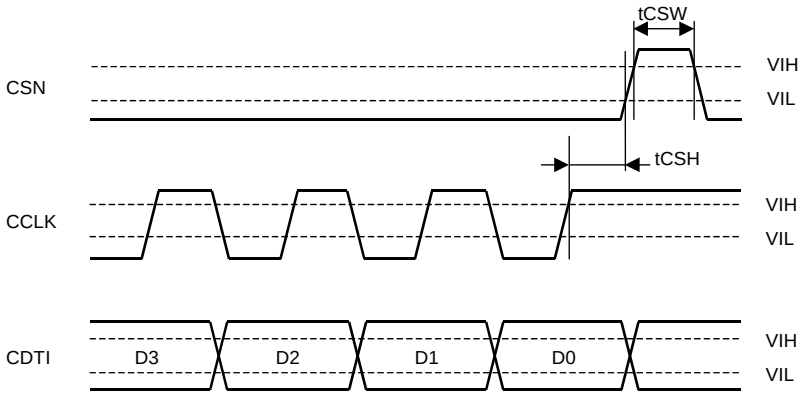


Figure 8. WRITE Data Input Timing

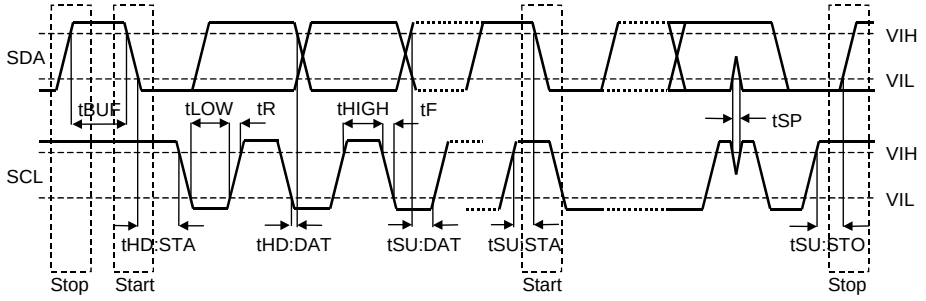


Figure 9. I^2C Bus Mode Timing

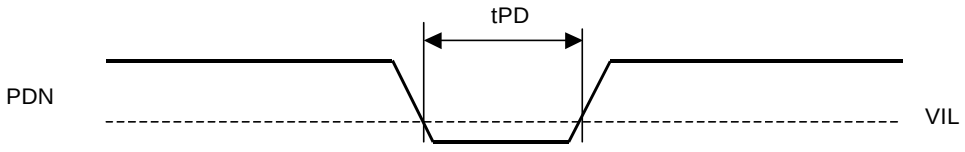


Figure 10. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

1) PLL mode (PMPLL bit = "1")

A fully integrated analog phase locked loop (PLL) generates a clock that is selected by PLL3-0 and FS3-0 bits (refer to Table 1 and Table 2). MCKO output frequency can be controlled by PS1-0 bits (Table 3). MCKO output can be enabled by controlling the MCKO bit. The PLL lock time is referred to Table 1. When changing the sampling frequency during normal operation (PMDAC bit = "1"), the change should occur after the input is muted by SMUTE bit = "1", or the input is set to "0" data.

The M/S bit selects either master or slave mode. When the M/S bit = "1" master mode is selected and "0" selects slave mode. When the AK4368 is in power-down mode (PDN pin = "L") and then exits the reset state, the AK4368 is in slave mode. After exiting the reset state, the AK4368 goes to master mode by changing the M/S bit to "1".

In master mode, when an external clock (11.2896MHz, 12MHz, 13MHz, 14.4MHz, 15.36MHz, 19.2MHz, 19.68MHz, 19.8MHz, 26MHz, 27MHz) is input to MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit (Figure 11).

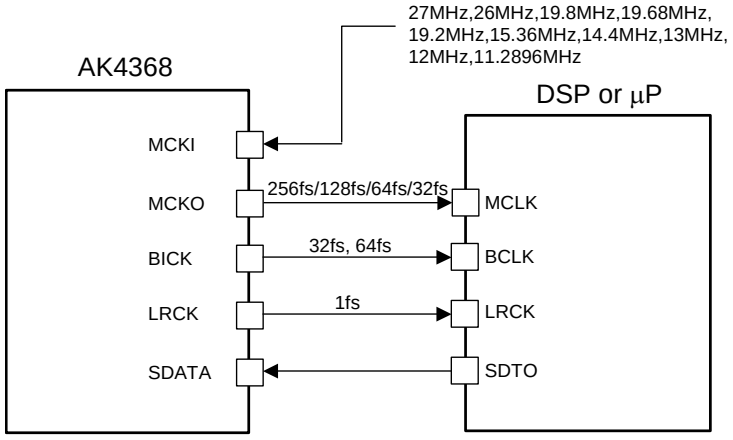


Figure 11. PLL Master Mode

When the AK4368 is used in the master mode, LRCK and BICK pins are in a floating state until the M/S bit becomes "1". LRCK and BICK pins of the AK4368 should be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

In master mode (M/S bits = "1"), LRCK and BICK pins output "L" before the PLL is locked by setting PMPLL = PMDAC bits = "0" → "1". At that time, MCKO pin outputs an abnormal frequency clock at MCKO bit = "1". When MCKO bit = "0", MCKO pin outputs "L". After the PLL is locked, LRCK and BICK start to output the clocks (Table 4).

In slave mode, a reference clock of PLL is selected among the input clocks to BICK or LRCK pin. The required clock to the AK4368 is generated by an internal PLL circuit. BICK and LRCK inputs should be synchronized with MCKO output (Figure 12).

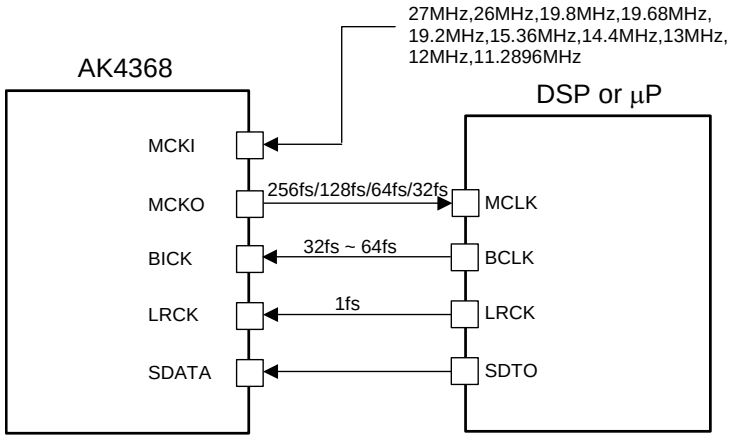


Figure 12. PLL Slave Mode

In slave mode (M/S bit = "0"), the MCKO pin outputs an abnormal frequency clock when the MCKO bit = "1" before the PLL is locked by setting PMPLL = PMDAC bits = "0" → "1". After the PLL is locked, the MCKO pin outputs the clock selected by Table 3. LRCK input should be synchronized with MCKI or MCKO in slave mode. LRCK and BICK should always be present whenever the AK4368 is in normal operation mode (PMDAC bit = "1"). If these clocks are not provided, the AK4368 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the AK4368 should be placed in power-down mode (PMDAC bit = "0").

Mode	PLL3	PLL2	PLL1	PLL0	MCKI	fs (Note 26)	R and C of VCOC pin		PLL Lock Time (typ)	
							R[Ω]	C[F]		
0	0	0	0	0	11.2896MHz	44.1, 48	10k	22n	20ms	Default
1	0	0	0	1	14.4MHz	44.1, 48	10k	22n	20ms	
2	0	0	1	0	12MHz	44.1, 48	10k	47n	20ms	
3	0	0	1	1	19.2MHz	44.1, 48	10k	22n	20ms	
4	0	1	0	0	15.36MHz	44.1, 48	10k	22n	20ms	
5	0	1	0	1	13MHz	44.1, 48	15k	330n	100ms	
6	0	1	1	0	19.68MHz	44.1, 48	10k	47n	20ms	
7	0	1	1	1	19.8MHz	44.1, 48	10k	47n	20ms	
8	1	0	0	0	26MHz	44.1, 48	15k	330n	100ms	
9	1	0	0	1	27MHz	44.1, 48	10k	47n	20ms	
10	1	0	1	0	13MHz	44.0995 48.0007	10k	22n	20ms	
11	1	0	1	1	26MHz	44.0995 48.0007	10k	22n	20ms	
12	1	1	0	0	19.8MHz	44.0995 47.9992	10k	22n	20ms	
13	1	1	0	1	27MHz	44.0995 47.9997	10k	22n	20ms	
14-15	Others				N/A	N/A	N/A	N/A	-	

Note 26. Type 1-4 frequency is indicated in Table 2.
Table 1. MCKI Input Frequency (PLL mode)

Mode	FS3	FS2	FS1	FS0	fs				
					Type 1	Type 2	Type 3	Type 4	
0	0	0	0	0	48kHz	48.0007kHz	47.9992kHz	47.9997kHz	
1	0	0	0	1	24kHz	24.0004kHz	23.9996kHz	23.9999kHz	
2	0	0	1	0	12kHz	12.0002kHz	11.9998kHz	11.9999kHz	
4	0	1	0	0	32kHz	32.0005kHz	31.9994kHz	31.9998kHz	
5	0	1	0	1	16kHz	16.0002kHz	15.9997kHz	15.9999kHz	
6	0	1	1	0	8kHz	8.0001kHz	7.9999kHz	7.9999kHz	
8	1	0	0	0	44.1kHz	44.0995kHz	44.0995kHz	44.0995kHz	Default
9	1	0	0	1	22.05kHz	22.0498kHz	22.0498kHz	22.0498kHz	
10	1	0	1	0	11.025kHz	11.0249kHz	11.0249kHz	11.0249kHz	
3, 7, 11-15	Others				N/A	N/A	N/A	N/A	

Table 2. Sampling Frequency (PLL mode)

PS1	PS0	MCKO	
0	0	256fs	Default
0	1	128fs	
1	0	64fs	
1	1	32fs	

Table 3. MCKO frequency (PLL mode, MCKO bit = “1”)

	Master Mode (M/S bit = “1”)		
	Power Up (PMDAC bit= PMPLL bit= “1”)	Power Down (PMDAC bit= PMPLL bit= “0”)	PLL Unlock
MCKI pin	Refer to Note 26. Type 1-4 frequency is indicated in Table 2. Table 1.	Input or fixed to “L” or “H”	Refer to Note 26. Type 1-4 frequency is indicated in Table 2. Table 1.
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”	MCKO bit = “0”: “L” MCKO bit = “1”: Unsettling
BICK pin	BF bit = “1”: 64fs output BF bit = “0”: 32fs output	“L”	“L”
LRCK pin	Output	“L”	“L”

Table 4. Clock Operation in Master mode (PLL mode)

	Slave Mode (M/S bit = “0”)		
	Power Up (PMDAC bit= PMPLL bit= “1”)	Power Down (PMDAC bit= PMPLL bit= “0”)	PLL Unlock
MCKI pin	Refer to Note 26. Type 1-4 frequency is indicated in Table 2. Table 1.	Input or fixed to “L” or “H”	Refer to Note 26. Type 1-4 frequency is indicated in Table 2. Table 1.
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”	MCKO bit = “0”: “L” MCKO bit = “1”: Unsettling
BICK pin	Input	Fixed to “L” or “H” externally	Input or Fixed to “L” or “H” externally
LRCK pin	Input	Fixed to “L” or “H” externally	Input or Fixed to “L” or “H” externally

Table 5. Clock Operation in Slave mode (PLL mode)

2) EXT mode (PMPLL bit = “0”: Default)

The AK4368 can be placed in external clock mode (EXT mode) by setting the PMPLL bit to “0”. In EXT mode, the master clock can directly input to the DAC via the MCKI pin without going through the PLL. In this case, the sampling frequency and MCKI frequency can be selected by FS3-0 bits (refer to Table 6). In EXT mode, PLL3-0 bits are ignored. MCKO output is enabled by controlling the MCKO bit. MCKO output frequency can be controlled by PS1-0 bits. If the sampling frequency is changed during normal operation of the DAC (PMDAC bit = “1”), the change should occur after the input is muted by SMUTE bit = “1”, or the input is set to “0” data.

LRCK and BICK are output from the AK4368 in master mode(Figure 13). The clock input to the MCKI pin should always be present whenever the DAC is in normal operation (PMDAC bit = “1”). If these clocks are not provided, the AK4368 may draw excessive current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PMDAC bit = “0”).

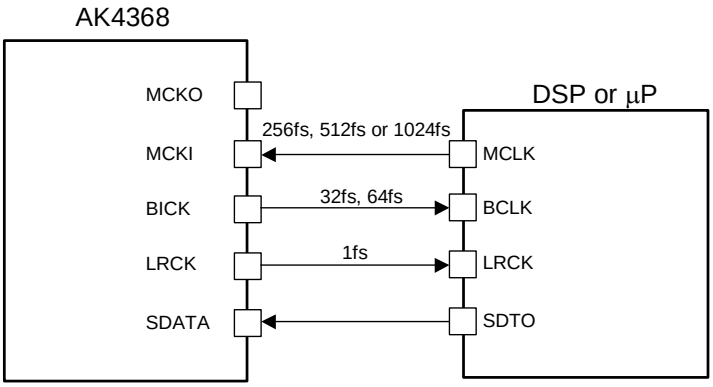


Figure 13. EXT Master Mode

The external clocks required to operate the AK4368 in slave mode are MCKI, LRCK and BICK(Figure 14). The master clock (MCKI) should be synchronized with the sampling clock (LRCK). The phase between these clocks does not matter. All external clocks (MCKI, BICK and LRCK) should always be present whenever the DAC is in normal operation mode (PMDAC bit = “1”). If these clocks are not provided, the AK4368 may draw excessive current and will not operate properly, because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PMDAC bit = “0”).

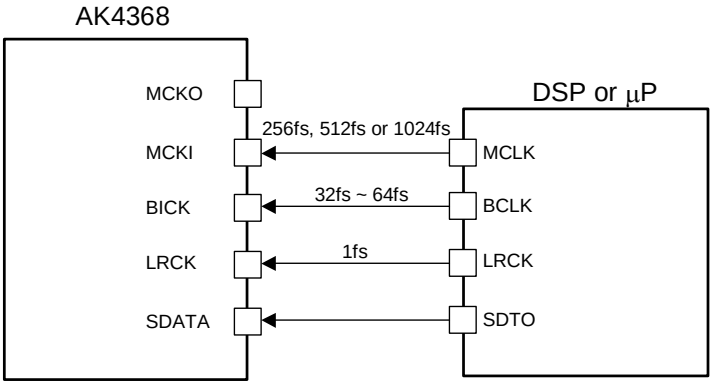


Figure 14. EXT Slave Mode

Mode	FS3	FS2	FS1	FS0	fs	MCKI	
0	0	0	0	0	8kHz ~ 48kHz	256fs	
1	0	0	0	1	8kHz ~ 24kHz	512fs	
2	0	0	1	0	8kHz ~ 12kHz	1024fs	
4	0	1	0	0	8kHz ~ 48kHz	256fs	
5	0	1	0	1	8kHz ~ 24kHz	512fs	
6	0	1	1	0	8kHz ~ 12kHz	1024fs	
8	1	0	0	0	8kHz ~ 48kHz	256fs	Default
9	1	0	0	1	8kHz ~ 24kHz	512fs	
10	1	0	1	0	8kHz ~ 12kHz	1024fs	
3, 7, 11-15	Others				N/A	N/A	

Table 6. Relationship between Sampling Frequency and MCKI Frequency (EXT mode)

PS1	PS0	MCKO	
0	0	256fs	Default
0	1	128fs	
1	0	64fs	
1	1	32fs	

Table 7. MCKO frequency (EXT mode, MCKO bit = “1”)

	Master Mode (M/S bit = “1”)	
	Power Up (PMDAC bit = “1”)	Power Down (PMDAC bit = “0”)
MCKI pin	Refer to Table 6.	Input or fixed to “L” or “H”
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”
BICK pin	BF bit = “1”: 64fs output BF bit = “0”: 32fs output	“L”
LRCK pin	Output	“L”

Table 8. Clock Operation in Master mode (EXT mode)

	Slave Mode (M/S bit = “0”)	
	Power Up (PMDAC bit = “1”)	Power Down (PMDAC bit = “0”)
MCKI pin	Refer to Table 6.	Input or fixed to “L” or “H”
MCKO pin	MCKO bit = “0”: “L” MCKO bit = “1”: Output	“L”
BICK pin	Input	Fixed to “L” or “H” externally
LRCK pin	Input	Fixed to “L” or “H” externally

Table 9. Clock Operation in Slave mode (EXT mode)

For low sampling rates, DR and S/N degrade because of the out-of-band noise. DR and S/N are improved by using higher frequency for MCKI. Table 10 shows DR and S/N when the DAC output is to the HP-amp.

MCKI	DR, S/N (BW=20kHz, A-weight)	
	fs=8kHz	fs=16kHz
256fs	56dB	75dB
512fs	75dB	90dB
1024fs	90dB	N/A

Table 10. Relationship between MCKI frequency and DR (and S/N) of HP-amp (2.4V)

■ Serial Data Interface

The AK4368 interfaces with external systems via the SDATA, BICK and LRCK pins. Five data formats are available, selected by setting the DIF2, DIF1 and DIF0 bits (Table 11). Mode 0 is compatible with existing 16-bit DACs and digital filters. Mode 1 is a 20-bit version of Mode 0. Mode 4 is a 24-bit version of Mode 0. Mode 2 is similar to AKM ADCs and many DSP serial ports. Mode 3 is compatible with the I^2S serial data protocol. In Modes 2 and 3 with BICK≥48fs, the following formats are also valid: 16-bit data followed by eight zeros (17th to 24th bits) and 20-bit data followed by four zeros (21st to 24th bits). In all modes, the serial data is MSB first and 2's complement format.

When master mode and BICK=32fs(BF bit = "0"), the AK4368 cannot be set to Mode 1 or Mode 2.

Mode	DIF2	DIF1	DIF0	Format	BICK	Figure	
0	0	0	0	0: 16bit, LSB justified	32fs ≤ BICK ≤ 64fs	Figure 15	
1	0	0	1	1: 20bit, LSB justified	40fs ≤ BICK ≤ 64fs	Figure 16	
2	0	1	0	2: 24bit, MSB justified	48fs ≤ BICK ≤ 64fs	Figure 17	Default
3	0	1	1	3: I^2S Compatible	BICK=32fs or 48fs ≤ BICK ≤ 64fs	Figure 18	
4	1	0	0	4: 24bit, LSB justified	48fs ≤ BICK ≤ 64fs	Figure 16	

Table 11. Audio Data Format

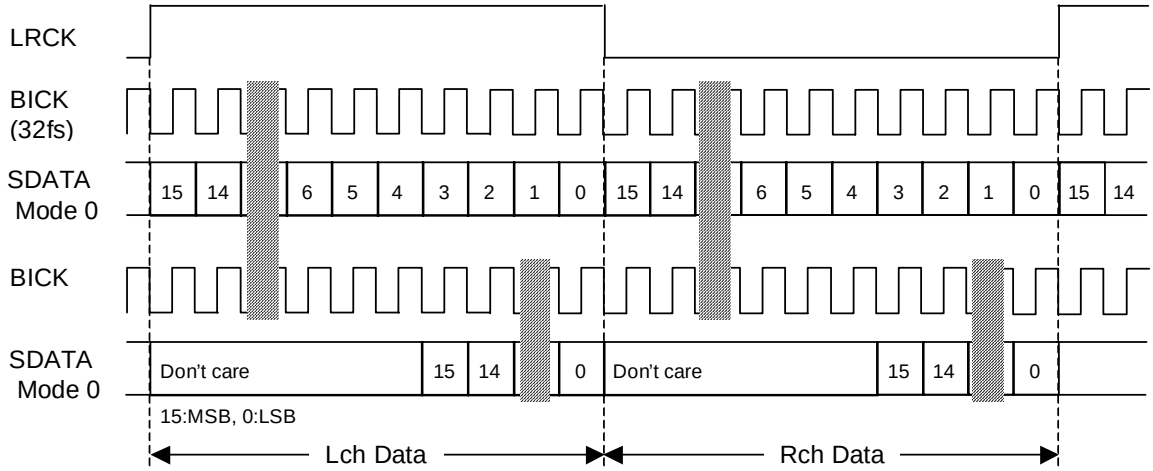


Figure 15. Mode 0 Timing (LRP = BCKP bits = "0")

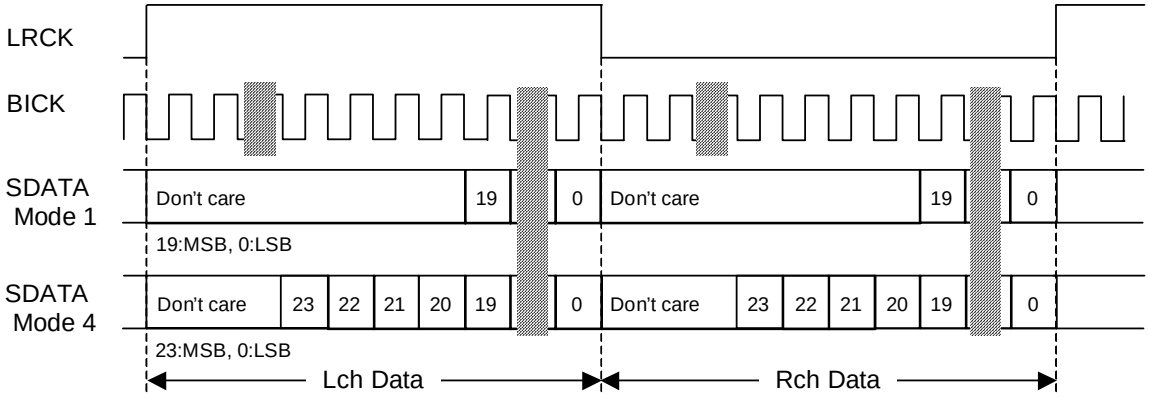


Figure 16. Mode 1, 4 Timing (LRP = BCKP bits = "0")

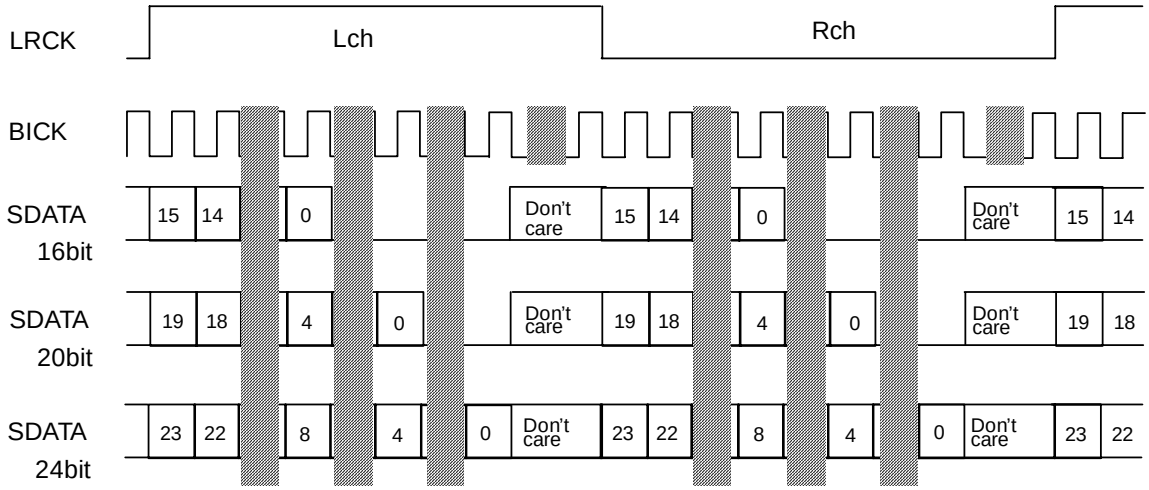


Figure 17. Mode 2 Timing (LRP = BCKP bits = "0")

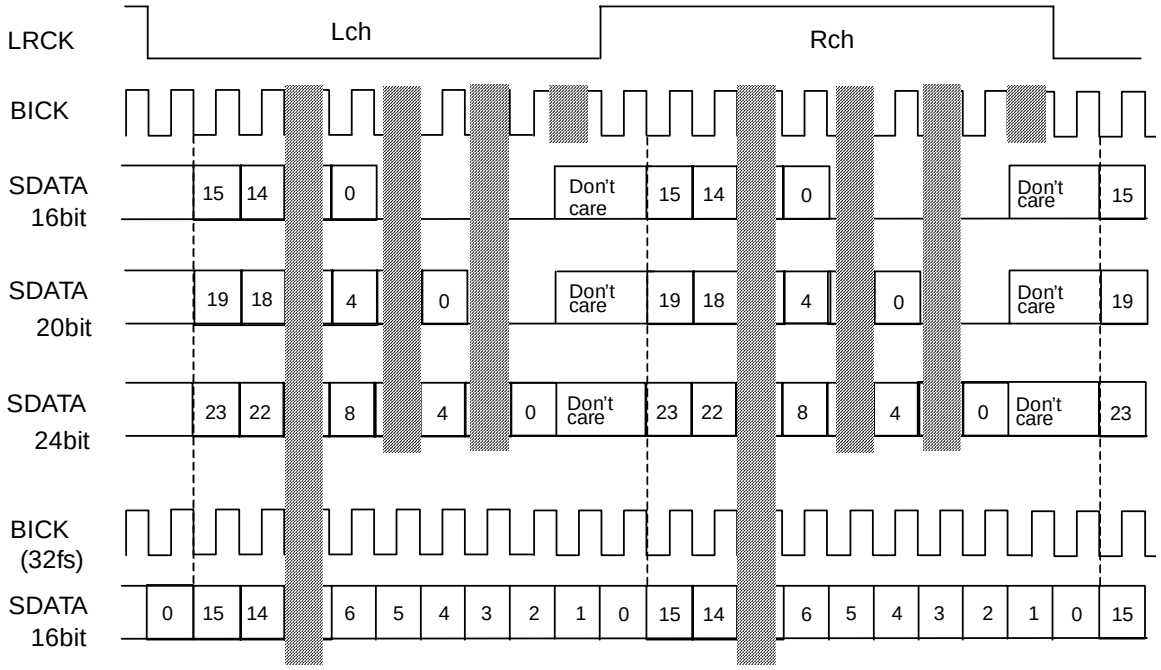


Figure 18. Mode 3 Timing (LRP = BCKP bits = "0")

■ ALC Operation

The ALC (Automatic Level Control) is controlled by the ALC block when ALC bit is "1". When ALC bit = "0", the gain of ALC block is fixed to 0dB.

[1] ALC Limiter Operation

During ALC limiter operation, when either the left or right channel exceeds the ALC limiter detection level (–6.0dBFS), the volume of both channel (same value) are attenuated automatically by the amount defined by the ALC limiter ATT step (LMAT1-0 bits, Table 13). The volume is changed by the ALC limiter operation at the individual zero crossing points of the left and right channels, or at the zero crossing timeout. ROTM1-0 bits set the zero crossing timeout period of both the ALC limiter and recovery operation (Table 12). Then the volume is set to the same value for both channels.

ROTM1	ROTM0		ALC Recovery Operation Waiting Period, Zero Crossing Timeout Period						
			fs=16kHz	fs=22.05kHz	fs=24kHz	fs=32kHz	fs=44.1kHz	fs=48kHz	
0	0	1024/fs	64ms	46ms	43ms	32ms	23ms	21ms	
0	1	2048/fs	128ms	93ms	85ms	64ms	46ms	43ms	Default
1	0	4096/fs	256ms	186ms	171ms	128ms	93ms	85ms	
1	1	Reserved	-	-	-	-	-	-	

Table 12. ALC Recovery Operation Waiting Period, Zero Crossing Timeout Period

LMAT1	LMAT0	ALC Limiter ATT Step				
		ALC Output ≥ –6.0dBFS	ALC Output ≥ 0dBFS	ALC Output ≥ +6dBFS	ALC Output ≥ +12dBFS	
0	0	1	1	1	1	Default
0	1	2	2	2	2	
1	0	2	2	4	4	
1	1	2	4	4	8	

Table 13. ALC Limiter ATT Step

[2] ALC Recovery Operation

The ALC recovery operation waits for the ROTM1-0 bits (Table 12) to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (−8.5dBFS) during the wait time, the ALC recovery operation is executed. The volume is automatically incremented by the RATT bit (Table 14) up to the set reference level (REF7-0 bits, Table 15), with zero crossing detection with a timeout period set by the ROTM1-0 bits (Table 12). Then the volume is set to the same level for both channels. The ALC recovery operation is executed at a period set by the ROTM1-0 bits. When a zero cross is detected for both channels during the wait period set by the ROTM1-0 bits, the ALC recovery operation waits until ROTM1-0 period and the next recovery operation is executed.

During ALC recovery operation or recovery waiting, the ALC limiter operation immediately starts if either channel exceeds the ALC limiter detection level (−6.0dBFS).

When
"ALC recovery waiting counter reset level (−8.5dBFS) ≤ Output Signal < ALC limiter detection level (−6.0dBFS)" during the ALC recovery operation, the wait timer of the ALC recovery operation is reset. When
the "ALC recovery waiting counter reset level (−8.5dBFS) > Output Signal",
the wait timer of the ALC recovery operation starts.

The ALC operation corresponds to impulse noise. When impulse noise is input, the ALC recovery operation executes faster than a normal recovery operation.

RATT	GAIN STEP	
0	1	Default
1	2	

Table 14. ALC Recovery GAIN Step

REF7-0	GAIN(dB)	
FFH : C2H	Reserved	
C1H	+18.0	
C0H	+17.625	
BFH	+17.25	
:	:	
92H	+0.375	
91H	0	Default
90H	−0.375	
:	:	
73H	−11.25	
72H	−11.625	
71H	−12.0	
70H : 00H	Reserved	

Table 15. Reference Level for ALC Recovery operation

[3] Example of ALC Operation

Register Name	Comment	fs=16kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
ROTM1-0	Zero crossing timeout period	00	64ms	01	46ms
REF7-0	Maximum gain at recovery operation	C1H	+18dB	C1H	+18dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
RATT	Recovery GAIN step	0	1 step	0	1 step
ALC	ALC enable	1	Enable	1	Enable

Table 16. Example of the ALC setting

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC bit = "0" or PMDAC bits = "0".

- **LMAT1-0, ROTM1-0, RATT, REF7-0**

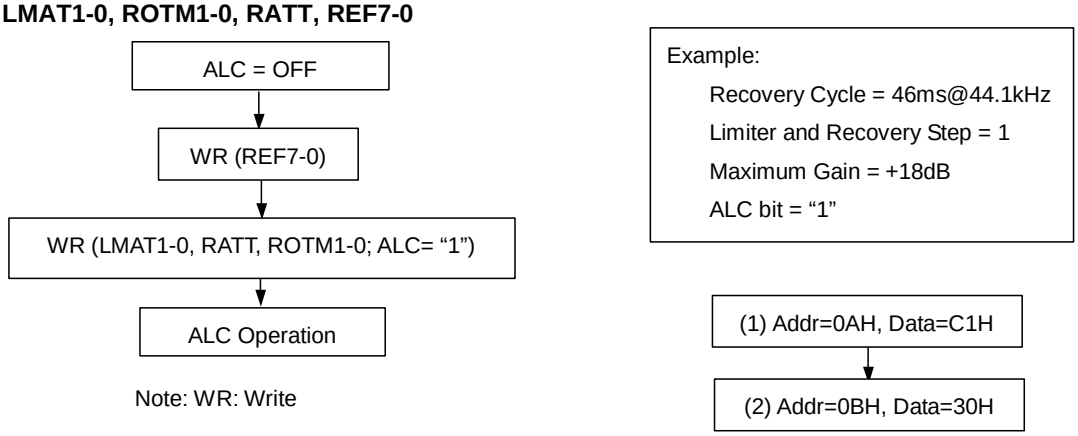


Figure 19. Registers set-up sequence at ALC operation

■ Digital Attenuator

The AK4368 has a channel-independent digital attenuator (256 levels, 0.5dB step). This digital attenuator is placed before the D/A converter. ATTL/R7-0 bits set the attenuation level (0dB to −127dB or MUTE) for each channel (Table 17). At DATTC bit = "1", ATTL7-0 bits control both channel's attenuation levels. At DATTC bit = "0", ATTL7-0 bits control the left channel level and ATTR7-0 bits control the right channel level.

ATTL7-0 ATTR7-0	Attenuation	
FFH	0dB	
FEH	–0.5dB	
FDH	–1.0dB	
FCH	–1.5dB	
:	:	
:	:	
02H	–126.5dB	
01H	–127.0dB	
00H	MUTE (–∞)	Default

Table 17. Digital Volume ATT values

The ATS bit sets the transition time between set values of ATT7-0 bits as either 1061/fs or 7424/fs (Table 18). When the ATS bit = "0", a soft transition between the set values occurs(1062 levels). It takes 1061/fs (24ms@fs=44.1kHz) from FFH(0dB) to 00H(MUTE). The ATTs are 00H when the PMDAC bit is "0". When the PMDAC returns to "1", the ATTs fade to their current value. The digital attenuator is independent of the soft mute function.

ATS	ATT speed		
	0dB to MUTE	1 step	
0	1061/fs	4/fs	Default
1	7424/fs	29/fs	

Table 18. Transition time between set values of ATT7-0 bits

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit goes to "1", the output signal is attenuated by –∞ during the ATT_DATA×ATT transition time (Table 18) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to –∞ after starting the operation, the attenuation is discontinued and is returned to the ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

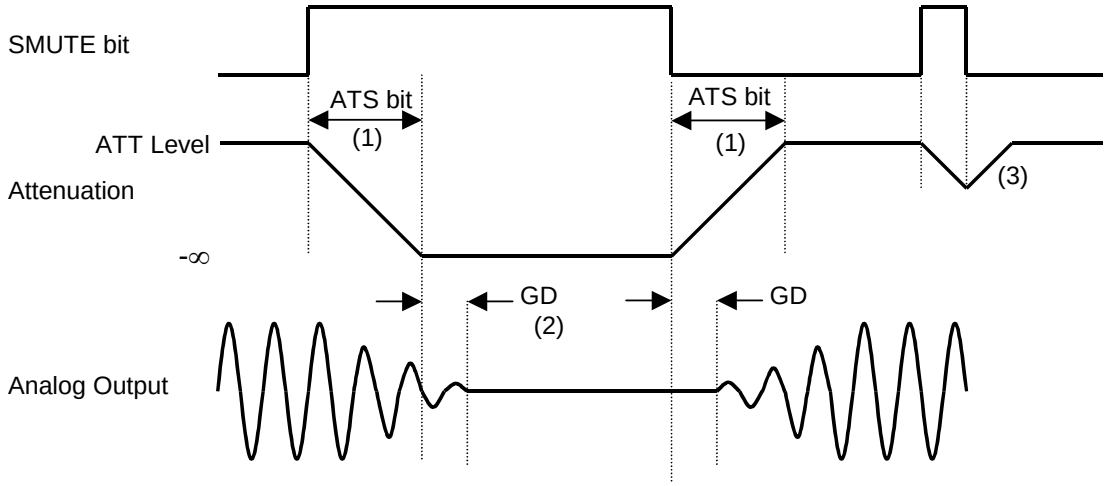


Figure 20. Soft Mute Function

Notes:

(1) ATT_DATA×ATT transition time (Table 18). For example, this time is 3712LRCK cycles (3712/fs) at ATS bit = "1" and ATT_DATA = "128".
(2) The analog output corresponding to the digital input has a group delay, GD.
(3) If the soft mute is cancelled before attenuating to –∞ after starting the operation, the attenuation is discontinued and it is returned to the ATT level by the same cycle.

■ De-emphasis Filter

The AK4368 includes a digital de-emphasis filter (tc = 50/15μs), using an IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter is enabled by setting DEM1-0 bits (Table 19).

DEM1 bit	DEM0 bit	De-emphasis	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 19. De-emphasis Filter Frequency Select

■ Bass Boost Function

By controlling the BST1-0 bits, a low frequency boost signal can be output from DAC. The setting value is common for both channels (Table 20).

BST1 bit	BST0 bit	BOOST	
0	0	OFF	Default
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 20. Low Frequency Boost Select

■ Mixing Function

MONO1-0 bits select the digital data mixing for the DAC (Table 21).

MONO1 bit	MONO0 bit	Lch	Rch	
0	0	L	R	Default
0	1	L	L	
1	0	R	R	
1	1	(L+R)/2	(L+R)/2	

Table 21. Mixer Setting

■ System Reset

The AK4368 should be reset once by bringing PDN pin “L” upon power-up. After exiting reset, VCOM, DAC, HPL, HPR, LOUT and ROUT switch to the power-down state. The contents of the control register are maintained until the reset is completed.

The DAC exits reset and power down states by MCKI after the PMDAC bit is changed to “1”. The DAC is in power-down mode until MCKI is input.

■ Headphone Output (HPL, HPR pins)

The power supply voltage for the headphone-amp is supplied from the HVDD pin and is centered on the MUTET voltage. The headphone-amp output load resistance is 16Ω (min). When the MUTEN bit is "1" at PMHPL=PMHPR= "1", the common voltage rises to 0.475 x HVDD. When the MUTEN bit is "0", the common voltage of the headphone-amp falls and the outputs (HPL and HPR pins) go to HVSS.

t_r: Rise Time up to VCOM/2	70k x C (typ)
t_f: Fall Time down to VCOM/2	60k x C (typ)

Table 22. Headphone-Amp Rise/Fall Time

[Example] : Capacitor between the MUTET pin and ground = 1μF:
Rise time up to VCOM/2: t_r = 70k x 1μ = 70ms(typ).
Fall time down to VCOM/2: t_f = 60k x 1μ = 60ms(typ).

When the PMHPL and PMHPR bits are "0", the headphone-amp is powered-down, and the outputs (HPL and HPR pins) go to HVSS.

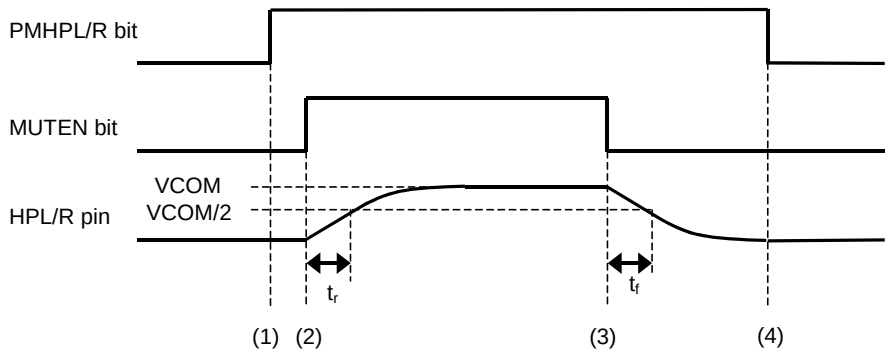


Figure 21. Power-up/Power-down Timing for the Headphone-Amp

(1) Headphone-amp power-up (PMHPL and PMHPR bits = "1"). The outputs are still at HVSS.
(2) Headphone-amp common voltage rises up (MUTEN bit = "1"). Common voltage of the headphone-amp is rising. This rise time depends on the capacitor value connected with the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ) when the capacitor value on MUTET pin is "C".
(3) Headphone-amp common voltage falls down (MUTEN bit = "0"). Common voltage of the headphone-amp is falling to HVSS. This fall time depends on the capacitor value connected with the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ) when the capacitor value on MUTET pin is "C".
(4) Headphone-amp power-down (PMHPL, PMHPR bits = "0"). The outputs are at HVSS. If the power supply is switched off or the headphone-amp is powered-down before the common voltage goes to HVSS, some pop noise may occur.

The cut-off frequency of the headphone-amp output depends on the external resistor and capacitor used. Table 23 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance R_L is 16Ω. Output powers are shown at AVDD = 2.4, 3.0 and 3.3V. The output voltage of the headphone is 0.47 x AVDD (Vpp) @−3dBFS.

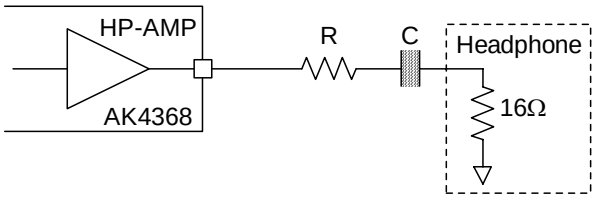


Figure 22. External Circuit Example of Headphone

R [Ω]	C [μF]	fc [Hz] BOOST=OFF	fc [Hz] BOOST=MIN	Output Power [mW]			
				HPG=0, 0dB			HPG=1, –4.8dB
				2.4V	3.0V	3.3V	3.3V
0	220	45	17	20	31	38	50
	100	100	43				
6.8	100	70	28	10	15	18	25
	47	149	78				
16	100	50	19	5	8	9	13
	47	106	47				

Table 23. Relationship of external circuit, output power and frequency response

DACHL, LINHL, MINHL, DACHR, RINHR and MINHR bits set the path, respectively. When the HPG bit is "0"(R_1= 100k), the gain is +0.76dB(typ) for all paths. When HPG bit is "1"(R_1= 50k), the DAC path gain is +6.76dB(typ).

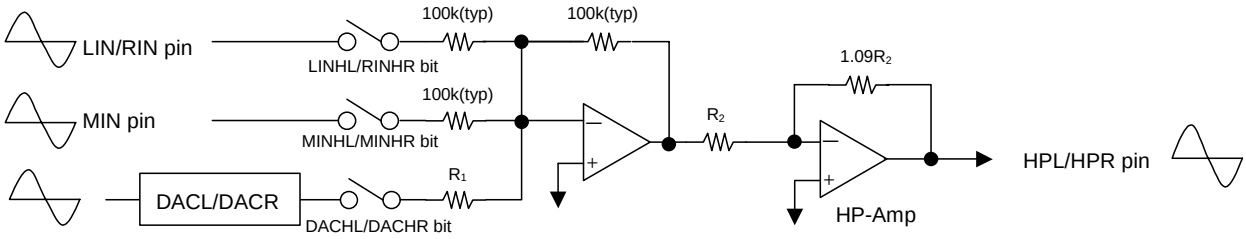


Figure 23. Summation circuit for headphone amp output (HPG bit = "0")

■ Stereo Line Output (LOUT, ROUT pins)

The common voltage is 0.475 x AVDD. The load resistance is 10kΩ(min). When the PMLO bit is "1", the stereo line output is powered-up. DACL, LINL, MINL, DACR, RINR and MINR bits set the path, respectively. When LOG bit is "0"(R_1= 100k) and ATTS3-0 bits is "0FH"(0dB), the gain is 0dB(typ) for all paths. When the LOG bit is "1"(R_1= 50k), the DAC path gain is +6dB.

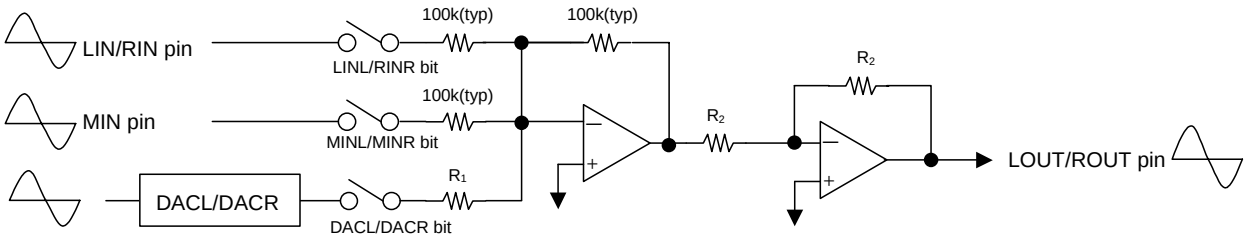


Figure 24. Summation circuit for stereo line output (LOG bit = "0")

■ Analog Output Volume

LOUT/ROUT volume is controlled by ATTS3-0 bits when LMUTE bit = "0" (0dB ~ –30dB, 2dB step, Table 24). Pop noise occurs when ATTS3-0 bits are changed.

LMUTE	ATTS3-0	Attenuation	
0	0FH	0dB	
	0EH	–2dB	
	0DH	–4dB	
	0CH	–6dB	
	:	:	
	:	:	
	01H	–28dB	
	00H	–30dB	
1	X	MUTE	Default

Table 24. LOUT/ROUT Volume ATT values (x: Don't care)

■ 3D Stereo Enhancement

AK4368 features a 3D stereo enhancement function. 3D1-0 bits control the power management of the 3D function block (Table 25), and DP1-0 bits set the 3D depth (Table 26). 3D1-0 and MUTEN bits should not be changed to avoid pop noise for 50ms after 3D1-0 bits are changed.

4.7nF±20% and 470nF±20% capacitors should be connected at 3DCAP1, 3DCAP2 and 3DCAP3 pins as shown in Figure 25. The load capacitance at 3DCAP1, 3DCAP2 and 3DCAP3 pins should be 20pF(max), respectively.

3D1 bit	3D0 bit	3D Function	3D Effect Output	Input Source	
0	0	OFF			Default
0	1	ON	LOUT, ROUT	Lineout summation circuit	
1	0	ON	HPL, HPR	Headphone summation circuit	
1	1	ON	LOUT, ROUT, HPL, HPR	Headphone summation circuit	

Table 25. 3D Function Power Management

DP1 bit	DP0 bit	3D Depth	
0	0	0%	Default
0	1	50%	
1	0	70%	
1	1	100%	

Table 26. 3D depth setting

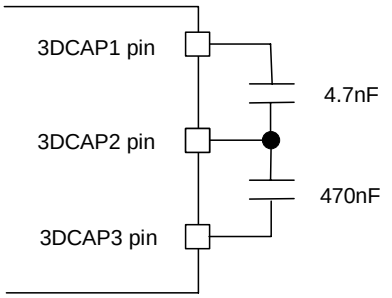


Figure 25. 3D Function External Circuit

■ Power-Up/Down Sequence (EXT mode)

1) DAC → HP-Amp

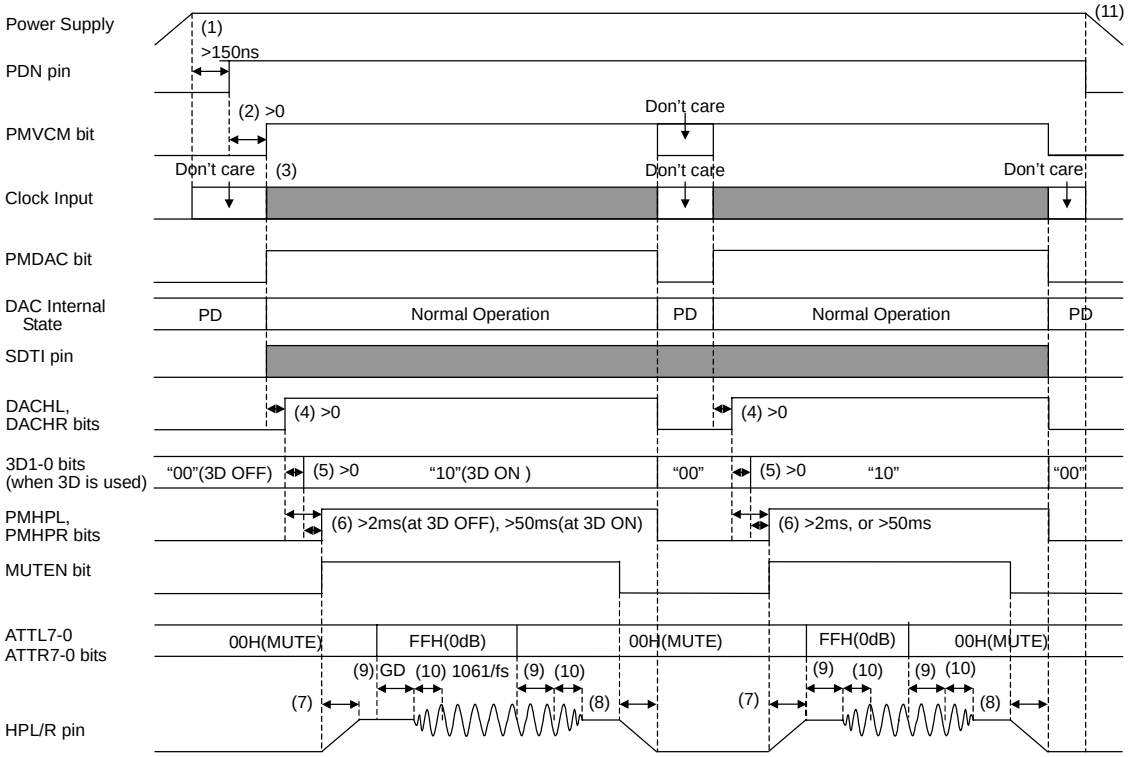


Figure 26. Power-up/down sequence of DAC and HP-amp (Don't care: except Hi-Z)

(1) PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM and PMDAC bits should be changed to "1" after PDN pin goes "H".
(3) External clocks (MCKI, BICK, LRCK) are needed to operate the DAC. When the PMDAC bit = "0", these clocks can be stopped. The headphone-amp can operate without these clocks.
(4) DACHL and DACHR bits should be changed to "1" after the PMDAC bit is changed to "1".
(5) When the 3D function is used, 3D1-0 bits should be changed to "10" after DACHL and DACHR bits are changed to "1".
(6) When the 3D function is not used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after the DACHL and DACHR bits are changed to "1". When the 3D function is used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 50ms after 3D1-0 bits are changed to "10".
(7) Rise time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(8) Fall time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after HPL and HPR pins go to HVSS. After that, the DACL/DACR bits should be changed to "0" and 3D1-0 bits = "00".
(9) Analog output corresponding to the digital input has a group delay (GD) of 22/fs(=499μs@fs=44.1kHz).
(10) The ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).
(11) The power supply should be switched off after the headphone-amp is powered down (HPL/R pins become "L").

2) DAC → Lineout

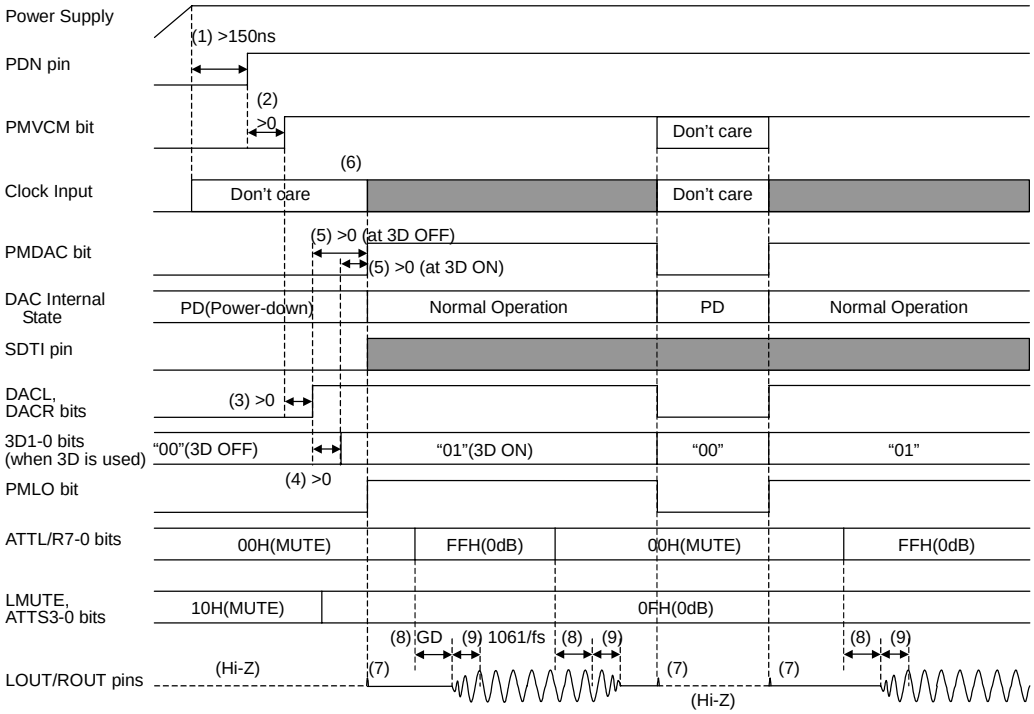


Figure 27. Power-up/down sequence of DAC and LOUT/ROUT (Don't care: except Hi-Z)

(1) PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM bit should be changed to "1" after the PDN pin goes "H".
(3) DACL and DACR bits should be changed to "1" after the PMVCM bit is changed to "1".
(4) When the 3D function is used, 3D1-0 bits should be changed to "01" after DACL and DACR bits are changed to "1".
(5) When the 3D function is not used, the PMDAC and PMLO bits should be changed to "1" after the DACL and DACR bits are changed to "1". When the 3D function is used, the PMDAC and PMLO bits should be changed to "1" after 3D1-0 bits are changed to "01".
(6) External clocks (MCKI, BICK, LRCK) are needed to operate the DAC. When the PMDAC bit = "0", these clocks can be stopped. The LOUT/ROUT buffer can operate without these clocks.
(7) When the PMLO bit is changed, pop noise is output from LOUT/ROUT pins.
(8) Analog output corresponding to the digital input has a group delay (GD) of 22fs(=499μs@fs=44.1kHz).
(9) The ATS bit sets the transition time of the digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).

3) LIN/RIN/MIN → HP-Amp

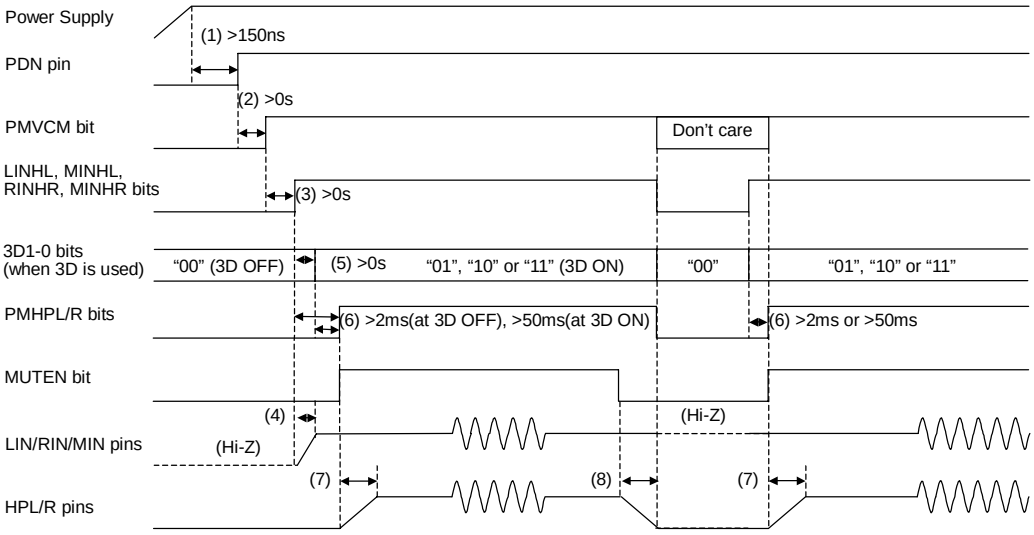


Figure 28. Power-up/down sequence of LIN/RIN/MIN and HP-amp

(1) PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after PDN pin goes "H".
(3) LINHL, MINHL, RINHR and MINHR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINHL, MINHL, RINHR or MINHR bit is changed to "1", LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) When the 3D function is used, 3D1-0 bits should be changed to "01", "10" or "11" after LINHL, MINHL, RINHR and MINHR bits are changed to "1".
(6) When the 3D function is not used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after LINHL, MINHL, RINHR and MINHR bits are changed to "1". When the 3D function is used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 50ms after 3D1-0 bits are changed to "01", "10" or "11".
(7) Rise time of the headphone-amp is determined by an external capacitor (C) of MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(8) Fall time of the headphone-amp is determined by an external capacitor (C) of MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after HPL and HPR pins go to HVSS. After that, LINHL, MINHL, RINHR and MINHR bits should be changed to "0".

4) LIN/RIN/MIN → Lineout

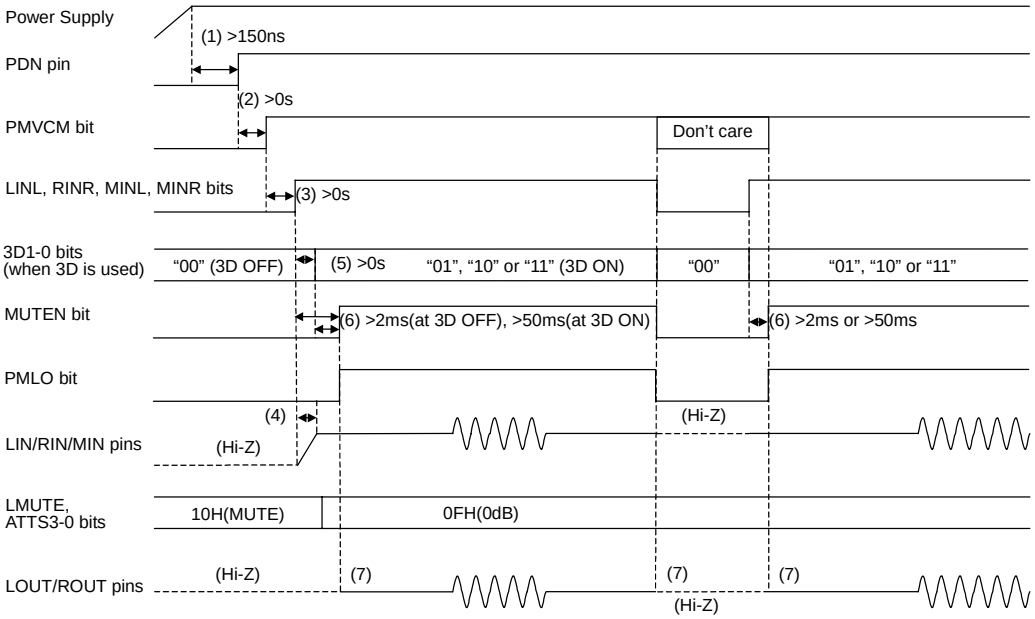


Figure 29. Power-up/down sequence of LIN/RIN/MIN and LOUT/ROUT

(1) PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after PDN pin goes "H".
(3) LINL, MINL, RINR and MINR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINL, MINL, RINR or MINR bit is changed to "1", LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) When the 3D function is used, 3D1-0 bits should be changed to "01", "10" or "11" after LINL, MINL, RINR and MINR bits are changed to "1".
(6) When the 3D function is not used, MUTEN and PMLO bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after LINL, MINL, RINR and MINR bits are changed to "1". When the 3D function is used, MUTEN and PMLO bits should be changed to "1" at least 50ms after 3D1-0 bits are changed to "01", "10" or "11".
(7) When the PMLO bit is changed, pop noise is output from LOUT/ROUT pins.

■ Power-Up/Down Sequence (PLL Slave mode)

1) DAC → HP-Amp

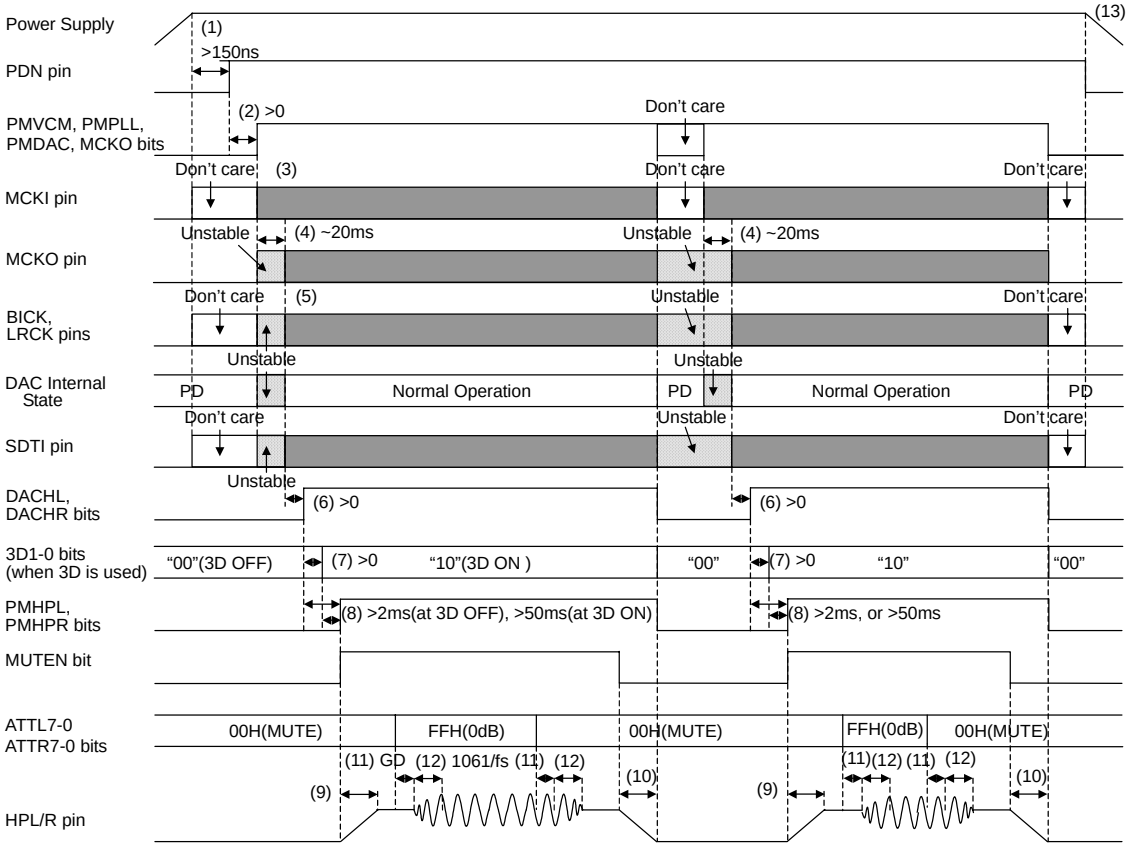


Figure 30. Power-up/down sequence of DAC and HP-amp (Don't care: except Hi-Z)

(1) PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM, PMPLL, PMDAC and MCKO bits should be changed to "1" after PDN pin goes "H".
(3) The PLL executes when the system clock is input to MCKI.
(4) The PLL lock time is referred to Note 26. Type 1-4 frequency is indicated in Table 2.
(5) Table 1. After the PLL is locked, the MCKO pin outputs the master clock.
(6) The clocks (BICK, LRCK) generated by MCKO are needed to operate the DAC. When the PMDAC bit = "0", these clocks can be stopped. The headphone-amp can operate without these clocks.
(7) DACHL and DACHR bits should be changed to "1" after the PLL is locked.
(8) When the 3D function is used, 3D1-0 bits should be changed to "10" after DACHL and DACHR bits are changed to "1".
(9) When the 3D function is not used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after the DACHL and DACHR bits are changed to "1". When the 3D function is used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 50ms after 3D1-0 bits are changed to "10".
(10) Rise time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(11) Fall time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after HPL and HPR pins go to HVSS. After that, the DACL/DACR bits should be changed to "0" and 3D1-0 bits should be changed to "00".
(12) Analog output corresponding to the digital input has a group delay (GD) of 22/fs(=499μs@fs=44.1kHz).
(13) The ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).
(14) The power supply should be switched off after the headphone-amp is powered down (HPL/R pins become "L").

2) DAC → Lineout

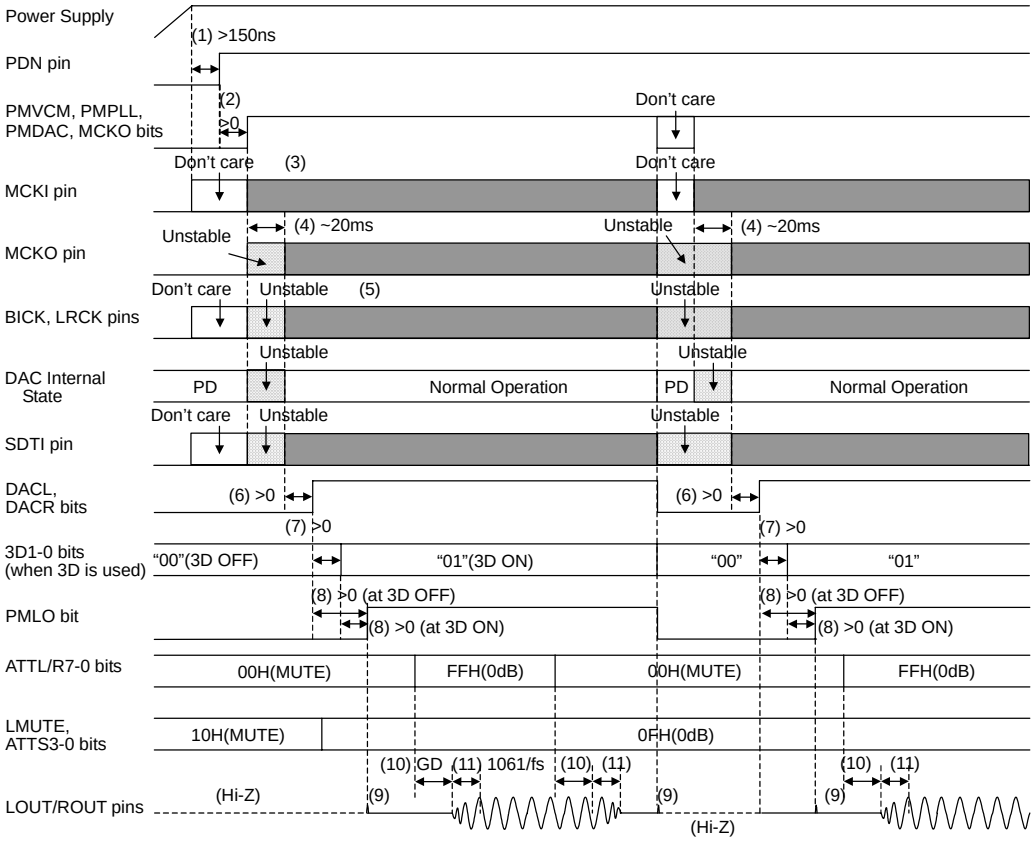


Figure 31. Power-up/down sequence of DAC and LOUT/ROUT (Don't care: except Hi-Z)

(1) PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM, PMPLL, PMDAC and MCKO bits should be changed to "1" after PDN pin goes "H".
(3) The PLL executes when the system clock is input to MCKI.
(4) The PLL lock time is referred to Note 26. Type 1-4 frequency is indicated in Table 2.
(5) Table 1. After the PLL is locked, the MCKO pin outputs the master clock.
(6) The clocks (BICK, LRCK) generated by MCKO are needed to operate the DAC. When the PMDAC bit = "0", these clocks can be stopped. The LOUT/ROUT buffer can operate without these clocks.
(7) DACL and DACR bits should be changed to "1" after the PLL is locked
(8) When the 3D function is used, 3D1-0 bits should be changed to "01" after DACL and DACR bits are changed to "1".
(9) PMLO bit is changed to "1".
(10) When the PMLO bit is changed, pop noise is output from LOUT/ROUT pins.
(11) Analog output corresponding to the digital input has a group delay (GD) of 22fs(=499μs@fs=44.1kHz).
(12) The ATS bit sets the transition time of the digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).

3) LIN/RIN/MIN → HP-Amp

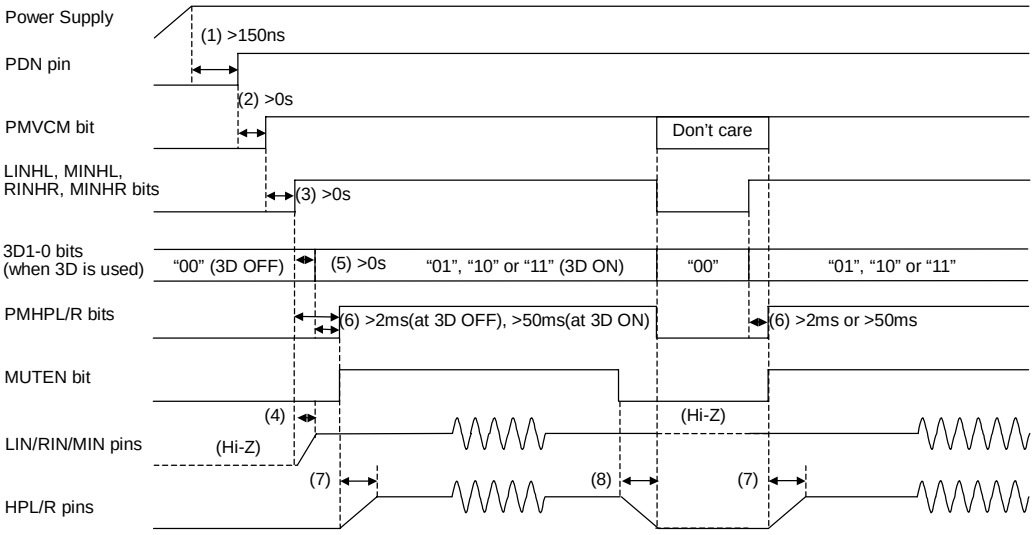


Figure 32. Power-up/down sequence of LIN/RIN/MIN and HP-amp

(1) PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after PDN pin goes "H".
(3) LINHL, MINHL, RINHR and MINHR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINHL, MINHL, RINHR or MINHR bit is changed to "1", LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) When the 3D function is used, 3D1-0 bits should be changed to "01", "10" or "11" after LINHL, MINHL, RINHR and MINHR bits are changed to "1".(refer to Table 25)
(6) When the 3D function is not used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after LINHL, MINHL, RINHR and MINHR bits are changed to "1". When the 3D function is used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 50ms after 3D1-0 bits are changed to "01", "10" or "11".
(7) Rise time of the headphone-amp is determined by an external capacitor (C) of MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(8) Fall time of the headphone-amp is determined by an external capacitor (C) of MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after HPL and HPR pins go to HVSS. After that, LINHL, MINHL, RINHR and MINHR bits should be changed to "0".

4) LIN/RIN/MIN → Lineout

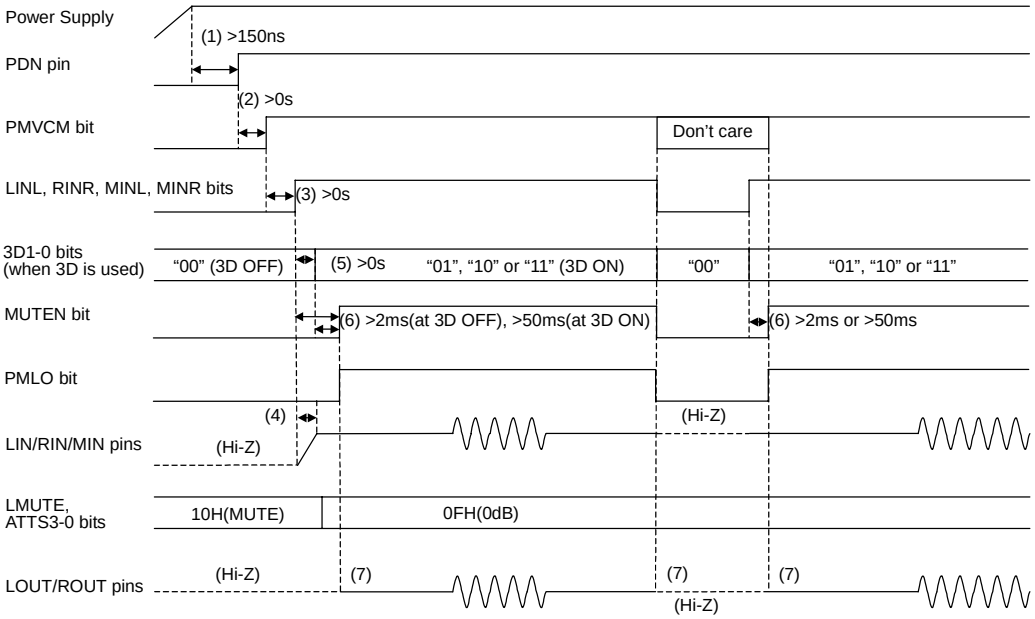


Figure 33. Power-up/down sequence of LIN/RIN/MIN and LOUT/ROUT

(1) PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after PDN pin goes "H".
(3) LINL, MINL, RINR and MINR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINL, MINL, RINR or MINR bit is changed to "1", LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) When the 3D function is used, 3D1-0 bits should be changed to "01", "10" or "11" after LINL, MINL, RINR and MINR bits are changed to "1".(refer to Table 25)
(6) When the 3D function is not used, MUTEN and PMLO bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after LINL, MINL, RINR and MINR bits are changed to "1". When the 3D function is used, MUTEN and PMLO bits should be changed to "1" at least 50ms after 3D1-0 bits are changed to "01", "10" or "11".
(7) When the PMLO bit is changed, pop noise is output from LOUT/ROUT pins.

■ Power-Up/Down Sequence (PLL Master mode)

1) DAC → HP-Amp

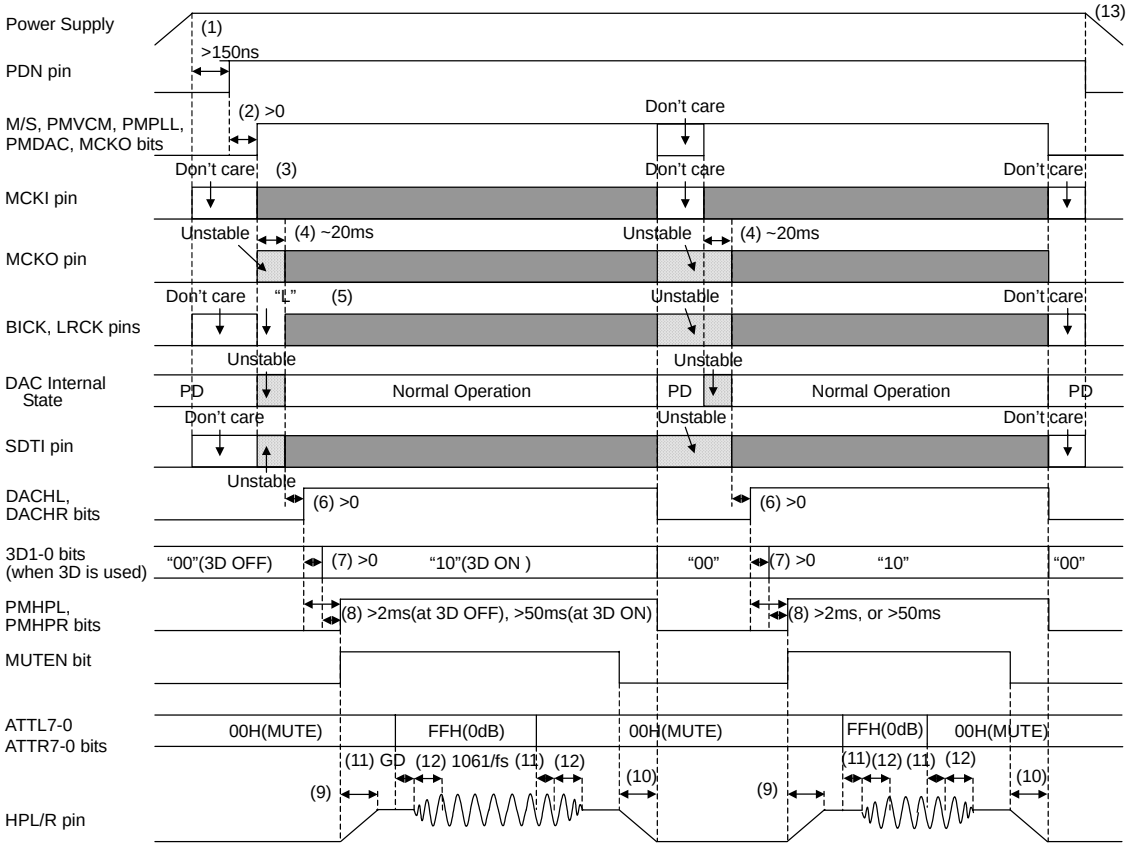


Figure 34 Power-up/down sequence of DAC and HP-amp (Don't care: except Hi-Z)

(1) PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM, PMPLL, PMDA, MCKO and M/S bits should be changed to "1" after PDN pin goes "H".
(3) The PLL executes when the system clock is input to MCKI.
(4) The PLL lock time is referred to Note 26. Type 1-4 frequency is indicated in Table 2.
(5) Table 1. After the PLL is locked, each clock is output from BICK, LRCK and MCKO pins.
(6) DACHL and DACHR bits should be changed to "1" after the PLL is locked.
(7) When the 3D function is used, 3D1-0 bits should be changed to "10" after DACHL and DACHR bits are changed to "1".
(8) When the 3D function is not used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after the DACHL and DACHR bits are changed to "1". When the 3D function is used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 50ms after 3D1-0 bits are changed to "10".
(9) Rise time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(10) Fall time of the headphone-amp is determined by an external capacitor (C) of the MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after HPL and HPR pins go to HVSS. After that, the DACL/DACR bits should be changed to "0" and 3D1-0 bits should be changed to "00".
(11) Analog output corresponding to the digital input has a group delay (GD) of 22/fs(=499μs@fs=44.1kHz).
(12) The ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).
(13) The power supply should be switched off after the headphone-amp is powered down (HPL/R pins become "L").

2) DAC → Lineout

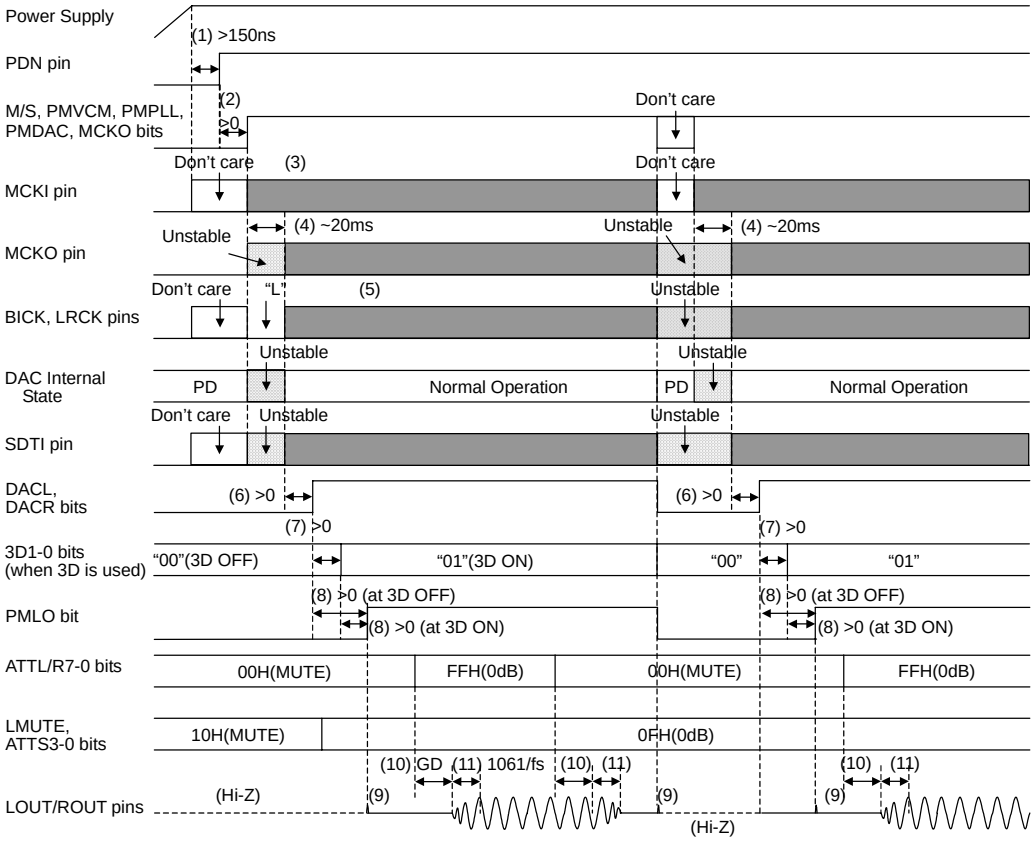


Figure 35. Power-up/down sequence of DAC and LOUT/ROUT(Don't care: except Hi-Z)

(1) PDN pin should be set to "H" at least 150ns after power is supplied.
(2) PMVCM, PMPLL, PMDAC, MCKO and M/S bits should be changed to "1" after PDN pin goes "H".
(3) The PLL executes when the system clock is input to MCKI.
(4) The PLL lock time is referred to Note 26. Type 1-4 frequency is indicated in Table 2.
(5) Table 1. After the PLL is locked, each clock is output from BICK, LRCK and MCKO pins.
(6) DACL and DACR bits should be changed to "1" after the PLL is locked.
(7) When the 3D function is used, 3D1-0 bits should be changed to "01" after DACL and DACR bits are changed to "1".
(8) PMLO bit is changed to "1".
(9) When the PMLO bit is changed, pop noise is output from LOUT/ROUT pins.
(10) Analog output corresponding to the digital input has a group delay (GD) of 22fs(=499μs@fs=44.1kHz).
(11) The ATS bit sets the transition time of the digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).

3) LIN/RIN/MIN → HP-Amp

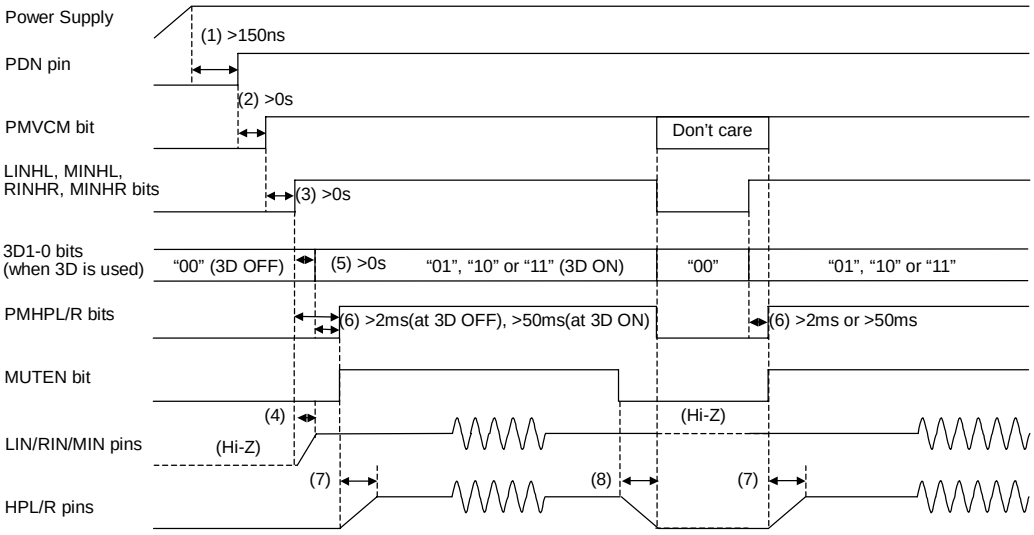


Figure 36. Power-up/down sequence of LIN/RIN/MIN and HP-amp

(1) PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after PDN pin goes "H".
(3) LINHL, MINHL, RINHR and MINHR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINHL, MINHL, RINHR or MINHR bit is changed to "1", LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) When the 3D function is used, 3D1-0 bits should be changed to "01", "10" or "11" after LINHL, MINHL, RINHR and MINHR bits are changed to "1".(refer to Table 25)
(6) When the 3D function is not used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after LINHL, MINHL, RINHR and MINHR bits are changed to "1". When the 3D function is used, PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 50ms after 3D1-0 bits are changed to "01", "10" or "11".
(7) Rise time of the headphone-amp is determined by an external capacitor (C) of MUTET pin. The rise time up to VCOM/2 is t_r = 70k x C(typ). When C=1μF, t_r = 70ms(typ).
(8) Fall time of the headphone-amp is determined by an external capacitor (C) of MUTET pin. The fall time down to VCOM/2 is t_f = 60k x C(typ). When C=1μF, t_f = 60ms(typ).
PMHPL and PMHPR bits should be changed to "0" after HPL and HPR pins go to HVSS. After that, LINHL, MINHL, RINHR and MINHR bits should be changed to "0".

4) LIN/RIN/MIN → Lineout

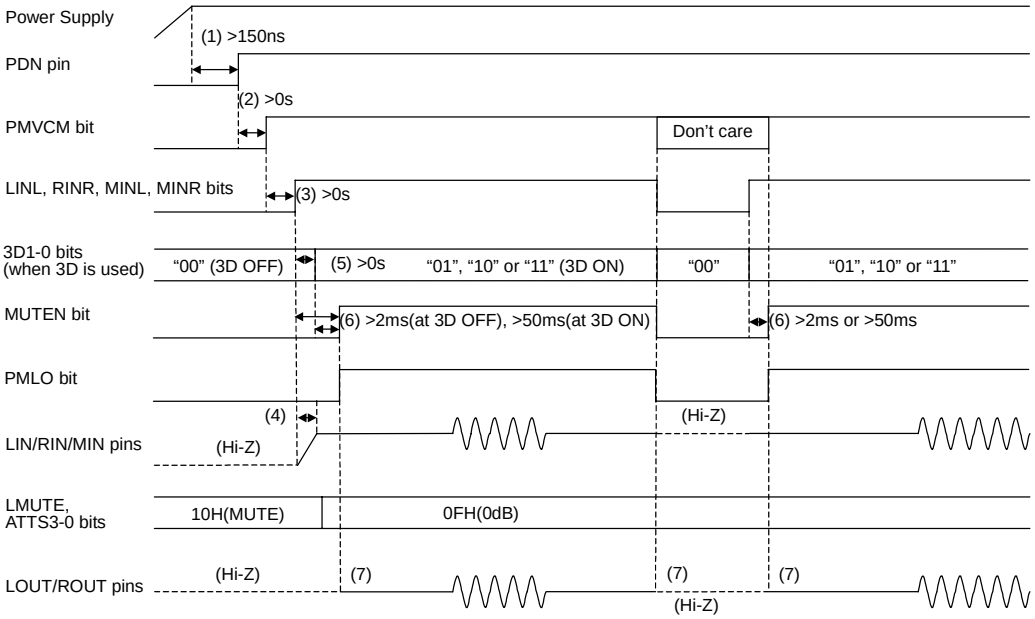


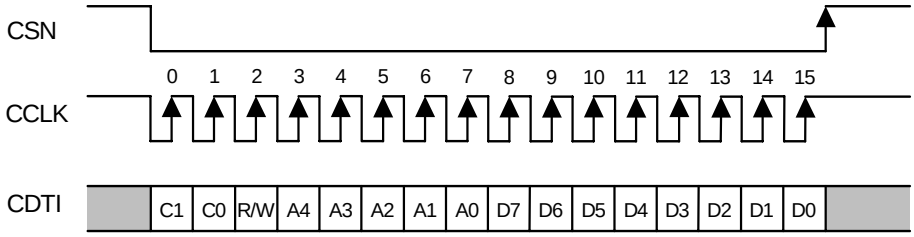
Figure 37. Power-up/down sequence of LIN/RIN/MIN and LOUT/ROUT

(1) PDN pin should be set to "H" at least 150ns after power is supplied. MCKI, BICK and LRCK can be stopped when DAC is not used.
(2) PMVCM bit should be changed to "1" after PDN pin goes "H".
(3) LINL, MINL, RINR and MINR bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINL, MINL, RINR or MINR bit is changed to "1", LIN, RIN or MIN pin is biased to 0.475 x AVDD.
(5) When the 3D function is used, 3D1-0 bits should be changed to "01", "10" or "11" after LINL, MINL, RINR and MINR bits are changed to "1".(refer to Table 25)
(6) When the 3D function is not used, MUTEN and PMLO bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after LINL, MINL, RINR and MINR bits are changed to "1". When the 3D function is used, MUTEN and PMLO bits should be changed to "1" at least 50ms after 3D1-0 bits are changed to "01", "10" or "11".
(7) When the PMLO bit is changed, pop noise is output from LOUT/ROUT pins.

■ Serial Control Interface

(1) 3-wire Serial Control Mode (I2C pin = "L")

Internal registers may be written to via the 3-wire μP interface pins (CSN, CCLK and CDTI). The data on this interface consists of the Chip address (2-bits, Fixed to "01"), Read/Write (1-bit, Fixed to "1", Write only), Register address (MSB first, 5-bits) and Control data (MSB first, 8-bits). Address and data are clocked in on the rising edge of CCLK. For write operations, the data is latched after a low-to-high transition of the 16th CCLK. The clock speed of CCLK is 5MHz(max). The value of the internal registers is initialized at PDN pin = "L".



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 38. 3-wire Serial Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")
The AK4368 supports fast-mode I²C-bus (max: 400kHz, Version 1.0).

(2)-1. WRITE Operations
Figure 39 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 45). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001000". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets this device address bit (Figure 40). If the slave address matches that of the AK4368, the AK4368 generates an acknowledgement and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 46). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4368. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 41). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 42). The AK4368 generates an acknowledgement after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 45).

The AK4368 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4368 generates an acknowledgement and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 0CH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 47) except for the START and STOP conditions.

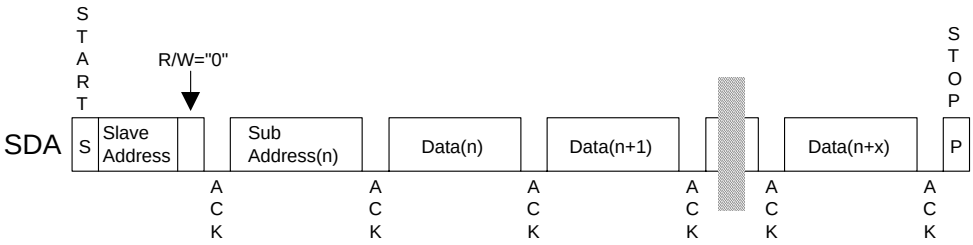


Figure 39. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	0	CAD0	R/W

(Those CAD0 should match with CAD0 pin)
Figure 40. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 41. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 42. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = “1” for the READ operation of the AK4368. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 0CH prior to generating a stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

The AK4368 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4368 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to “1”, the AK4368 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledgement to the data but instead generates a stop condition, the AK4368 ceases transmission.

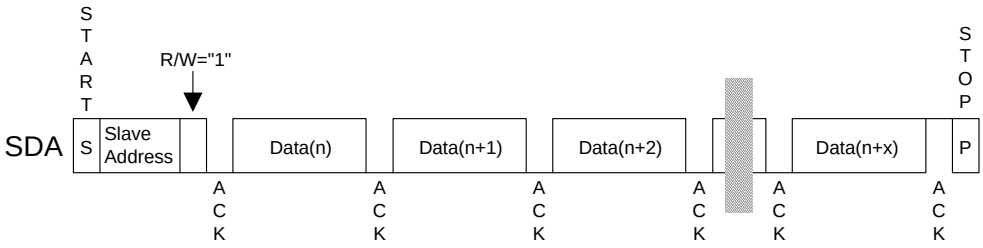


Figure 43. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to “1”. The AK4368 then generates an acknowledgement, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledgement to the data but instead generates a stop condition, the AK4368 ceases transmission.

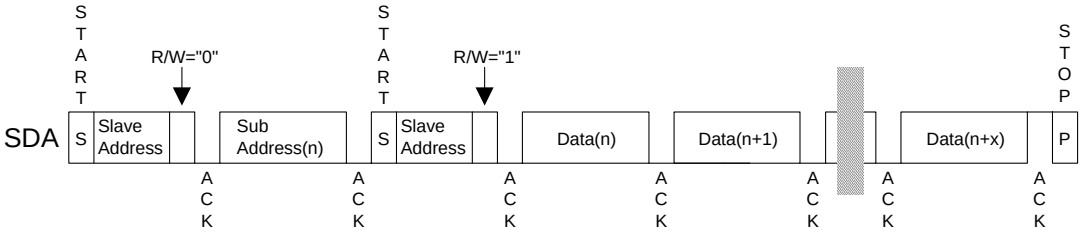


Figure 44. RANDOM ADDRESS READ

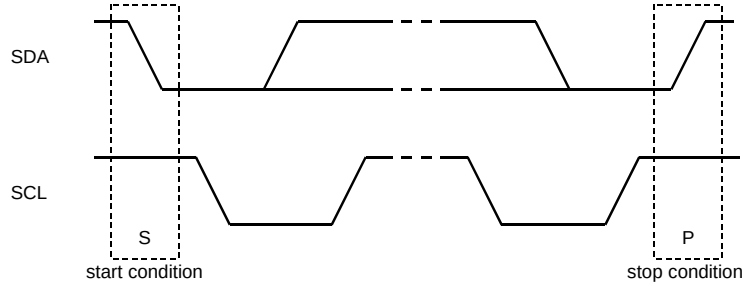


Figure 45. START and STOP Conditions

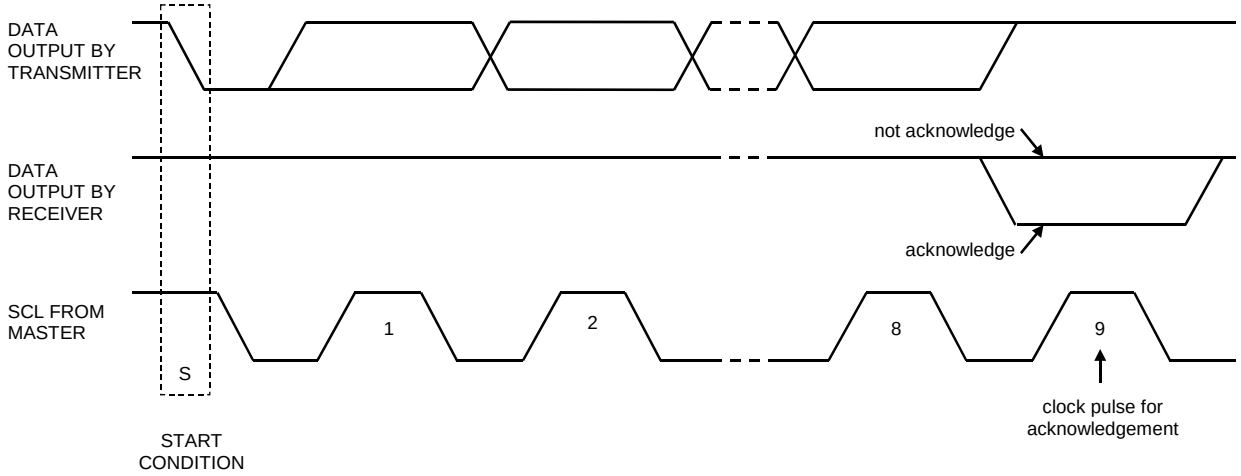


Figure 46. Acknowledge on the I^2C-Bus

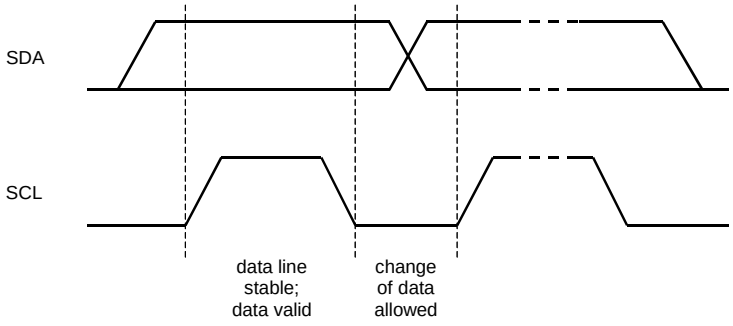


Figure 47. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	PMPLL	PMLO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
01H	PLL Control	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
02H	Clock Control	0	0	M/S	MCKAC	BF	PS0	PS1	MCKO
03H	Mode Control 0	0	MONO1	MONO0	BCKP	LRP	DIF2	DIF1	DIF0
04H	Mode Control 1	ATS	DATTC	LMUTE	SMUTE	BST1	BST0	DEM1	DEM0
05H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
06H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
07H	Headphone Out Select	0	HPG	MINHR	MINHL	RINHR	LINHL	DACHR	DACHL
08H	Lineout Select	0	LOG	MINR	MINL	RINR	LINL	DACR	DACL
09H	Lineout ATT	0	0	0	0	ATTS3	ATTS2	ATTS1	ATTS0
0AH	ALC Mode Control 1	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
0BH	ALC Mode Control 2	0	0	ALC	ROTM1	ROTM0	LMAT1	LMAT0	RATT
0CH	3D Control	0	0	0	0	DP1	DP0	3D1	3D0

All registers inhibit writing at PDN pin = "L".
PDN pin = "L" resets the registers to their default values.
For addresses from 0DH to 1FH, data must not be written.
Unused bits must contain a "0" value.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	PMPLL	PMLO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMVCM: Power Management for VCOM Block
0: Power OFF (Default)
1: Power ON

PMDAC: Power Management for DAC Blocks
0: Power OFF (Default)
1: Power ON
When the PMDAC bit is changed from "0" to "1", the DAC is powered-up to the current register values (ATT value, sampling rate, etc).

PMHPL: Power Management for the left channel of the headphone-amp
0: Power OFF (Default). HPL pin goes to HVSS(0V).
1: Power ON

PMHPR: Power Management for the right channel of the headphone-amp
0: Power OFF (Default). HPR pin goes to HVSS(0V).
1: Power ON

MUTEN: Headphone Amp Mute Control
0: Mute (Default). HPL and HPR pins go to HVSS(0V).
1: Normal operation. HPL and HPR pins go to 0.475 x AVDD.

PMLO: Power Management for Stereo Output
0: Power OFF (Default) LOUT/ROUT pins go to Hi-Z.
1: Power ON

PMPLL: Power Management for PLL
0: Power OFF: EXT mode (Default)
1: Power ON: PLL mode

Each block can be powered-down respectively by writing "0" in each bit of this address. When the PDN pin is "L", all blocks are powered-down regardless as setting of this address. In this case, register is initialized to the default value.

When PMVCM, PMDAC, PMHPL, PMHPR, PMLO, PMPLL and MCKO bits are "0", all blocks are powered-down. The register values remain unchanged. Power supply current is 20μA(typ) in this case. For fully shut down (typ. 1μA), PDN pin should be "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	PLL Control	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

FS3-0: Select Sampling Frequency
PLL mode: Table 2
EXT mode: Table 6

PLL3-0: Select MCKI Frequency
PLL mode: Note 26. Type 1-4 frequency is indicated in Table 2.
Table 1
EXT mode: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Clock Control	0	0	M/S	MCKAC	BF	PS0	PS1	MCKO
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MCKO: Control of MCKO signal
0: Disable (Default)
1: Enable

PS1-0: MCKO Frequency
PLL mode: Table 3
EXT mode: Table 7

BF: BICK Period setting in Master Mode. In slave mode, this bit is ignored.
0: 32fs (Default)
1: 64fs

MCKAC: MCKI Input Mode Select
0: CMOS input (Default)
1: AC coupling input

M/S: Master/Slave Mode Select
0: Slave mode (Default)
1: Master mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control 0	0	MONO1	MONO0	BCKP	LRP	DIF2	DIF1	DIF0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF2-0: Audio Data Interface Format Select (Table 11)
Default: “010” (Mode 2)

LRP: LRCK Polarity Select in Slave Mode
0: Normal (Default)
1: Invert

BCKP: BICK Polarity Select in Slave Mode
0: Normal (Default)
1: Invert

MONO1-0: Mixing Select (Table 21)
Default: “00” (LR)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	ATS	DATTC	LMUTE	SMUTE	BST1	BST0	DEM1	DEM0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	0	1

DEM1-0: De-emphasis Filter Frequency Select (Table 19)
Default: "01" (OFF)

BST1-0: Low Frequency Boost Function Select (Table 20)
Default: "00" (OFF)

SMUTE: Soft Mute Control
0: Normal operation (Default)
1: DAC outputs soft-muted

LMUTE: Mute control for LOUT/ROUT (Table 24)
0: Normal operation. ATTS3-0 bits control attenuation value.
1: Mute. ATTS3-0 bits are ignored. (Default)

DATTC: DAC Digital Attenuator Control Mode Select
0: Independent (Default)
1: Dependent
At DATTC bit = "1", ATTL7-0 bits control both channel attenuation levels, while register values of ATTL7-0 bits are not written to the ATTR7-0 bits. At DATTC bit = "0", the ATTL7-0 bits control the left channel level and the ATTR7-0 bits control the right channel level.

ATS: Digital attenuator transition time setting (Table 18)
0: 1061/fs (Default)
1: 7424/fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
06H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTL7-0: Setting of the attenuation value of output signal from DACL (Table 17)
ATTR7-0: Setting of the attenuation value of output signal from DACR (Table 17)
Default: "00H" (MUTE)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Headphone Out Select	0	HPG	MINHR	MINHL	RINHR	LINHL	DACHR	DACHL
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACHL: DAC left channel output signal is added to the left channel of the headphone-amp.
0: OFF (Default)
1: ON

DACHR: DAC right channel output signal is added to the right channel of the headphone-amp.
0: OFF (Default)
1: ON

LINHL: Input signal to LIN pin is added to the left channel of the headphone-amp.
0: OFF (Default)
1: ON

RINHR: Input signal to RIN pin is added to the right channel of the headphone-amp.
0: OFF (Default)
1: ON

MINHL: Input signal to MIN pin is added to the left channel of the headphone-amp.
0: OFF (Default)
1: ON

MINHR: Input signal to MIN pin is added to the right channel of the headphone-amp.
0: OFF (Default)
1: ON

HPG: DAC → HPL/R Gain
0: 0.76dB (Default)
1: +6.76dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Lineout Select	0	LOG	MINR	MINL	RINR	LINL	DACR	DACL
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACL: DAC left channel output is added to the LOUT buffer amp.
0: OFF (Default)
1: ON

DACR: DAC right channel output is added to the ROUT buffer amp.
0: OFF (Default)
1: ON

LINL: Input signal to the LIN pin is added to the LOUT buffer amp.
0: OFF (Default)
1: ON

RINR: Input signal to the RIN pin is added to the ROUT buffer amp.
0: OFF (Default)
1: ON

MINL: Input signal to the MIN pin is added to the LOUT buffer amp.
0: OFF (Default)
1: ON

MINR: Input signal to the MIN pin is added to the ROUT buffer amp.
0: OFF (Default)
1: ON

LOG: DAC → LOUT/ROUT Gain
0: 0dB (Default)
1: +6dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Lineout ATT	0	0	0	0	ATTS3	ATTS2	ATTS1	ATTS0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTS3-0: Analog volume control for LOUT/ROUT (Table 24)
Default: LMUTE bit = "1", ATTS3-0 bits = "0000" (MUTE)

Setting of ATTS3-0 bits is enabled at LMUTE bit is "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ALC Mode Control 1	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

REF7-0: Reference Value for ALC Recovery Operation, 0.375dB step, 81 level, Default: “91H” (Table 15)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 2	0	0	ALC	ROTM1	ROTM0	LMAT1	LMAT0	RATT
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	0

RATT: ALC Recovery GAIN Step (Table 14)

LMAT1-0: ALC Limiter ATT Step (Table 13)

ROTM1-0: ALC Recovery Waiting Period, Limiter/Recovery Operation Zero Crossing Timeout Period (Table 12)

ALC: ALC Enable
0: ALC Disable (Default)
1: ALC Enable

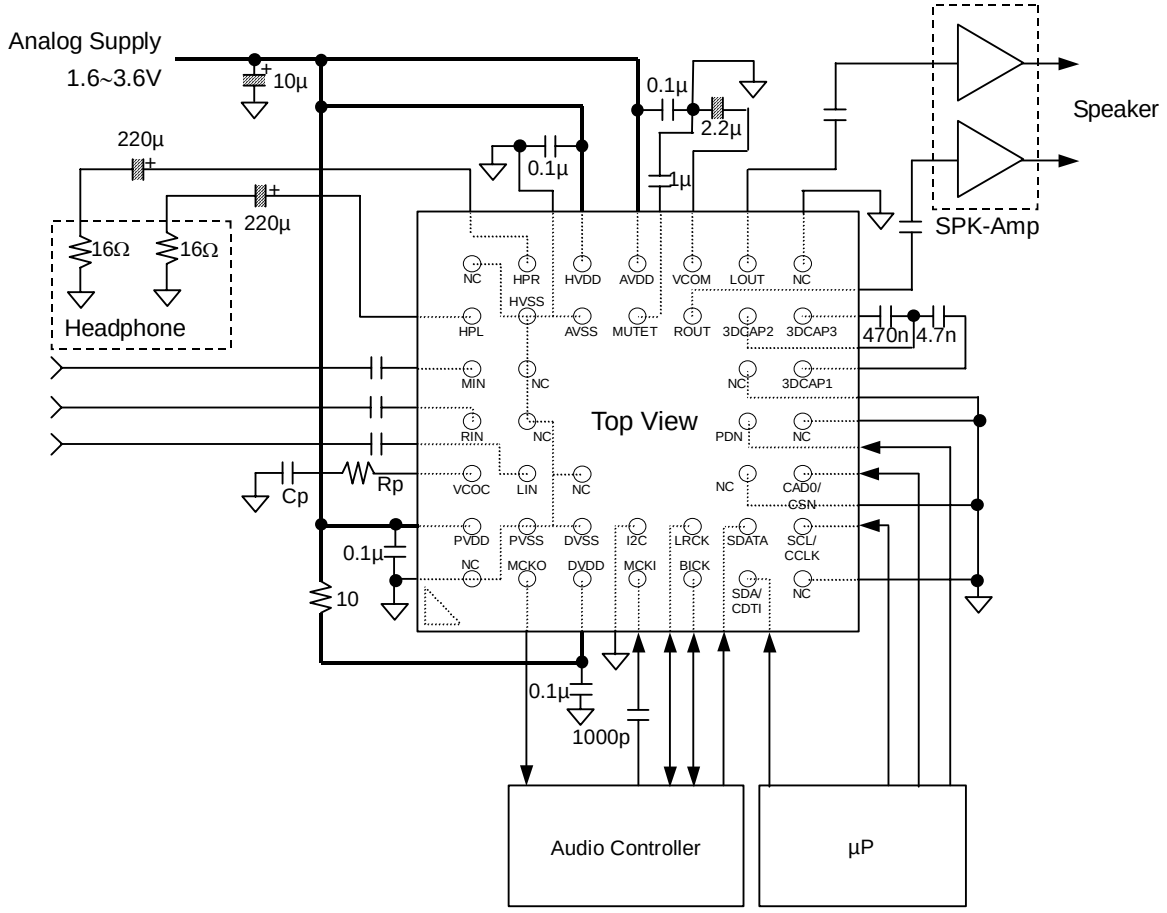
Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	3D Control	0	0	0	0	DP1	DP0	3D1	3D0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

3D1-0: 3D Stereo Enhancement Enable (Table 25)
Default: “00” (Disable)

DP1-0: 3D Depth (Table 26)
Default: “00” (0%)

SYSTEM DESIGN

Figure 48 shows the system connection diagram. An evaluation board [AKD4368] is available which demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:

- AVSS, DVSS, HVSS and PVSS of the AK4368 should be distributed separately from the ground of external controllers.
- Do not let digital input pins float.
- When the AK4368 is in EXT mode (PMPLL bit = "0"), a resistor and capacitor for the VCOC pin is not needed.
- When the AK4368 is in PLL mode (PMPLL bit = "1"), a resistor and capacitor for the VCOC pin is shown in Note 26. Type 1-4 frequency is indicated in Table 2.

Table 1.

- When the AK4368 is used in master mode, LRCK and BICK pins are floating before the M/S bit is changed to "1". Therefore, a 100kΩ pull-up resistor should be connected to the LRCK and BICK pins of the AK4368.

Figure 48. Typical Connection Diagram (In case of AC coupling to MCKI)

1. Grounding and Power Supply Decoupling

The AK4368 requires careful attention to power supply and grounding arrangements. AVDD, PVDD and HVDD are usually supplied from the analog power supply in the system and DVDD is supplied from AVDD via a 10Ω resistor. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. When AVDD and HVDD are supplied separately, AVDD is powered-up at the same time or earlier than HVDD. When the AK4368 is powered-down, HVDD is powered-down at the same time or later than AVDD. The power up sequence of PVDD is not critical. AVSS, DVSS, PVSS and HVSS must be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close to the AK4368 as possible, with the small value ceramic capacitors being the nearest.

2. Voltage Reference

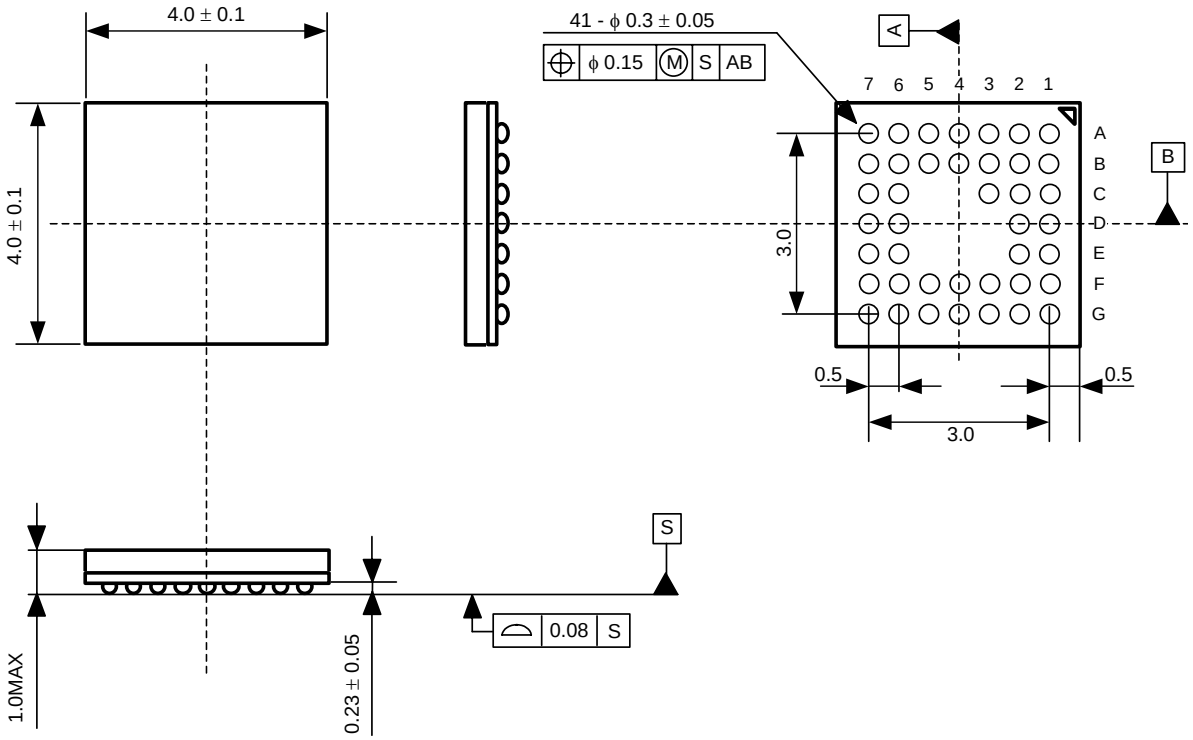
The input voltage to AVDD sets the analog output range. A 0.1μF ceramic capacitor and a 10μF electrolytic capacitor are connected between AVDD and AVSS. VCOM is a signal ground of this chip (0.475 x AVDD). An electrolytic 2.2μF attached between VCOM and AVSS eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clock, should be kept away from AVDD and VCOM in order to avoid unwanted coupling into the AK4368.

3. Analog Outputs

The analog outputs are single-ended outputs, and 0.47 x AVDD Vpp(typ)@-3dBFS for headphone-amp and 0.61xAVDD Vpp(typ) @0dBFS for LOUT/ROUT centered on the VCOM voltage. The input data format is 2's compliment. The output voltage is a positive full scale for 7FFFFFH(@24bit) and negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit).

DC offsets on the analog outputs is eliminated by AC coupling since the analog outputs have a DC offset equal to VCOM plus a few mV.

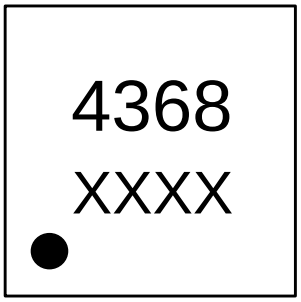
PACKAGE



■ **Package & Lead frame material**

Package molding compound: Epoxy
Interposer material: BT resin
Solder ball material: SnAgCu

MARKING



XXXX: Date code (4 digit)
Pin #1 indication

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/07/25	00	First Edition		

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