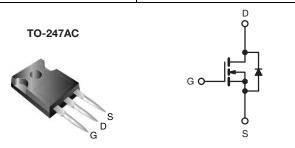


Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	600				
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.18				
Q _g (Max.) (nC)	180				
Q _{gs} (nC)	56				
Q _{gd} (nC)	86				
Configuration	Single				



N-Channel MOSFET

FEATURES

• Low Gate Charge Qq Results in Simple Drive



- Improved Gate, Avalanche and Dynamic dV/dt RoHS Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Enhanced Body Diode dV/dt Capability
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Hard Switching Primary or PFC Switch
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Motor Drive

ORDERING INFORMATION			
Package	TO-247AC		
Load (Rh) from	IRFP27N60KPbF		
Lead (Pb)-free	SiHFP27N60K-E3		
SnPb	IRFP27N60K		
SIPO	SiHFP27N60K		

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	600	V	
Gate-Source Voltage			V_{GS}	± 30	V	
Continuous Proin Current	V _{GS} at 10 V	T _C = 25 °C	- I _D	27		
Continuous Drain Current		T _C = 100 °C		18	Α	
Pulsed Drain Current ^a			I _{DM}	110		
Linear Derating Factor				4.0	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	530	mJ	
Repetitive Avalanche Current ^a			I _{AR}	27	А	
Repetitive Avalanche Energy ^a			E _{AR}	50	mJ	
Maximum Power Dissipation $T_C = 25 ^{\circ}C$			P _D	500	W	
Peak Diode Recovery dV/dt ^c			dV/dt	13	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150		
Soldering Recommendations (Peak Temperature) for 10 s				300 ^d	- °C	
Mounting Toyana	6.00 04.1	0.00 140		10	lbf ⋅ in	
Mounting Torque	6-32 or M3 screw			1.1	N · m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Starting T_J = 25 °C, L = 1.4 mH, R_g = 25 Ω , I_{AS} = 27 A, dV/dt = 13 V/ns (see fig. 12). c. I_{SD} \leq 27 A, dI/dt \leq 390 A/µs, V_{DD} \leq V_{DS}, T_J \leq 150 °C.

- d. 1.6 mm from case.

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply

IRFP27N60K, SiHFP27N60K

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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	40		
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.24	-	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.29		

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static		•						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	= 0 V, I _D = 250 μA	600	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referen	ce to 25 °C, I _D = 1 mA	-	640	-	mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS}	$= V_{GS}, I_D = 250 \mu A$	3.0	-	5.0	V	
Gate-Source Leakage	I _{GSS}		$V_{GS} = \pm 30 \text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	1	V _{DS} :	V _{DS} = 600 V, V _{GS} = 0 V		-	50	μA	
Zero date voltage Brain ourient	I _{DSS}	$V_{DS} = 480^{\circ}$	V, V _{GS} = 0 V, T _J = 125 °C	-	-	250	μΑ	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 16 A ^b	-	0.18	0.22	Ω	
Forward Transconductance	9 _{fs}	V_{DS}	$= 50 \text{ V}, I_D = 16 \text{ A}$	14	-	-	S	
Dynamic								
Input Capacitance	C_{iss}		$V_{GS} = 0 V$	-	4660	-		
Output Capacitance	Coss		$V_{DS} = 25 \text{ V}$	-	460	-		
Reverse Transfer Capacitance	C_{rss}	f = 1	f = 1.0 MHz, see fig. 5		41	-] _ [
Output Conscitance	ut Capacitance	$V_{GS} = 0 V$	V _{DS} = 1.0 V , f = 1.0 MHz	-	5490	-	pF	
Output Oapacitance		$V_{DS} = 480 \text{ V}$, $f = 1.0 \text{ MHz}$	-	120	-			
Effective Output Capacitance	C _{oss} eff.	$V_{GS} = 0 V$	V _{DS} = 0 V to 480 V	-	250	-		
Total Gate Charge	Q_g			-	-	180		
Gate-Source Charge	Q _{gs}	$V_{GS} = 10 \text{ V}$ $I_D = 27 \text{ A}, V_{DS} = 480 \text{ V}$ see fig. 6 and 13^{b}		-	-	56	nC	
Gate-Drain Charge	Q_{gd}			-	-	86		
Turn-On Delay Time	t _{d(on)}	'		_	27	-		
Rise Time	t _r	V_{DD}	V _{DD} = 300 V, I _D = 27 A		110	-]	
Turn-Off Delay Time	t _{d(off)}	$R_0 = 4.3 \Omega$, V _{GS} = 10 V, see fig. 10 ^b	-	43	-	ns	
Fall Time	t _f	ys,go - 10 v, 000g. 10		-	38	-		
Drain-Source Body Diode Characteristic	cs							
Continuous Source-Drain Diode Current	Is	MOSFET symbol showing the integral reverse p - n junction diode		-	-	27	- A	
Pulsed Diode Forward Current ^a	I _{SM}			-	-	110		
Body Diode Voltage	V_{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 27 \text{A}, V_{GS} = 0 \text{V}^{\text{b}}$		-	-	1.5	٧	
Body Diode Reverse Recovery Time	t _{rr}			-	620	920	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 27 \text{A}, \text{dl/dt} = 100 \text{A/} \mu \text{s}^{\text{b}}$		-	11	16	μC	
Reverse Recovery Current	I _{RRM}			-	36	53	Α	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300~\mu s;$ duty cycle $\leq 2~\%.$
- c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80% V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

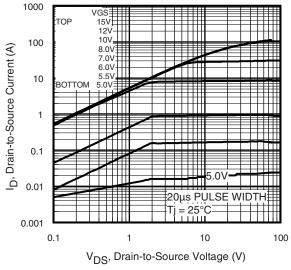


Fig. 1 - Typical Output Characteristics

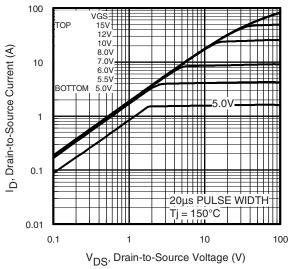


Fig. 2 - Typical Output Characteristics

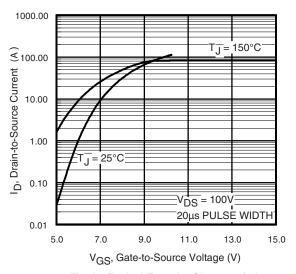


Fig. 3 - Typical Transfer Characteristics

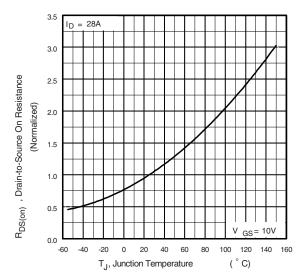


Fig. 4 - Normalized On-Resistance vs. Temperature

IRFP27N60K, SiHFP27N60K

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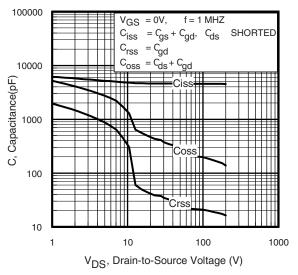


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

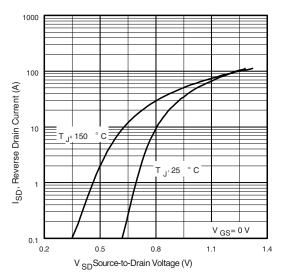


Fig. 7 - Typical Source-Drain Diode Forward Voltage

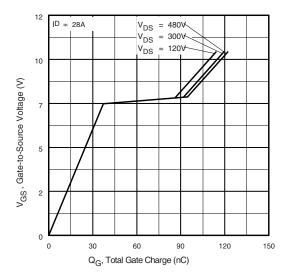


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

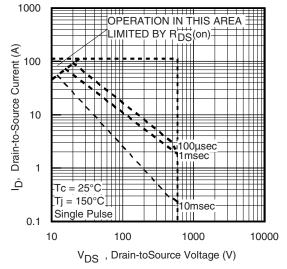


Fig. 8 - Maximum Safe Operating Area



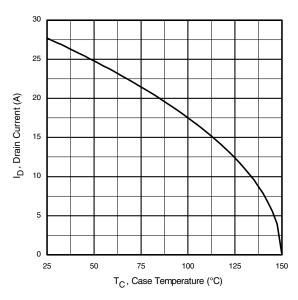


Fig. 9 - Maximum Drain Current vs. Case Temperature

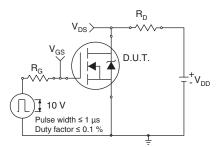


Fig. 10a - Switching Time Test Circuit

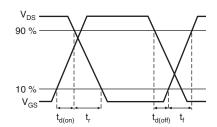


Fig. 10b - Switching Time Waveforms

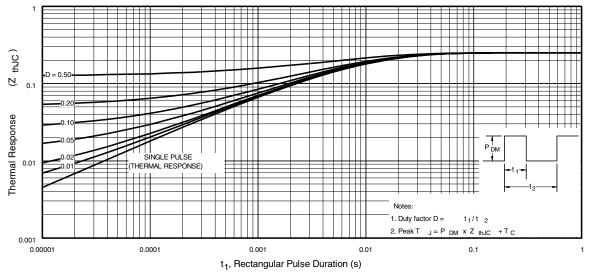


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



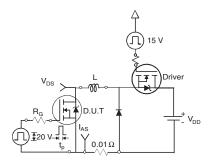


Fig. 12a - Unclamped Inductive Test Circuit

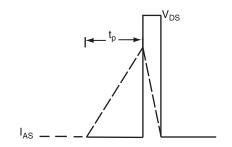


Fig. 12b - Unclamped Inductive Waveforms

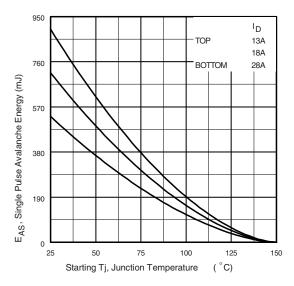


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

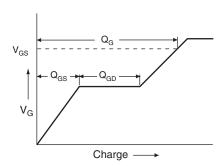


Fig. 13a - Basic Gate Charge Waveform

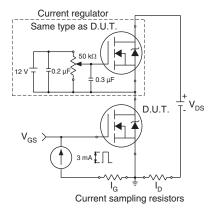
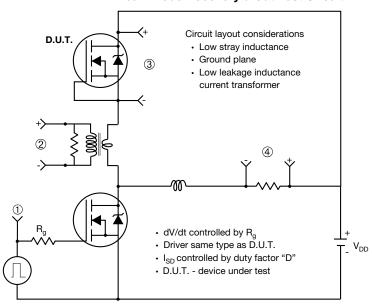


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



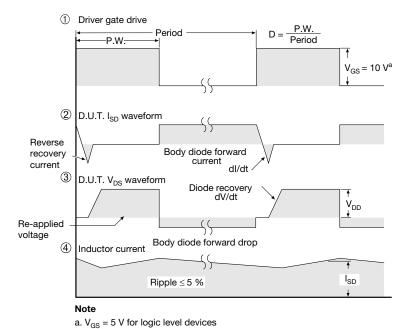


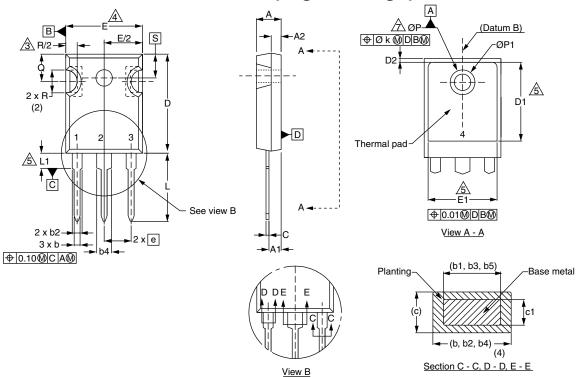
Fig. 14 - For N-Channel

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www.vishay.com

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TO-247AC (High Voltage)



	MILLIM	IETERS	INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	4.58	5.31	0.180	0.209	
A1	2.21	2.59	0.087	0.102	
A2	1.17	2.49	0.046	0.098	
b	0.99	1.40	0.039	0.055	
b1	0.99	1.35	0.039	0.053	
b2	1.53	2.39	0.060	0.094	
b3	1.65	2.37	0.065	0.093	
b4	2.42	3.43	0.095	0.135	
b5	2.59	3.38	0.102	0.133	
С	0.38	0.86	0.015	0.034	
c1	0.38	0.76	0.015	0.030	
D	19.71	20.82	0.776	0.820	
D1	13.08	-	0.515	-	
FON V40 0407 Pr. P. 04 0 40					

	MILLIMETERS		INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
D2	0.51	1.30	0.020	0.051	
Е	15.29	15.87	0.602	0.625	
E1	13.72	-	0.540	-	
е	5.46	BSC	0.215 BSC		
Øk	0.2	0.254		0.010	
L	14.20	16.25	0.559	0.640	
L1	3.71	4.29	0.146	0.169	
N	7.62 BSC		0.300 BSC		
ØΡ	3.51	3.66	0.138	0.144	
Ø P1	-	7.39	-	0.291	
Q	5.31	5.69	0.209	0.224	
R	4.52	5.49	0.178	0.216	
S	5.51 BSC		0.217	BSC	

ECN: X12-0167-Rev. B, 24-Sep-12

DWG: 5971

Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Contour of slot optional.
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- 4. Thermal pad contour optional with dimensions D1 and E1.
- 5. Lead finish uncontrolled in L1.
- 6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
- 7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
- 8. Xian and Mingxin actually photo.



Revision: 24-Sep-12 Document Number: 91360



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