

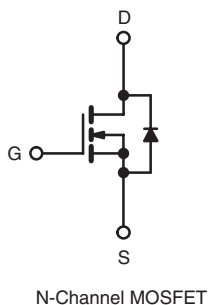
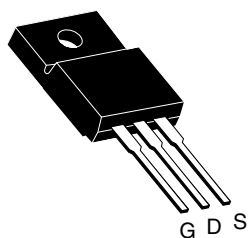


## Power MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	650	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.93
$Q_g$ (Max.) (nC)	48	
$Q_{gs}$ (nC)	12	
$Q_{gd}$ (nC)	19	
Configuration	Single	

TO-220 FULLPAK



## FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC

RoHS\*  
COMPLIANT

## APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> ( $t = 60$  s,  $f = 60$  Hz)

## TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback
- Single Transistor Forward

## ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIB5N65APbF SiHFIB5N65A-E3
SnPb	IRFIB5N65A SiHFIB5N65A

ABSOLUTE MAXIMUM RATINGS  $T_C = 25^\circ\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current <sup>e</sup>	$I_D$	$T_C = 25^\circ\text{C}$	A
Continuous Drain Current		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	21	
Linear Derating Factor		0.48	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	325	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	5.2	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	6	mJ
Maximum Power Dissipation	$P_D$	60	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>	$dV/dt$	2.8	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s	300	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

## Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 24$  mH,  $R_G = 25\ \Omega$ ,  $I_{AS} = 5.2$  A (see fig. 12).
- $I_{SD} \leq 5.2$  A,  $dI/dt \leq 90$  A/ $\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- 1.6 mm from case.
- Drain current limited by maximum junction temperature.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	2.1	

**SPECIFICATIONS**  $T_J = 25\text{ °C}$ , unless otherwise noted

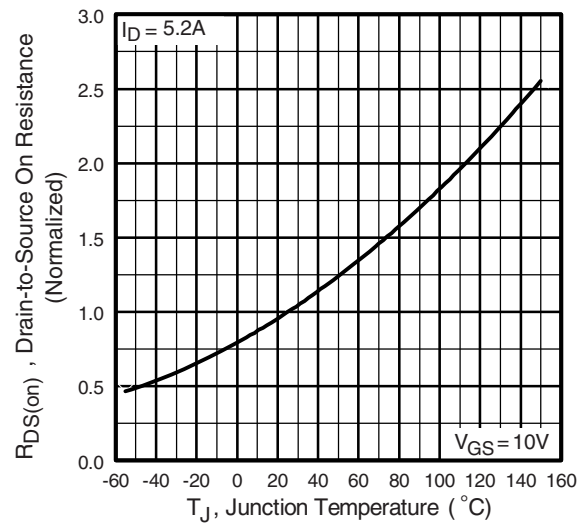
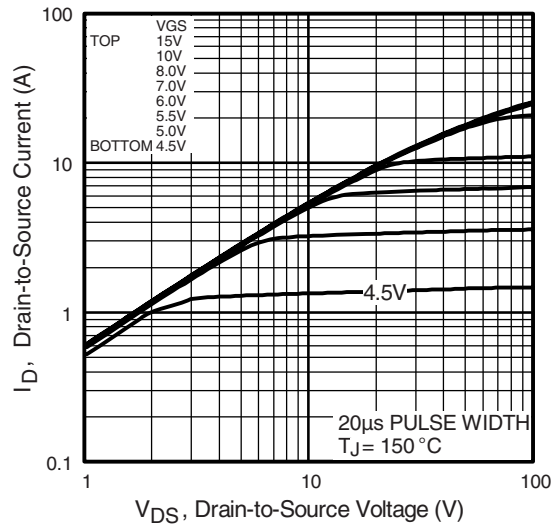
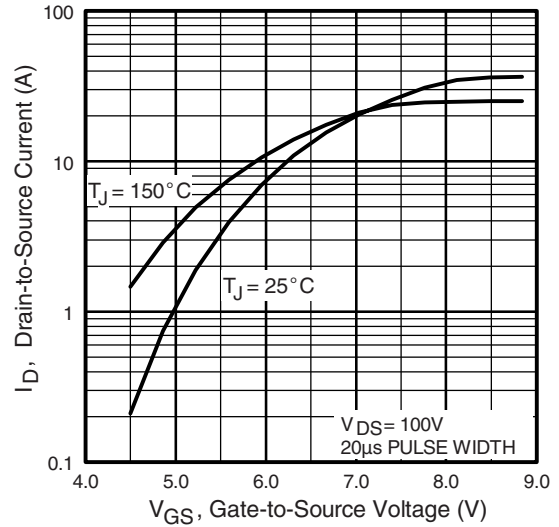
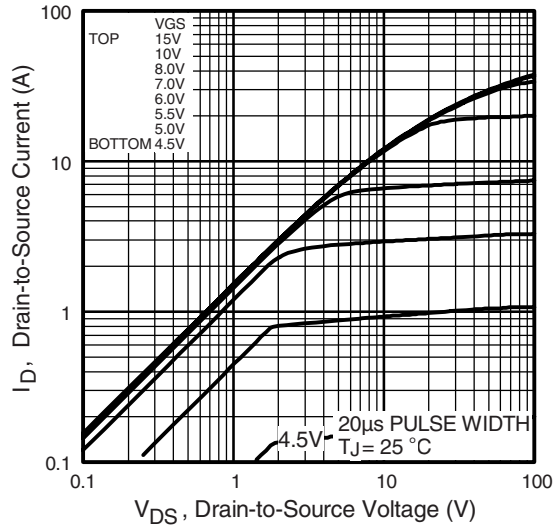
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA <sup>d</sup>		-	670	-	mV/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.1 A <sup>b</sup>	-	-	0.93	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 3.1 A		3.9	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	1417	-	pF
Output Capacitance	C <sub>oss</sub>			-	177	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	7.0	-	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 1.0 V, f = 1.0 MHz	-	1912	-	
Effective Output Capacitance	C <sub>oss eff.</sub>		V <sub>DS</sub> = 520 V, f = 1.0 MHz	-	48	-	
		V <sub>DS</sub> = 0 V to 520 V <sup>c</sup>		-	84	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 5.2 A, V <sub>DS</sub> = 400 V see fig. 6 and 13 <sup>b</sup>	-	-	48	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	12	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	19	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 325 V, I <sub>D</sub> = 5.2 A R <sub>G</sub> = 9.1 Ω, R <sub>D</sub> = 62 Ω, see fig. 10 <sup>b</sup>		-	14	-	ns
Rise Time	t <sub>r</sub>			-	20	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	34	-	
Fall Time	t <sub>f</sub>			-	18	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	5.2	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	21	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 5.2 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 5.2 A, dI/dt = 100 A/μs <sup>b</sup>		-	493	739	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	2.1	3.2	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .
- $t = 60\text{ s}$ ,  $f = 60\text{ Hz}$ .



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



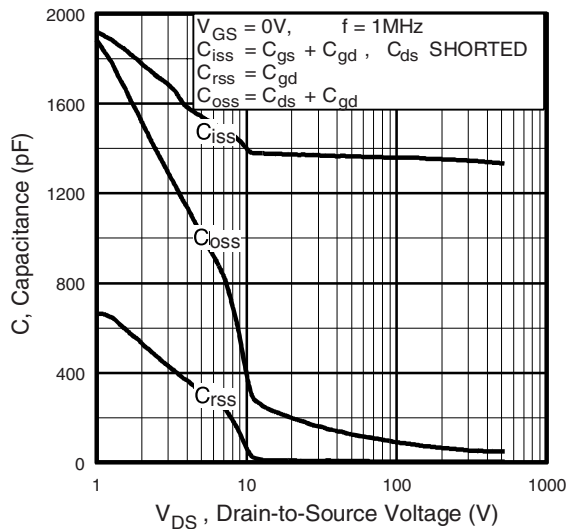


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

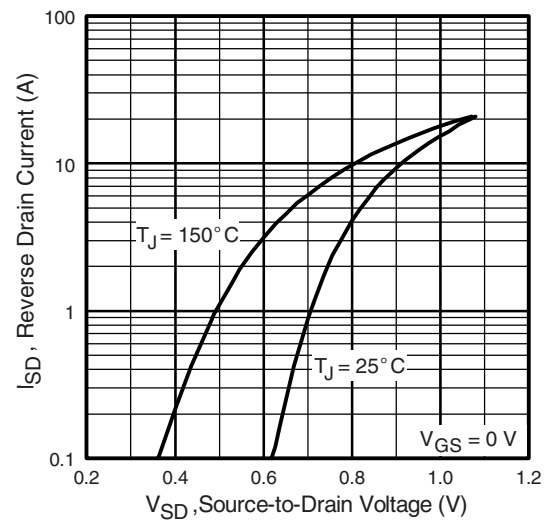


Fig. 7 - Typical Source-Drain Diode Forward Voltage

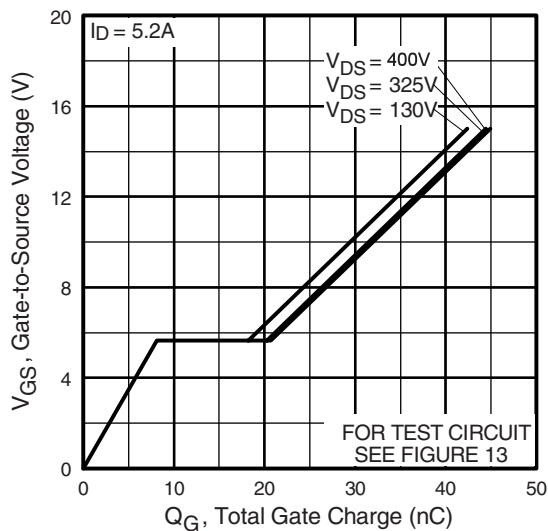


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

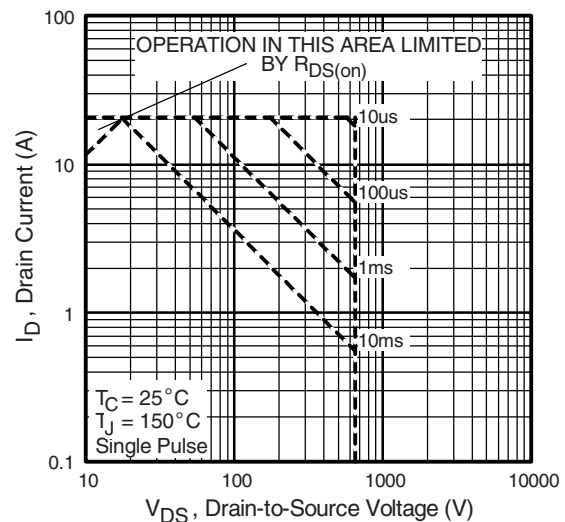


Fig. 8 - Maximum Safe Operating Area

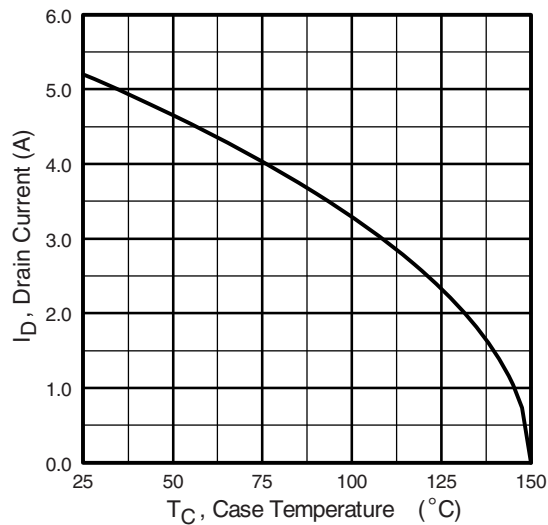


Fig. 9 - Maximum Drain Current vs. Case Temperature

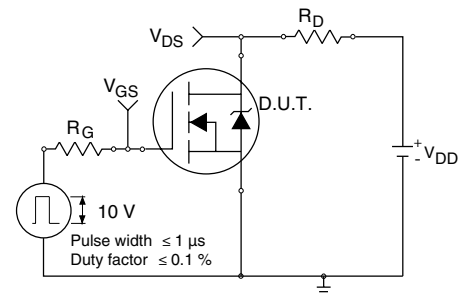


Fig. 10a - Switching Time Test Circuit

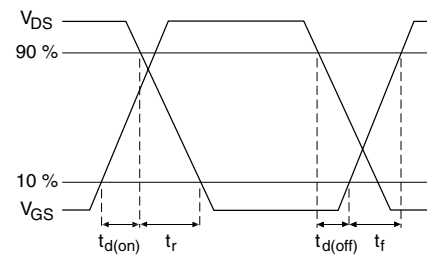


Fig. 10b - Switching Time Waveforms

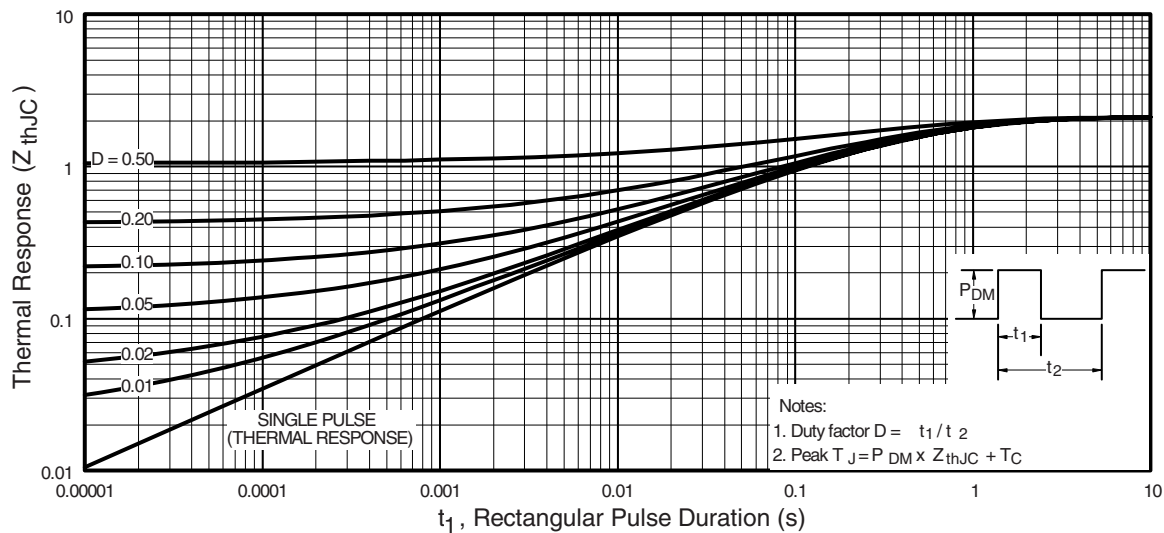


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

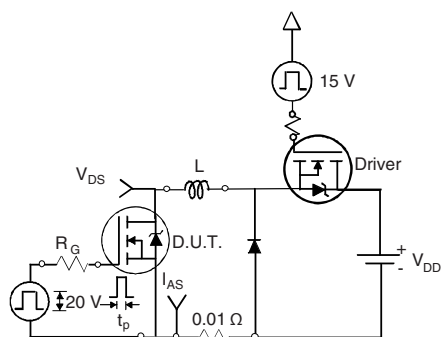


Fig. 12a - Unclamped Inductive Test Circuit

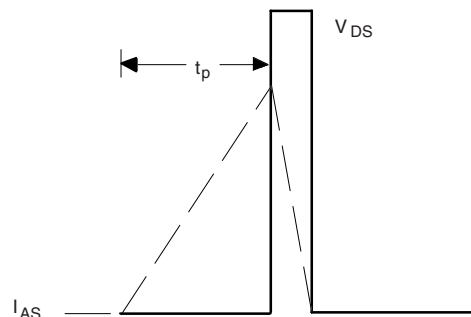


Fig. 12b - Unclamped Inductive Waveforms

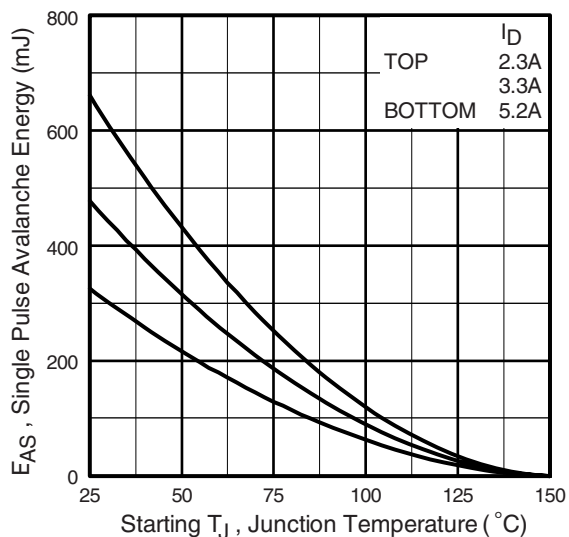


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

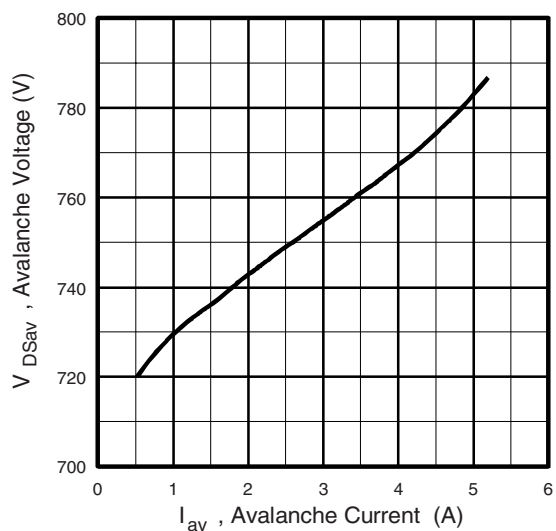


Fig. 12d - Typical Drain-to Source Voltage vs. Avalanche Current

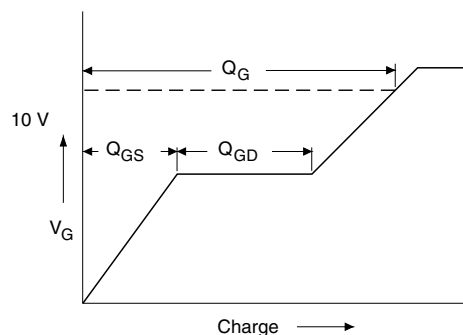


Fig. 13a - Basic Gate Charge Waveform

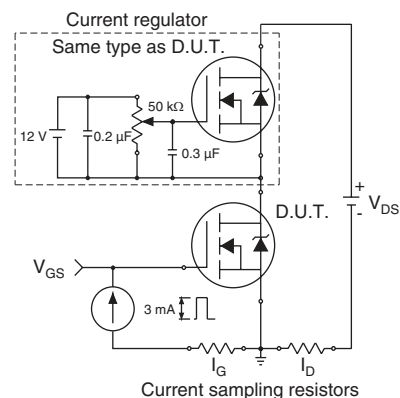
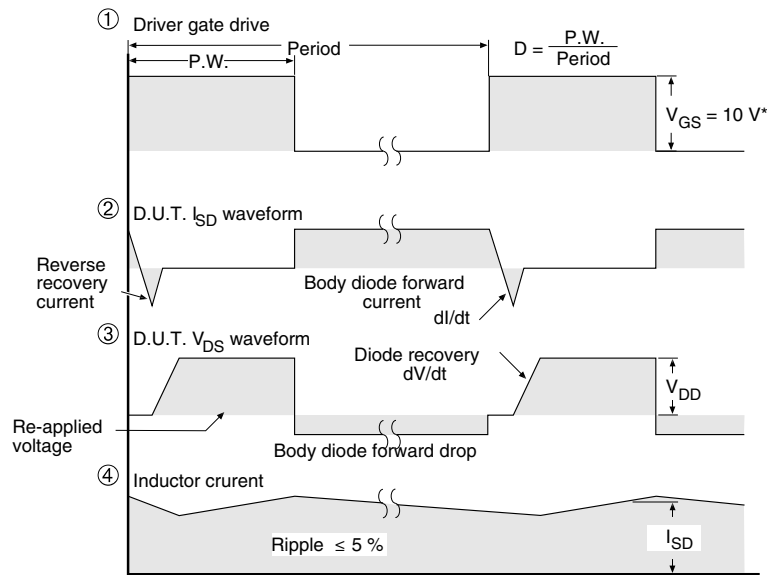
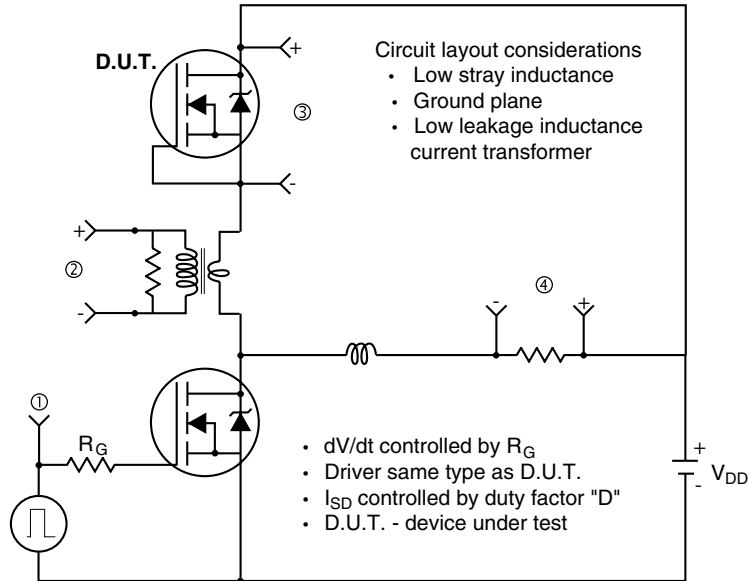


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 14 - For N-Channel

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