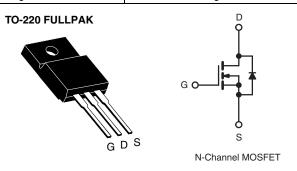


Vishay Siliconix

### **Power MOSFET**

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	600			
$R_{DS(on)}\left(\Omega\right)$	V <sub>GS</sub> = 10 V	0.75		
Q <sub>g</sub> (Max.) (nC)	49			
Q <sub>gs</sub> (nC)	13			
Q <sub>gd</sub> (nC)	20			
Configuration	Single			



#### **FEATURES**

• Low Gate Charge Q<sub>g</sub> Results in Simple Drive Requirement



• Improved Gate, Avalanche and Dynamic dV/dt RoHS Ruggedness

- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC

#### **APPLICATIONS**

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- · High Speed Power Switching
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> (t = 60 s, f = 60 Hz)

#### **TYPICAL SMPS TOPOLOGIES**

- · Single Transistor Forward
- · Active Clamped Forward

ORDERING INFORMATION			
Package	TO-220 FULLPAK		
Load (Dh.) free	IRFIB6N60APbF		
Lead (Pb)-free	SiHFIB6N60A-E3		
SnPb	IRFIB6N60A		
ו אורט	SiHFIB6N60A		

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_C = 25$ °C, unless otherw PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			$V_{DS}$	600	V	
Gate-Source Voltage			V <sub>GS</sub>	± 30	V	
Continuous Drain Current	V <sub>GS</sub> at 10 V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$	1	5.5		
		T <sub>C</sub> = 100 °C	I <sub>D</sub>	3.5		
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	37		
Linear Derating Factor				0.48	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	290	mJ	
Repetitive Avalanche Currenta			I <sub>AR</sub>	9.2	Α	
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	6.0	mJ	
Maximum Power Dissipation	T <sub>C</sub> =	25 °C	P <sub>D</sub>	60	W	
Peak Diode Recovery dV/dtc			dV/dt	5.0	V/ns	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw			10	lbf ⋅ in	
				1.1	N · m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Starting T $_J$  = 25 °C, L = 6.8 mH, R $_G$  = 25  $\Omega$ , I $_{AS}$  = 9.2 A (see fig. 12). c. I $_{SD}$  ≤ 9.2 A, dl/dt ≤ 50 A/ $\mu$ s, V $_{DD}$  ≤ V $_{DS}$ , T $_J$  ≤ 150 °C. d. 1.6 mm from case.

<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply

# IRFIB6N60A, SiHFIB6N60A

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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	65	°C/W	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	2.1	C/VV	

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		600	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I <sub>D</sub> = 1 mA <sup>d</sup>		-	660	-	mV/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	,	V <sub>GS</sub> = ± 30 V		-	± 100	nA
Zero Gate Voltage Drain Current	l	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$		-	-	25	μΑ
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>GS</sub> = 10 V I <sub>D</sub> = 3.3 A <sup>b</sup>		-	0.75	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 5.5 A		5.5	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ $f = 1.0 \text{ MHz, see fig. 5}$		ı	1400	-	- -
Output Capacitance	$C_{oss}$			i	180	-	
Reverse Transfer Capacitance	$C_{rss}$			ı	7.1	-	
Output Canacitance	<u></u>		V <sub>DS</sub> = 1.0 V, f = 1.0 MHz	ı	1957	-	pF
Output Capacitance	$C_{oss}$	$V_{GS} = 0 V$	V <sub>DS</sub> = 480 V, f = 1.0 MHz	ı	49	-	
Effective Output Capacitance	Coss eff.	V <sub>DS</sub> = 0 V to 480 V <sup>c</sup>		ı	96	-	
Total Gate Charge	$Q_g$		I <sub>D</sub> = 9.2 A, V <sub>DS</sub> = 400 V, see fig. 6 and 13 <sup>b</sup>	-	-	49	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V		-	-	13	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	20	
Turn-On Delay Time	t <sub>d(on)</sub>		V <sub>DD</sub> = 300 V, I <sub>D</sub> = 9.2 A,		13	-	ns
Rise Time	t <sub>r</sub>				25	-	
Turn-Off Delay Time	t <sub>d(off)</sub>	$R_G = 9.1 \ \Omega, \ R_D = 35.5 \ \Omega,$ see fig. $10^b$		-	30	-	
Fall Time	t <sub>f</sub>			-	22	-	
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		ı	-	5.5	- A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	37	
Body Diode Voltage	$V_{SD}$	$T_J = 25  ^{\circ}\text{C}, \ I_S = 9.2  \text{A}, \ V_{GS} = 0  \text{V}^{\text{b}}$		ı	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	- T <sub>J</sub> = 25 °C, I <sub>F</sub> = 9.2 A, dI/dt = 100 A/μs <sup>b</sup>		ı	530	800	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	3.0	4.4	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic tu	ırn-on time is negligible (turn-	on is don	ninated by	L <sub>S</sub> and I	L <sub>D</sub> )

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300~\mu s;$  duty cycle  $\leq 2~\%.$
- c.  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .
- d. t = 60 s, f = 60 Hz.





#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

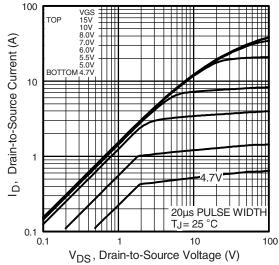


Fig. 1 - Typical Output Characteristics

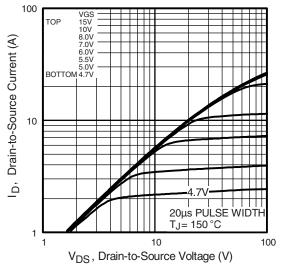


Fig. 2 - Typical Output Characteristics

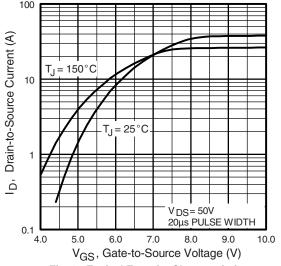


Fig. 3 - Typical Transfer Characteristics

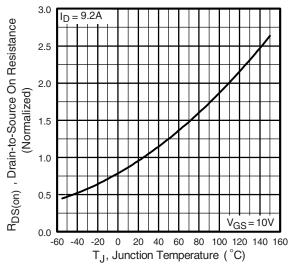


Fig. 4 - Normalized On-Resistance vs. Temperature

### IRFIB6N60A, SiHFIB6N60A

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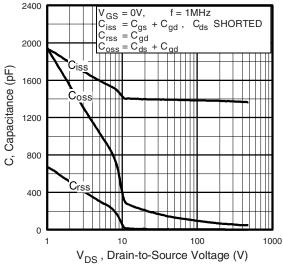


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

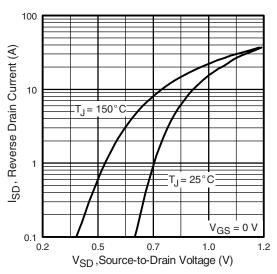


Fig. 7 - Typical Source-Drain Diode Forward Voltage

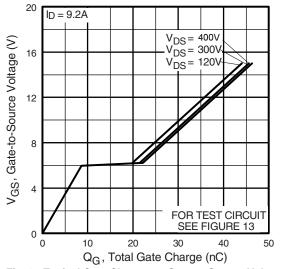


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

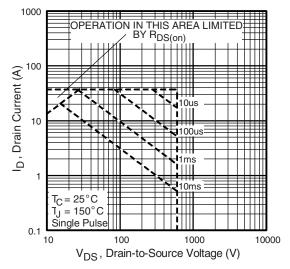


Fig. 8 - Maximum Safe Operating Area





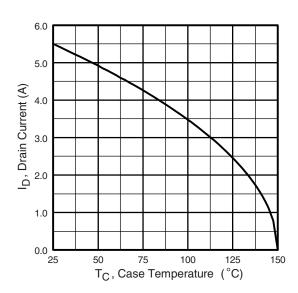


Fig. 9 - Maximum Drain Current vs. Case Temperature

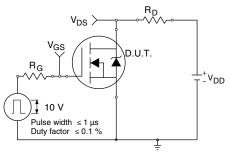


Fig. 10a - Switching Time Test Circuit

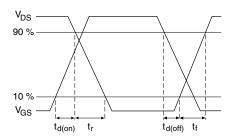


Fig. 10b - Switching Time Waveforms

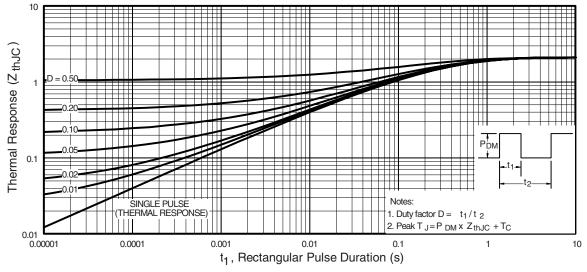


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

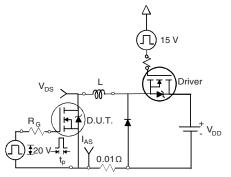


Fig. 12a - Unclamped Inductive Test Circuit

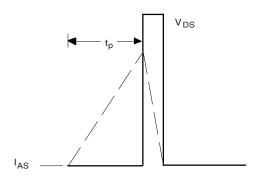


Fig. 12b - Unclamped Inductive Waveforms

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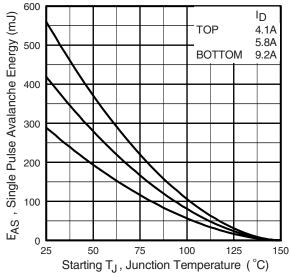


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

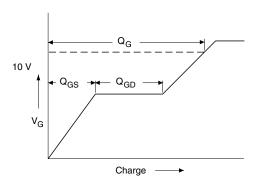


Fig. 13a - Basic Gate Charge Waveform

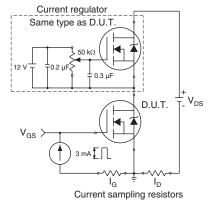
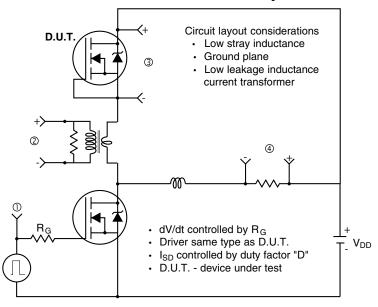
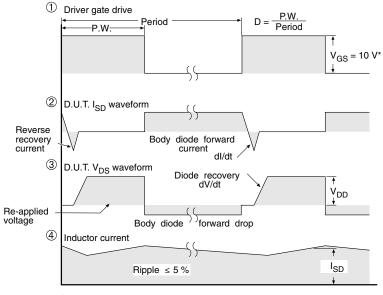


Fig. 13b - Gate Charge Test Circuit



### Peak Diode Recovery dV/dt Test Circuit





\* V<sub>GS</sub> = 5 V for logic level devices

Fig. 14 - For N-Channel

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