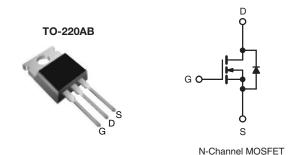


Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	400			
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V 0.55			
Q _g (Max.) (nC)	63			
Q _{gs} (nC)	9.0			
Q _{gd} (nC)	32			
Configuration	Single			



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- · Fast Switching
- · Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF740PbF
Leau (Fb)-free	SiHF740-E3
SnPb	IRF740
SHED	SiHF740

ABSOLUTE MAXIMUM RATINGS (T _C	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V_{DS}	400		
Gate-Source Voltage			V_{GS}	± 20	V	
Continuous Drain Current	T _C = 25 °C		10			
Continuous Drain Current	V _{GS} at 10 V	$T_C = 25 \degree C$ $T_C = 100 \degree C$	I _D	6.3	Α	
Pulsed Drain Current ^a			I _{DM}	40		
Linear Derating Factor				1.0	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	520	mJ	
Repetitive Avalanche Current ^a			I _{AR}	10	Α	
Repetitive Avalanche Energy ^a			E _{AR}	13	mJ	
Maximum Power Dissipation $T_C = 25 ^{\circ}C$			P_{D}	125	W	
Peak Diode Recovery dV/dt ^c			dV/dt	4.0	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	- °C	
Soldering Recommendations (Peak Temperature) for 10 s				300 ^d	7	
Mounting Torque	6-32 or M3 screw			10	lbf ⋅ in	
Mounting Torque				1.1	N · m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, L = 9.1 mH, $R_q = 25$ Ω , $I_{AS} = 10$ A (see fig. 12).
- c. $I_{SD} \le 10 \text{ A}$, $dI/dt \le 120 \text{ A/}\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_{J} \le 150 \,^{\circ}\text{C}$.
- d. 1.6 mm from case.

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	62	
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.50	-	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.0	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$) V, I _D = 250 μA	400	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	to 25 °C, I _D = 1 mA	-	0.49	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V$	' _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	VG	_{SS} = ± 20 V	-	-	± 100	nA
Zoro Coto Voltago Drain Current	1	V _{DS} = 400 V, V _{GS} = 0 V		-	-	25	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 320 V, V	V _{GS} = 0 V, T _J = 125 °C	-	-	250	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 6.0 A ^b	-	-	0.55	Ω
Forward Transconductance	9 _{fs}	$V_{DS} = 5$	60 V, I _D = 6.0 A ^b	5.8	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V	$t_{GS} = 0 \text{ V},$	1	1400	-	
Output Capacitance	C _{oss}	V	$V_{DS} = 0 V$, $V_{DS} = 25 V$,		330	-	pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0	MHz, see fig. 5	1	120	-	
Total Gate Charge	Qg		1 10 A V 220 V	ı	-	63	nC
Gate-Source Charge	Q_{gs}	$V_{GS} = 10 \text{ V}$	$I_D = 10 \text{ A}, V_{DS} = 320 \text{ V},$ see fig. 6 and 13 ^b	-	-	9.0	
Gate-Drain Charge	Q_{gd}		see lig. 6 and 13°	-	-	32	
Turn-On Delay Time	t _{d(on)}			-	14	-	
Rise Time	t _r	V _{DD} = 200 V, I _D = 10 A		-	27	-	
Turn-Off Delay Time	t _{d(off)}	$R_g = 9.1 \Omega$, $R_D = 20 \Omega$, see fig. 10^b		-	50	-	ns -
Fall Time	t _f			-	24	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	
Internal Source Inductance	L _S			-	7.5	-	nH
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	1	MOSFET symbol		-	10	
Pulsed Diode Forward Current ^a	I _{SM}	showing the integral reverse p - n junction diode		-	-	40	А
Body Diode Voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 10 \text{A}, V_{GS} = 0 \text{V}^{\text{b}}$		-	-	2.0	V
Body Diode Reverse Recovery Time	t _{rr}	$T_J = 25 \text{ °C}, I_F = 10 \text{ A, dl/dt} = 100 \text{ A/µs}^b$		-	370	790	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	3.8	8.2	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)			1 _\		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

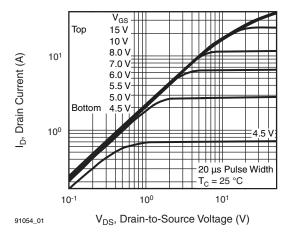


Fig. 1 - Typical Output Characteristics, $T_C = 25$ °C

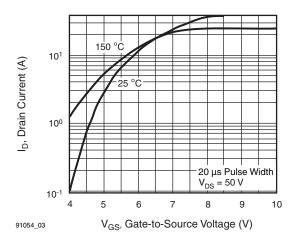


Fig. 3 - Typical Transfer Characteristics

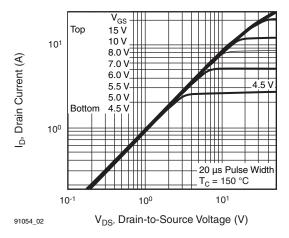


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

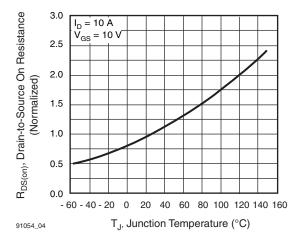
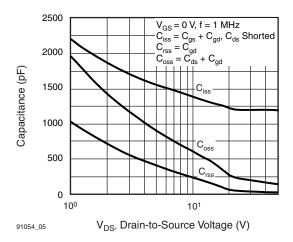


Fig. 4 - Normalized On-Resistance vs. Temperature





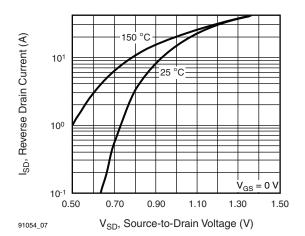
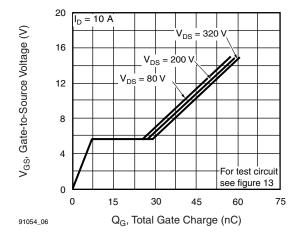


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage



 10^{3} Operation in this area limited by R_{DS(on} 10² ID, Drain Current (A) 2 10 1 T_C = 25 °C 5 = 150 °C 2 Single Pulse 0.1 10 0.1 V_{DS}, Drain-to-Source Voltage (V) 91054_08

Fig. 6 - Typical Gate Charge vs. Drain-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area





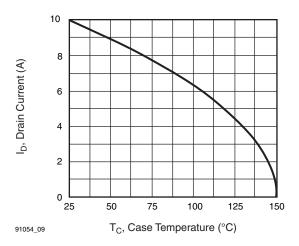


Fig. 9 - Maximum Drain Current vs. Case Temperature

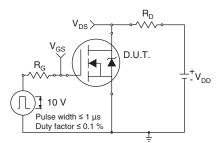


Fig. 10a - Switching Time Test Circuit

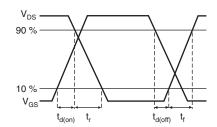


Fig. 10b - Switching Time Waveforms

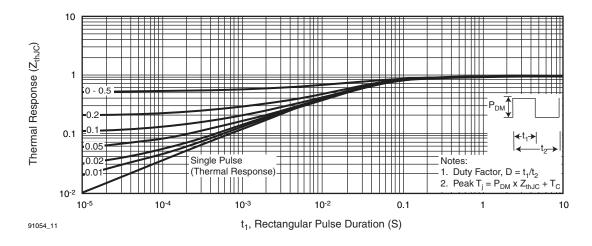


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



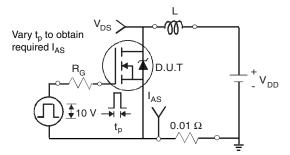


Fig. 12a - Unclamped Inductive Test Circuit

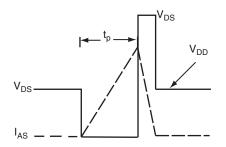


Fig. 12b - Unclamped Inductive Waveforms

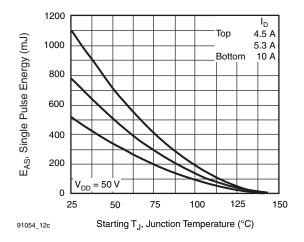


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

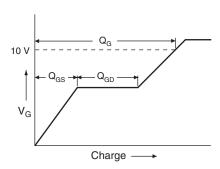


Fig. 13a - Basic Gate Charge Waveform

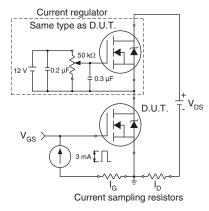
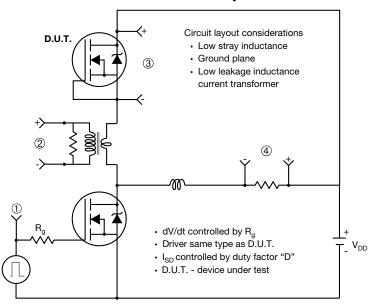


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



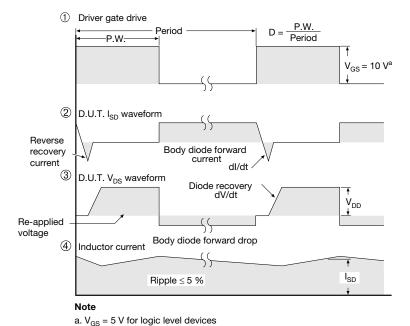


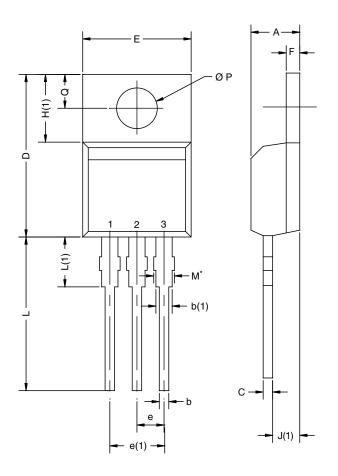
Fig. 14 - For N-Channel

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TO-220AB



	MILLIN	METERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
E	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØР	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
	0208-Rev. N,		0.102	0.118	

Notes

- * M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM
- · Xi'an and Mingxin actual photo





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