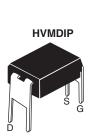
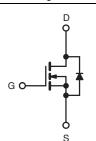
Vishay Siliconix

COMPLIANT

# **Power MOSFET**

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	100				
$R_{DS(on)}(\Omega)$	$V_{GS} = 5.0 \text{ V}$	0.54			
Q <sub>g</sub> (Max.) (nC)	6.1				
Q <sub>gs</sub> (nC)	2.6				
Q <sub>gd</sub> (nC)	3.3				
Configuration	Single				





N-Channel MOSFET

#### **FEATURES**

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- Logic-Level Gate Drive
- R<sub>DS(on)</sub> Specified at V<sub>GS</sub> = 4 V and 5 V
- 175 °C Operating Temperature
- Material categorization: For definitions of compliance please see <a href="https://www.vishay.com/doc?99912">www.vishay.com/doc?99912</a>

#### Note

\* Lead (Pb)-containing terminations are not RoHS-compliant. Exemptions may apply.

#### **DESCRIPTION**

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION			
Package	HVMDIP		
Load (Ph) from	IRLD110PbF		
Lead (Pb)-free	SiHLD110-E3		
SnPb	IRLD110		
SILL	SiHLD110		

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>A</sub> = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			$V_{DS}$	100	V	
Gate-Source Voltage			$V_{GS}$	± 10	v	
Continuous Drain Current	V at 5.0.V	T <sub>A</sub> = 25 °C T <sub>A</sub> = 100 °C	- I <sub>D</sub>	1.0		
	V <sub>GS</sub> at 5.0 V	T <sub>A</sub> = 100 °C		0.70	Α	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	8.0		
Linear Derating Factor				0.0083	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	100	mJ	
Avalanche Current <sup>a</sup>			I <sub>AR</sub>	1.0	Α	
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	0.13	mJ	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C		P <sub>D</sub>	1.3	W	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	5.5	V/ns	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature)	for	for 10 s		300 <sup>d</sup>		

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b.  $V_{DD} = 25 \text{ V}$ , starting  $T_J = 25 \,^{\circ}\text{C}$ ,  $L = 6.4 \,\text{mH}$ ,  $R_g = 25 \,\Omega$ ,  $I_{AS} = 5.6 \,\text{A}$  (see fig. 12).
- c.  $I_{SD} \le 5.6$  A,  $dI/dt \le 75$  A/ $\mu$ s,  $V_{DD} \le V_{DS}$ ,  $T_J \le 175$  °C.
- d. 1.6 mm from case.



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THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	120	°C/W		

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT		
Static				L	L	L		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		100	-	-	V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I <sub>D</sub> = 1 mA	-	0.12	-	V/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	· V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0	-	2.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	,	V <sub>GS</sub> = ± 10 V	-	-	± 100	nA	
7 0 1 1/1 1 5 1 0 1	I <sub>DSS</sub>	V <sub>DS</sub> =	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V		-	25		
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 80 V	, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C	-	-	250	μA	
D : 0	_	$V_{GS} = 5.0 \text{ V}$	I <sub>D</sub> = 0.60 A <sup>b</sup>	-	-	0.54		
Drain-Source On-State Resistance	$R_{DS(on)}$	V <sub>GS</sub> = 4.0 V	I <sub>D</sub> = 0.50 A <sup>b</sup>	-	-	0.76	Ω	
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> =	50 V, I <sub>D</sub> = 0.60 A <sup>b</sup>	1.3	-	-	S	
Dynamic				I.	I.	l .		
Input Capacitance	C <sub>iss</sub>		$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ $f = 1.0 \text{ MHz}, \text{ see fig. 5}$		250	-	pF	
Output Capacitance	C <sub>oss</sub>				80	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1.			15	-		
Total Gate Charge	Qg			-	-	6.1		
Gate-Source Charge	$Q_gs$	$V_{GS} = 5.0 \text{ V}$	$I_D = 5.6 \text{ A}, V_{DS} = 80 \text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	2.6	nC	
Gate-Drain Charge	Q <sub>gd</sub>		See fig. 6 and 16	-	-	3.3		
Turn-On Delay Time	t <sub>d(on)</sub>				9.3	-	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 50 V, $I_{D}$ = 5.6 A, $R_{g}$ = 12 $\Omega$ , $R_{D}$ = 8.4 $\Omega$ , see fig. 10 <sup>b</sup>		-	4.7	-		
Turn-Off Delay Time	t <sub>d(off)</sub>			-	16	-		
Fall Time	t <sub>f</sub>			-	17	-		
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	-11	
Internal Source Inductance	L <sub>S</sub>			-	6.0	-	- nH	
Drain-Source Body Diode Characteristic	s							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	1.0	A	
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	8.0	^	
Body Diode Voltage	$V_{SD}$	T <sub>J</sub> = 25 °C	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 1.0 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	2.5	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T 05 °C !	E.C.A. dl/d+ 100 A/:h	-	110	130	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	$T_J = 25  ^{\circ}\text{C}, I_F = 5.6  \text{A},  \text{dI/dt} = 100  \text{A/} \mu \text{s}^{\text{b}}$		-	0.50	0.65	μC	
Forward Turn-On Time	t <sub>on</sub>	Intrinsic tu	rn-on time is negligible (turn	on is dor	ninated b	y L <sub>s</sub> and	L <sub>D</sub> )	

## Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width  $\leq 300~\mu s;$  duty cycle  $\leq 2~\%.$ 



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

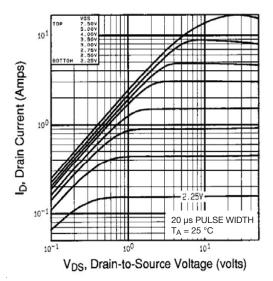


Fig. 1 - Typical Output Characteristics,  $T_A$  = 25 °C

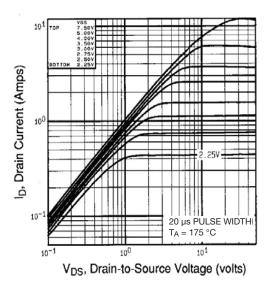


Fig. 2 - Typical Output Characteristics,  $T_A$  = 175 °C

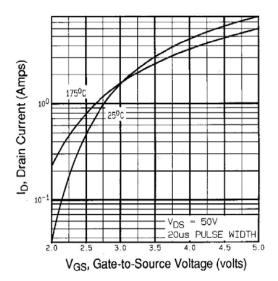


Fig. 3 - Typical Transfer Characteristics

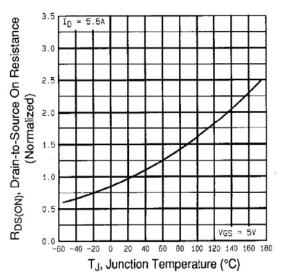


Fig. 4 - Normalized On-Resistance vs. Temperature



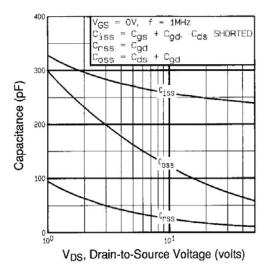


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

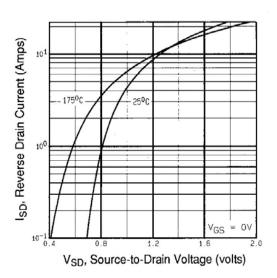


Fig. 7 - Typical Source-Drain Diode Forward Voltage

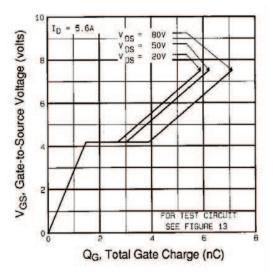


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

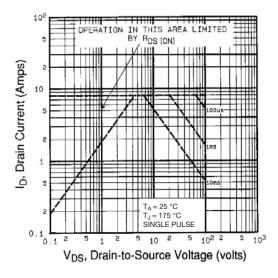


Fig. 8 - Maximum Safe Operating Area



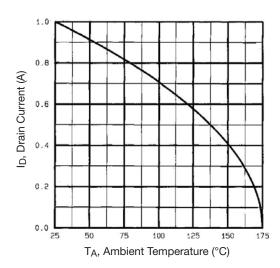


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

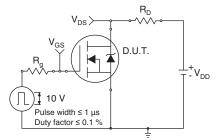


Fig. 10 - Switching Time Test Circuit

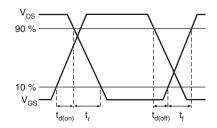


Fig. 11 - Switching Time Waveforms

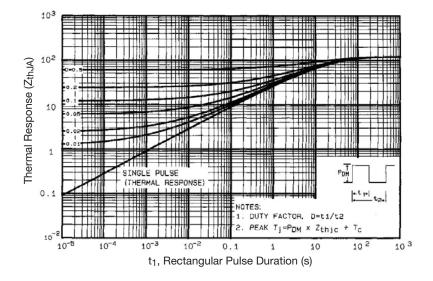


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



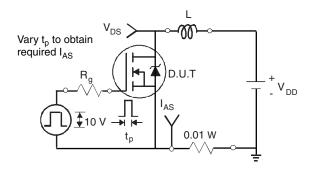


Fig. 13 - Unclamped Inductive Test Circuit

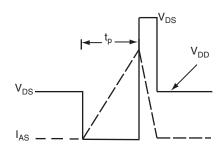


Fig. 14 - Unclamped Inductive Waveforms

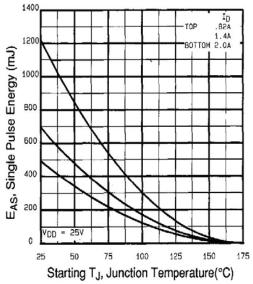


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

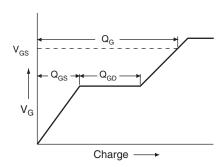


Fig. 16 - Basic Gate Charge Waveform

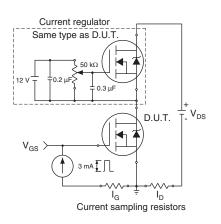
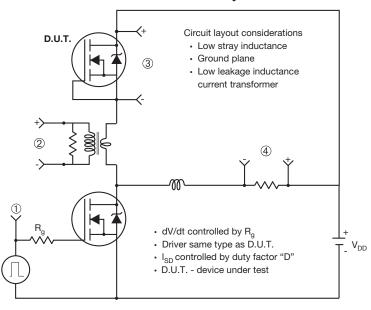


Fig. 17 - Gate Charge Test Circuit



## Peak Diode Recovery dV/dt Test Circuit



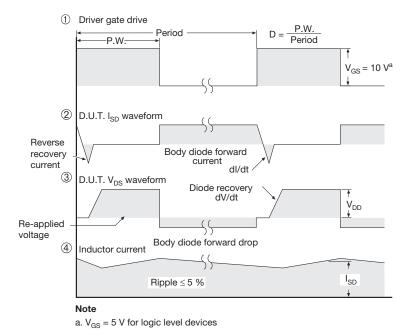


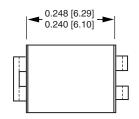
Fig. 18 - For N-Channel

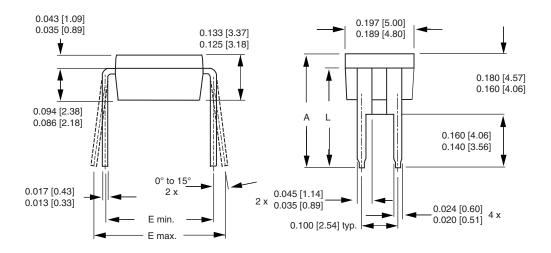
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## **HVM DIP** (High voltage)





	INCHES		INCHES MILLIMETERS		METERS
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	0.310	0.330	7.87	8.38	
E	0.300	0.425	7.62	10.79	
L	0.270	0.290	6.86	7.36	

ECN: X10-0386-Rev. B, 06-Sep-10

DWG: 5974

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

Document Number: 91361 Revision: 06-Sep-10



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