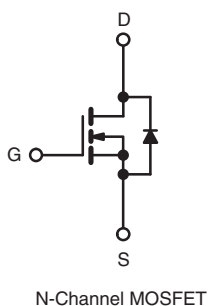
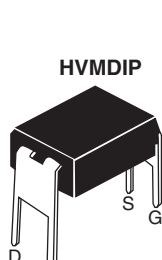


## Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	60	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 5.0$ V	0.10
$Q_g$ (Max.) (nC)	18	
$Q_{gs}$ (nC)	4.5	
$Q_{gd}$ (nC)	12	
Configuration	Single	



### FEATURES

- Dynamic dV/dt Rating
- For Automatic Insertion
- End Stackable
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS} = 4$  V and 5 V
- 175 °C Operating Temperature
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertible case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

### ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRLD024PbF SiHLD024-E3
SnPb	IRLD024 SiHLD024

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 10$	
Continuous Drain Current	$I_D$	$T_A = 25$ °C	A
		$T_A = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	20	
Linear Derating Factor		0.0083	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	91	mJ
Maximum Power Dissipation	$P_D$	1.3	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$  V, starting  $T_J = 25$  °C,  $L = 16$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 2.5$  A (see fig. 12).
- $I_{SD} \leq 17$  A,  $di/dt \leq 140$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175$  °C.
- 1.6 mm from case.


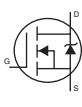
\* Pb containing terminations are not RoHS compliant, exemptions may apply



**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	120	°C/W

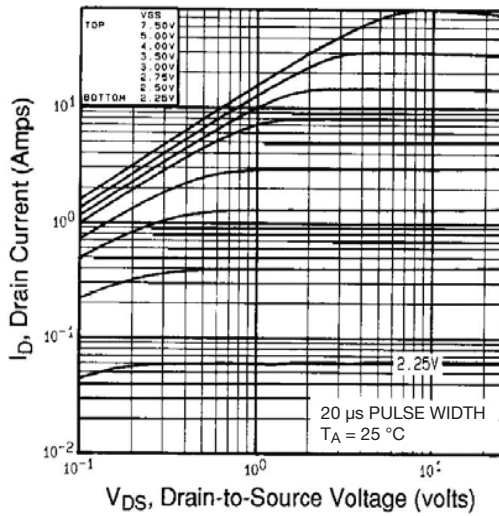
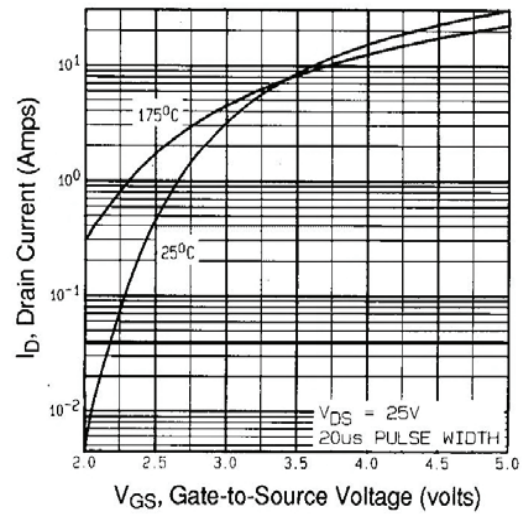
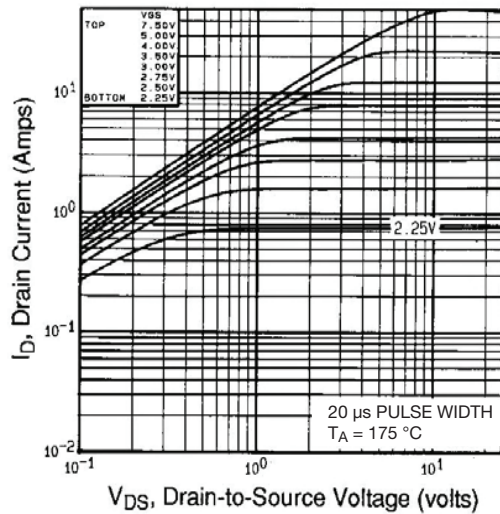
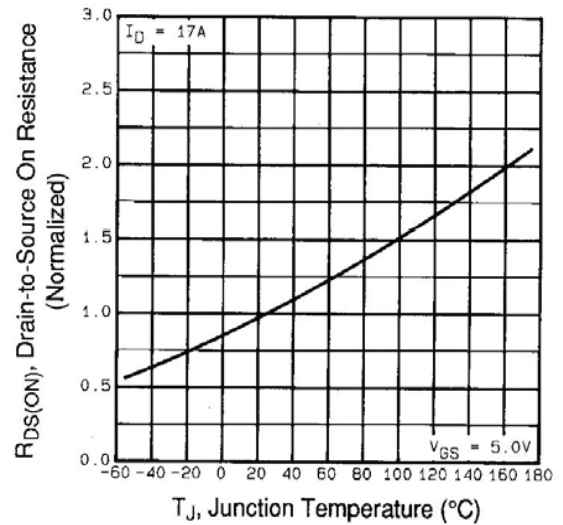
**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		60	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.060	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.0	-	2.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 10 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 5.0 V	I <sub>D</sub> = 1.5A <sup>b</sup>	-	-	0.10	Ω
		V <sub>GS</sub> = 4.0 V	I <sub>D</sub> = 1.3 A <sup>b</sup>	-	-	0.14	
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 1.5 A <sup>b</sup>		3.7	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 25 V f = 1.0 MHz, see fig. 5		-	870	-	pF
Output Capacitance	C <sub>oss</sub>			-	360	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	53	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 5.0 V	I <sub>D</sub> = 17 A, V <sub>DS</sub> = 48 V see fig. 6 and 13 <sup>b</sup>	-	-	18	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	4.5	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	12	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 17 A R <sub>g</sub> = 9.0 Ω, R <sub>D</sub> = 1.7 Ω, see fig. 10 <sup>b</sup>		-	11	-	ns
Rise Time	t <sub>r</sub>			-	110	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	23	-	
Fall Time	t <sub>f</sub>			-	41	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L <sub>S</sub>			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2.5	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	20	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 2.5 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 17 A, dI/dt = 100 A/μs <sup>b</sup>		-	110	260	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	0.49	1.5	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_A = 25^\circ C$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_A = 175^\circ C$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**



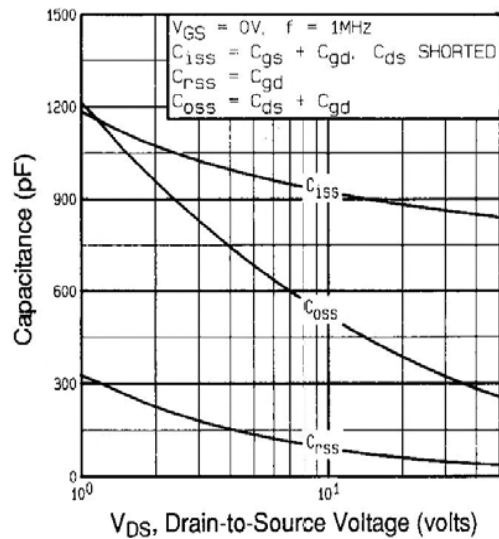


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

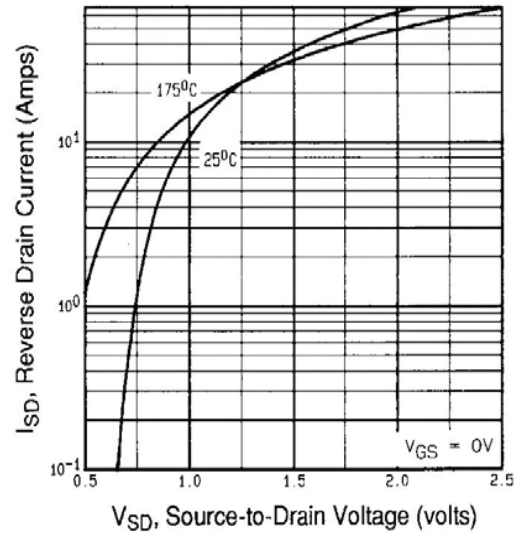


Fig. 7 - Typical Source-Drain Diode Forward Voltage

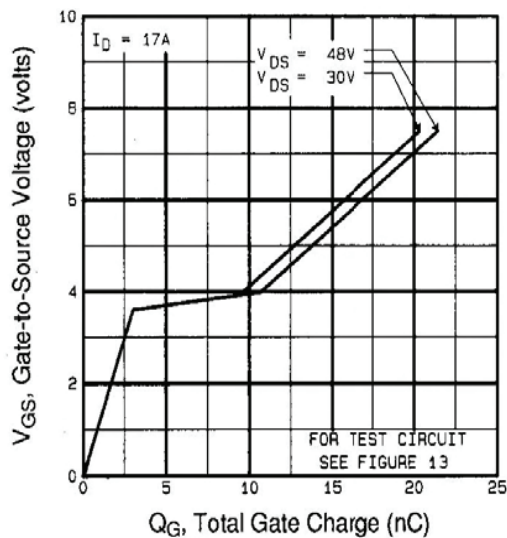


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

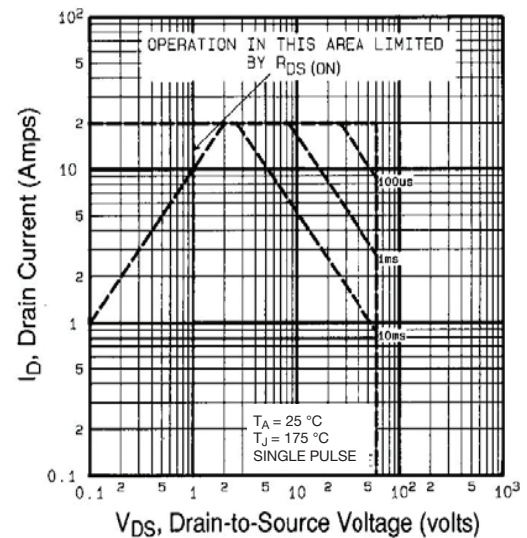
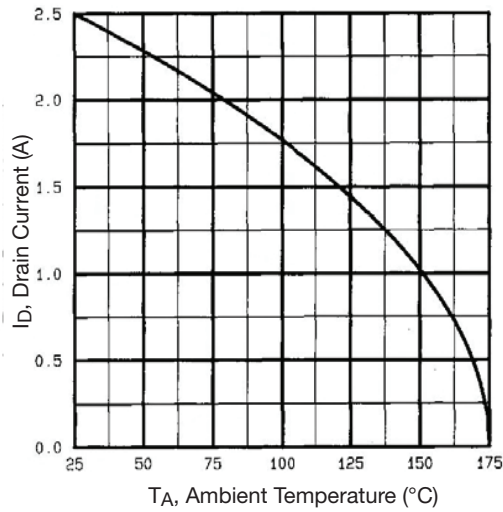
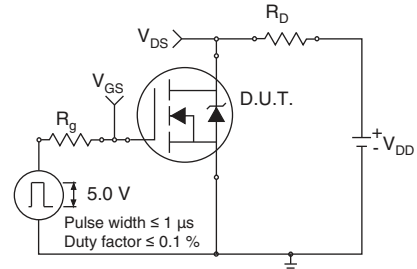
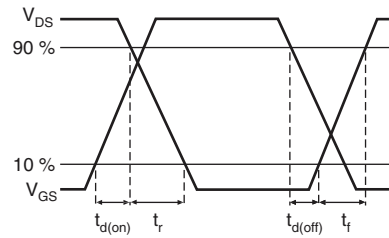
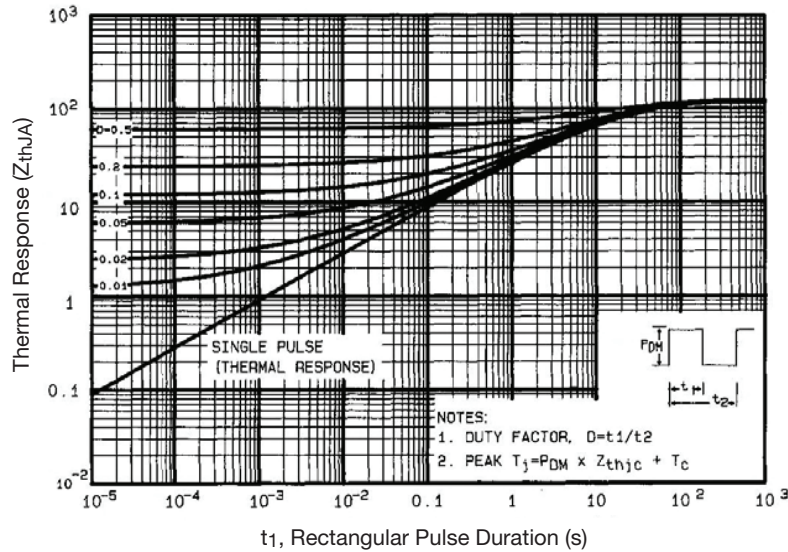


Fig. 8 - Maximum Safe Operating Area




**Fig. 9 - Maximum Drain Current vs. Ambient Temperature**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**



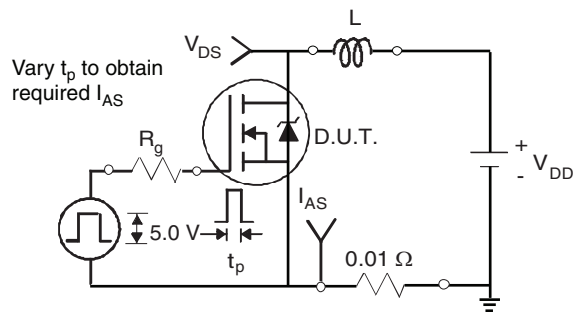


Fig. 12a - Unclamped Inductive Test Circuit

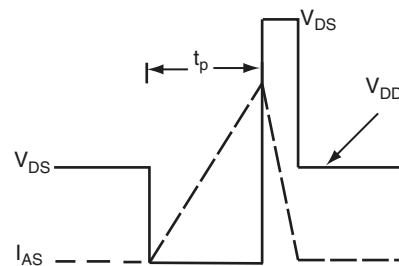


Fig. 12b - Unclamped Inductive Waveforms

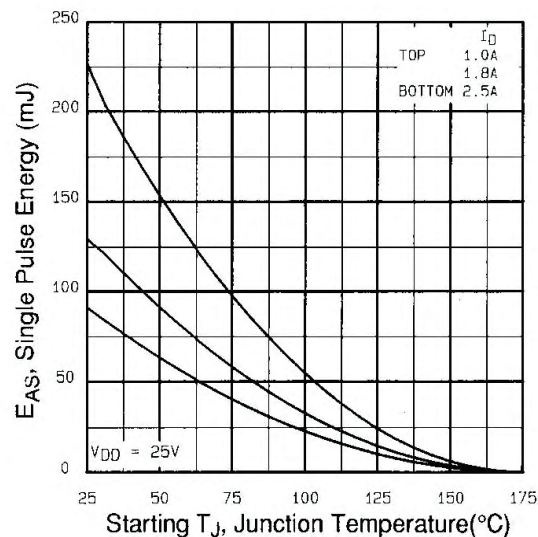


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

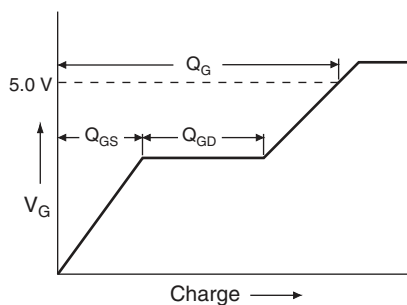


Fig. 13a - Basic Gate Charge Waveform

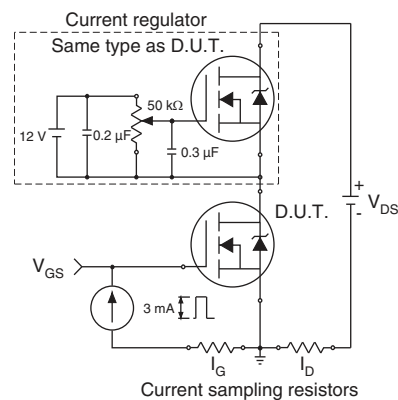
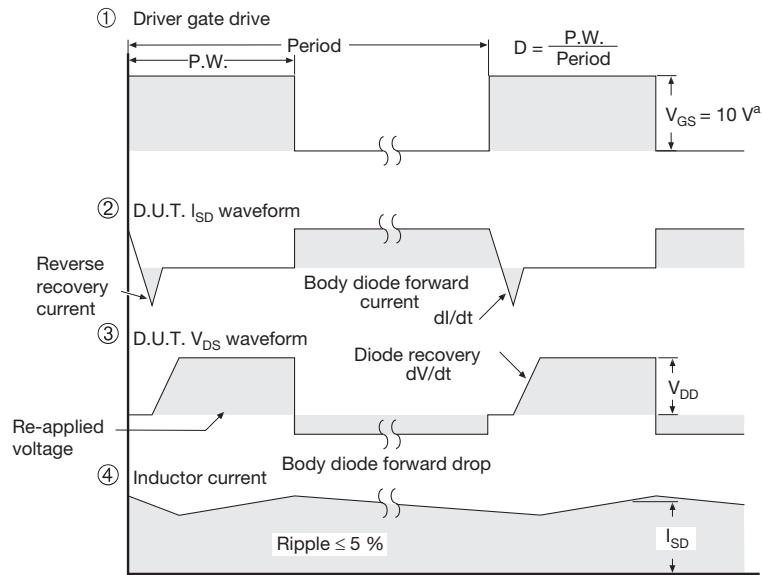
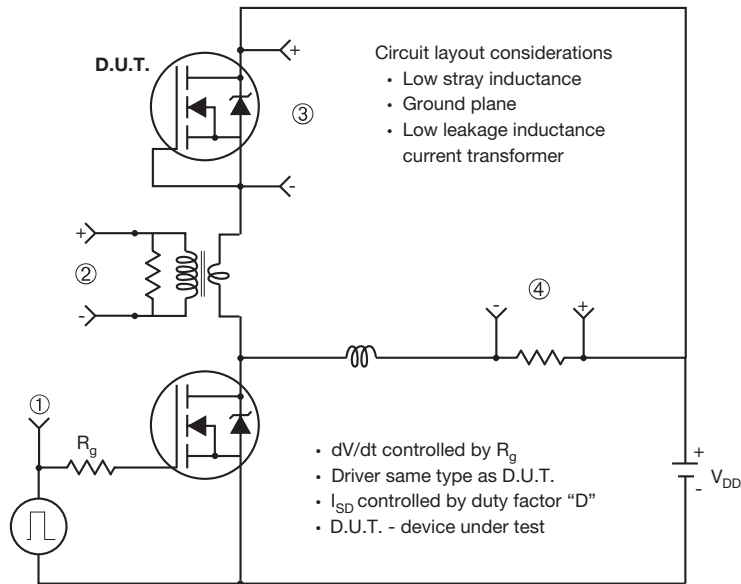


Fig. 13b - Gate Charge Test Circuit



**Peak Diode Recovery  $dV/dt$  Test Circuit**

**Note**

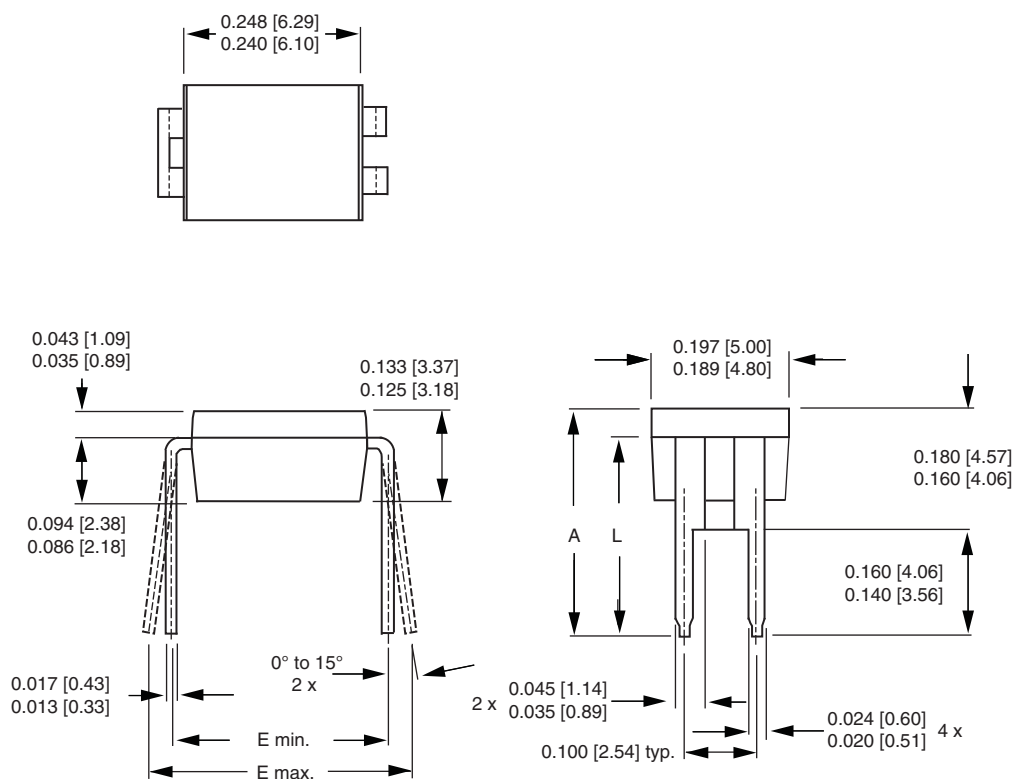
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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## HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10  
DWG: 5974

### Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.





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