



N-Channel 75-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{(BR)DSS} (V)	$r_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ)			
75	0.0062 at V _{GS} = 10 V	90 ^d	75			

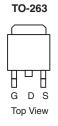
FEATURES

- TrenchFET® Power MOSFETS
- 175 °C Junction Temperature
- 100 % R_q and UIS Tested

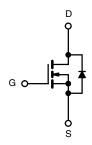


APPLICATIONS

- Power Supply
 - Secondary Synchronous Rectification
- Industrial



Ordering Information: SUM90N08-6m2P-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _C = 25 °C, unless oth	erwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	75	V		
Gate-Source Voltage	V _{GS}	± 20	7 v		
Continuous Drain Current (T _{.I} = 175 °C)	T _C = 25 °C	1-	90 ^d		
Continuous Diam Current (1 _J = 175 C)	T _C = 70 °C	I _D	90 ^d		
Pulsed Drain Current		I _{DM}	240	A	
Avalanche Current		I _{AS}	50		
Single Avalanche Energy ^a	L = 0.1 mH	E _{AS}	125	mJ	
Mariana Barra Birainatina	T _C = 25 °C	В	272 ^b	14/	
Maximum Power Dissipation ^a	T _A = 25 °C ^c	$ P_D$ $-$	3.75	W	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Unit		
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W		
Junction-to-Case (Drain)	R _{thJC}	0.55	C/VV		

Notes:

- a. Duty cycle \leq 1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).
- d. Package limited.

SUM90N08-6m2P

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SPECIFICATIONS T _{,J} = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	75			V	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.5		4.5		
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 250	nA	
		$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50	μΑ	
		$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 150 ^{\circ}\text{C}$			250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	70			Α	
Durin Course On Otata Basistana d	r	V _{GS} = 10 V, I _D = 20 A		0.0051	0.0062	0	
Drain-Source On-State Resistance ^a	^r DS(on)	V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C		0.0082	0.0105	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A		50		S	
Dynamic ^b							
Input Capacitance	C _{iss}			4620		pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 30 \text{ V}, f = 1 \text{ MHz}$		517			
Reverse Transfer Capacitance	C _{rss}			247			
Total Gate Charge ^c	Q_g			75	115		
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$		25.5		nC	
Gate-Drain Charge ^c	Q_{gd}			20			
Gate Resistance	R_g	f = 1 MHz		1.2	2.4	Ω	
Turn-On Delay Time ^c	t _{d(on)}			16	30		
Rise Time ^c	t _r	V_{DD} = 30 V, R_L = 0.6 Ω		11	20	ns	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		24	40		
Fall Time ^c	t _f			10	20		
Source-Drain Diode Ratings and Ch	aracteristics 7	_C = 25 °C ^b					
Continuous Current	Is				85	^	
Pulsed Current	I _{SM}	SM			240	Α	
Forward Voltage ^a	V_{SD}	$I_F = 20 \text{ A}, V_{GS} = 0 \text{ V}$		0.83	1.5	V	
Reverse Recovery Time	t _{rr}			60	100	ns	
Peak Reverse Recovery Current	I _{RM(REC)}	$I_F = 75 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		3.3	5	Α	
Reverse Recovery Charge	Q _{rr}			100	150	nC	

Notes:

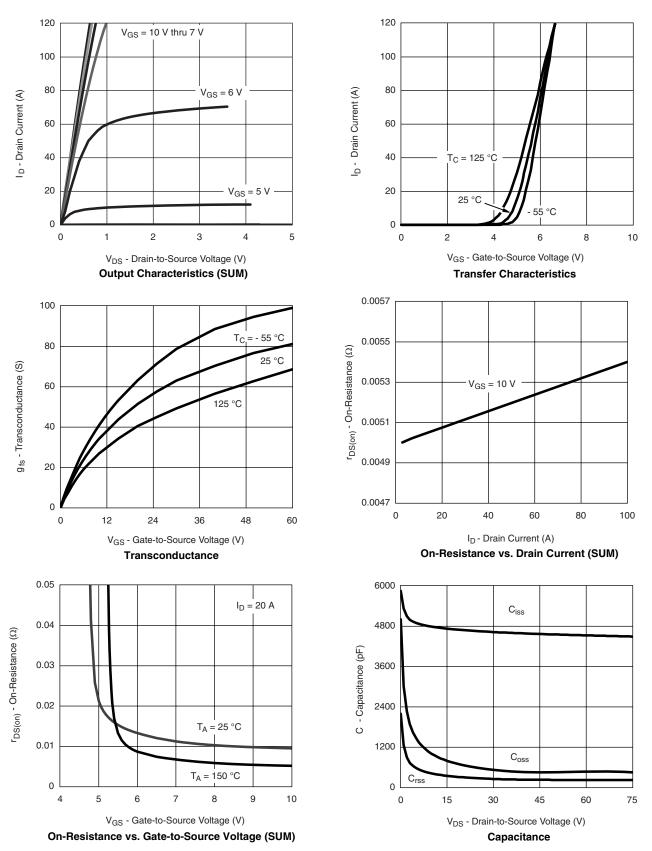
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





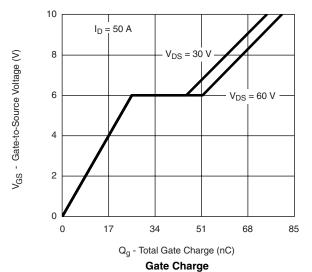
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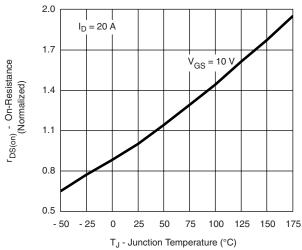


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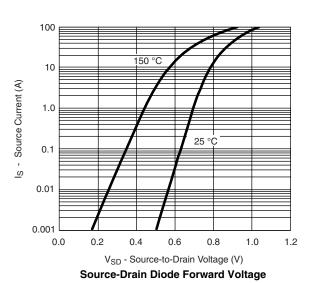
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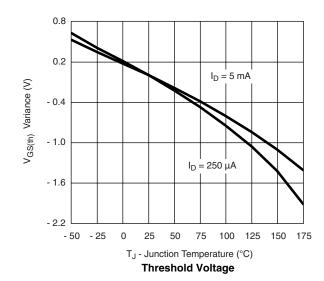
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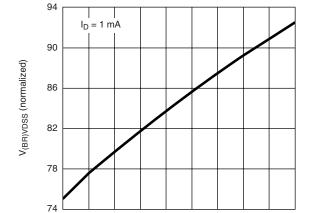


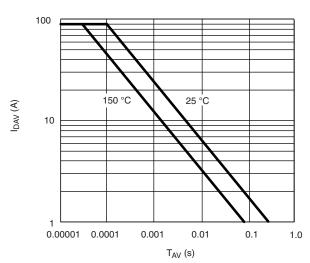


On-Resistance vs. Junction Temperature









 $\label{eq:TJ-Junction} T_{J} \text{ - Junction Temperature (°C)}$ Drain source Breakdown vs. Junction Temperature

100 125 150 175

50 75

Single Pulse Avalanche Current Capability vs. Time

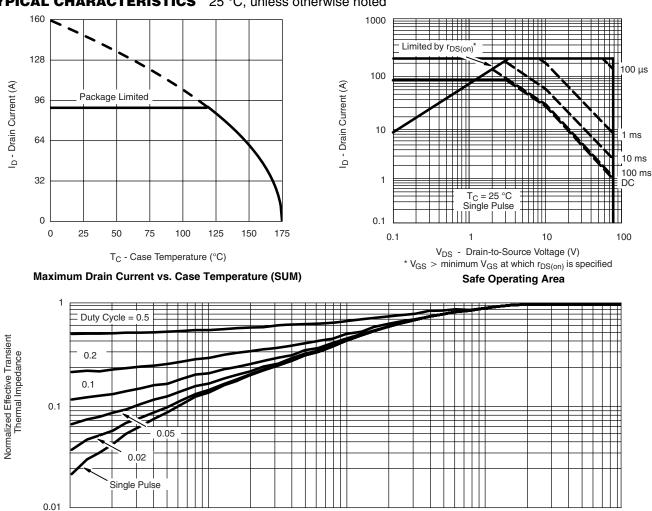
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

10-3



Square Wave Pulse Duration (s) Normalized Thermal Transient Impedance, Junction-to-Case

10-2

10-1

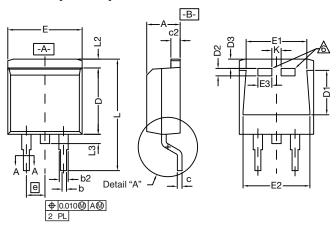
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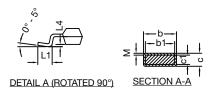
10-4





TO-263 (D²PAK): 3-LEAD





		INC	HES	MILLIN	/IETERS	
DIM.		MIN.	MAX.	MIN.	MAX.	
Α		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
	Thin lead	0.013	0.018	0.330	0.457	
C*	Thick lead	0.023	0.028	0.584	0.711	
	Thin lead	0.013	0.017	0.330	0.431	
c1	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
D		0.340	0.380	8.636	9.652	
D1		0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
	е	0.100	BSC	2.54	BSC	
	K	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
	L1	0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
L4		0.010 BSC		0.254 BSC		
	М	-	0.002	-	0.050	
	N: T10-0738-R G: 5843	ev. J, 03-Ja	n-11			

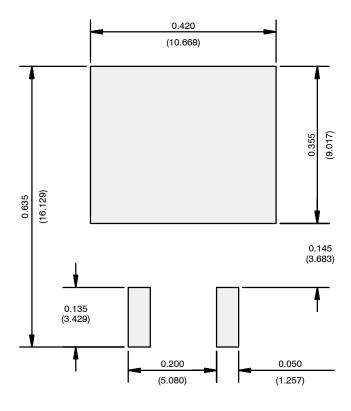
Notes

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.





RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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