



N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)			
20	0.091 at $V_{GS} = 4.5 \text{ V}$	1.3 ^a	3.5			
	0.124 at V _{GS} = 2.5 V	1.1	3.5			

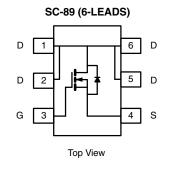
FEATURES

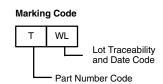
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

· Load Switch for Portable Devices





Ordering Information: Si1058X-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage	V_{DS}	20	V			
Gate-Source Voltage		V_{GS}	± 12	v		
Ocaliana Davis Ocasa (T. 450.00)	T _A = 25 °C	L	1.3 ^{b, c}			
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C	- I _D	1.03 ^{b, c}	Α Α		
Pulsed Drain Current		I _{DM}	6	A		
Avalanche Current	L = 0.1 mH	I _{AS}	7			
Repetitive Avalanche Energy	L = 0.1 min	E _{AS}	2.45	mJ		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	0.2 ^{b, c}	A		
Marian and David Display time?	T _A = 25 °C	P _D	0.236 ^{b, c}	W		
Maximum Power Dissipation ^a	T _A = 70 °C] 'D	0.151 ^{b, c}	VV		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	°C			

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Manifestore Longition to Applicate by	t ≤ 5 s	R _{thJA}	440	530	°C/W	
Maximum Junction-to-Ambient ^{b, d}	Steady State	' ¹thJA	540	650	C/VV	

Notes:

- a. Based on T_C = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 650 °C/W.

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SPECIFICATIONS $(T_J = 25 ^{\circ})$	C, unless othe	erwise noted)					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		18.9		m\//°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	1		- 3.6		mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.7		1.55	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zoro Cata Valtaga Drain Current		V _{DS} = 20 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V, T _J = 85 °C			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	6			Α	
D : 0	D	V _{GS} = 4.5 V, I _D = 1.3 A		0.076	0.091	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 2.5 V, I _D = 1.1 A		0.103	0.124	Ω	
Forward Transconductance	9 _{fs}	V _{DS} = 10 V, I _D = 1.3 A		5.5		S	
Dynamic ^b							
Input Capacitance	C _{iss}			380			
Output Capacitance	C _{oss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		75		pF	
Reverse Transfer Capacitance	C _{rss}			45			
Total Octo Observe	0	$V_{DS} = 10 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 1.3 \text{ A}$		3.9	5.9		
Total Gate Charge	Q _g			3.51	5.3	nC	
Gate-Source Charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 1.3 \text{ A}$		0.82			
Gate-Drain Charge	Q _{gd}			0.61			
Gate Resistance	R_g	f = 1 MHz		4.3	5.6	Ω	
Turn-On Delay Time	t _{d(on)}			8	12		
Rise Time	t _r	V_{DD} = 10 V, R_L = 15 Ω		20	30	ns	
Turn-Off DelayTime	t _{d(off)}	$I_D \cong 1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		13	18		
Fall Time	t _f			6	9		
Drain-Source Body Diode Characteris	tics						
Pulse Diode Forward Current ^a	I _{SM}				6		
Body Diode Voltage	V_{SD}	I _S = 1 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			10.4	16	nC	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 1 A, dl/dt = 100 A/μs		3.7	5.7		
Reverse Recovery Fall Time	t _a	η - 1 A, αι/αι = 100 A/μδ		6.5		ns	
Reverse Recovery Rise Time	t _b	3.9					

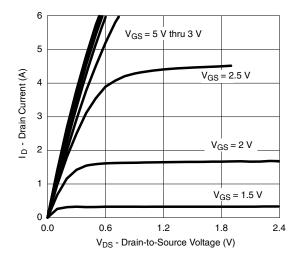
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

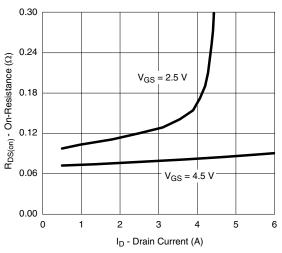
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



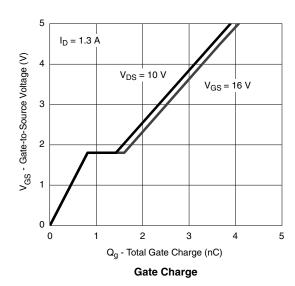
TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

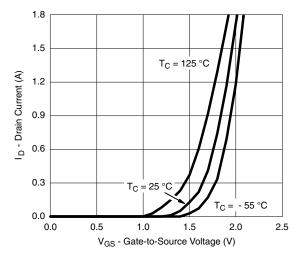


Output Characteristics

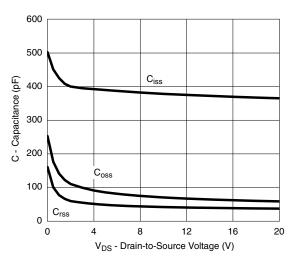


On-Resistance vs. Drain Current

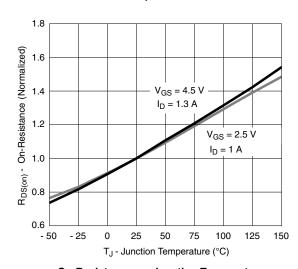




Transfer Characteristics Curves vs. Temp.



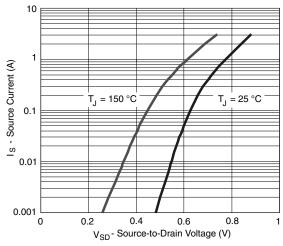
Capacitance



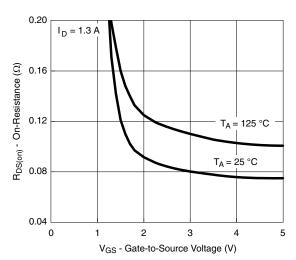
On-Resistance vs. Junction Temperature

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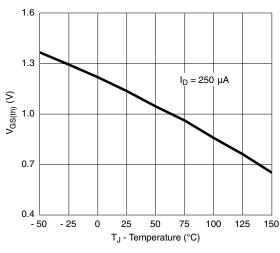
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



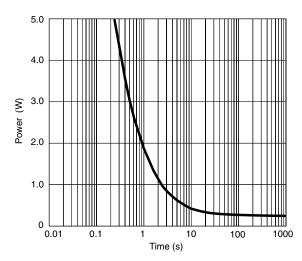
Source-Drain Diode Forward Voltage



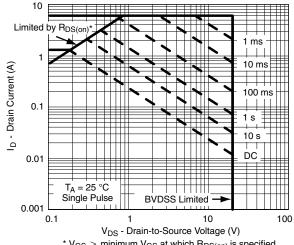
R_{DS(on)} vs. V_{GS} vs. Temperature



Threshold Voltage



Single Pulse Power

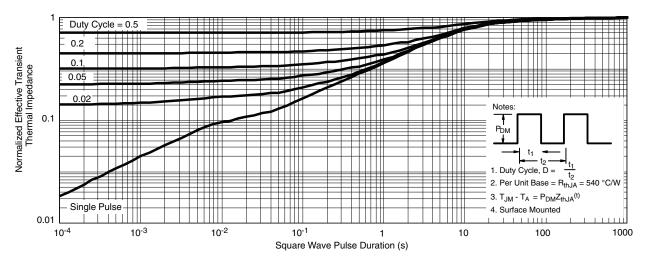


* $V_{GS} > \mbox{minimum } V_{GS}$ at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

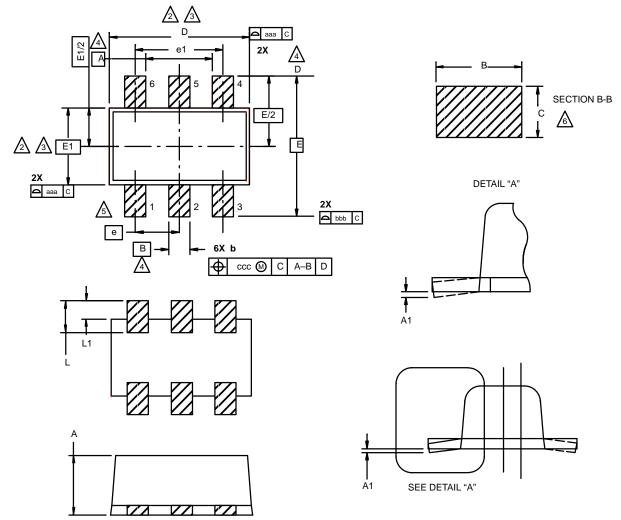


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppq?73894.



SC89: 6- LEADS (SOT-563F)



NOTES:

1. Dimensions in millimeters.



Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.



Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.



Datums A, B and D to be determined 0.10 mm from the lead tip.



Terminal numbers are shown for reference only.



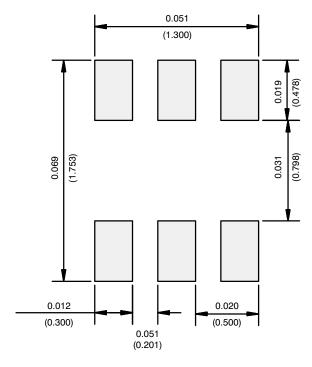
These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

Dim A	Min	Max			Tolerances Of Form And Position		
Α		IVIAX	Note	Symbol			
	0.56	0.60		aaa	0.10		
A1	0.00	0.10		bbb	0.10		
b	0.15	0.30		ccc	0.10		
С	0.10	0.18					
D	1.50	1.70	2, 3				
E	1.55	1.70					
E1	1.20 BSC		2, 3				
е	0.50 BSC						
e1	1.00 BSC						
L	0.35 BSC						
L1	0.20 BSC						

DWG: 5880



RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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