Complementary N- and P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
N-Channel	20	0.396 at V_{GS} = 4.5 V	0.5	0.75 nC
		0.456 at V_{GS} = 2.5 V	0.2	
		0.546 at V_{GS} = 1.8 V	0.2	
		0.760 at V_{GS} = 1.5 V	0.05	
P-Channel	- 20	0.756 at V_{GS} = - 4.5 V	- 0.35	1 nC
		1.038 at V_{GS} = - 2.5 V	- 0.35	
		1.440 at V_{GS} = - 1.8 V	- 0.1	
		2.4 at V_{GS} = - 1.5 V	- 0.05	

FEATURES

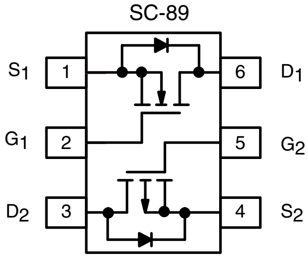
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- High-Side Switching
- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Typical ESD Protection: N-Channel 1500 V P-Channel 1000 V (HBM)
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

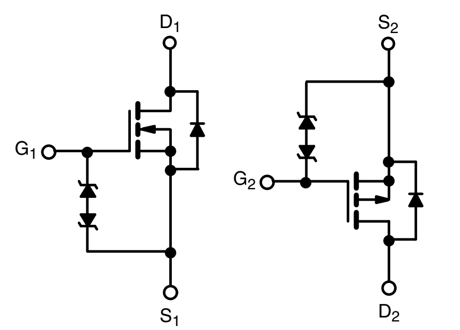
- Load Switch, Small Signal Switches and Level-Shift Switches
  - Battery Operated Systems
  - Portable

SOT-563
SC-89



Marking Code: 5

Top View



N-Channel MOSFET P-Channel MOSFET

Ordering Information: Si1016CX-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
Parameter		**Symbol**	**N-Channel**	**P-Channel**	**Unit**
Drain-Source Voltage		V_{DS}	20	- 20	V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current (T_J = 150 °C)	T_A = 25 °C	I_D	0.6[a, b]	- 0.6[a, b]	A
	T_A = 70 °C		0.49[a, b]	- 0.49[a, b]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	2	- 1.5	
Source Drain Current Diode Current	T_A = 25 °C	I_S	0.18[a, b]	- 0.18[a, b]	
Maximum Power Dissipation	T_A = 25 °C	P_D	0.22[a, b]	0.22[a, b]	W
	T_A = 70 °C		0.14[a, b]	0.14[a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[d, e]			260		

THERMAL RESISTANCE RATINGS							
			N-Channel		**P-Channel**		
Parameter		**Symbol**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Unit**
Maximum Junction-to-Ambient[a, c]	t ≤ 5 s	R_{thJA}	470	565	470	565	°C/W
	Steady State		560	675	560	675	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. t = 5 s.
c. Maximum under steady state conditions is 675 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = - 250 µA	P-Ch	- 20			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	N-Ch		17		mV/°C
		I_D = - 250 µA	P-Ch		- 12		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	N-Ch		- 1.8		
		I_D = - 250 µA	P-Ch		1.8		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	0.4		1	V
		$V_{DS} = V_{GS}$, I_D = - 250 µA	P-Ch	- 0.4		- 1	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V	N-Ch			± 1	µA
			P-Ch			± 1	
		V_{DS} = 0 V, V_{GS} = ± 8 V	N-Ch			± 30	
			P-Ch			± 30	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			1	
		V_{DS} = - 20 V, V_{GS} = 0 V	P-Ch			- 1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C	N-Ch			10	
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 55 °C	P-Ch			- 10	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 4.5 V	N-Ch	2			A
		$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	P-Ch	- 1.5			
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.5 A	N-Ch		0.330	0.396	Ω
		V_{GS} = - 4.5 V, I_D = - 0.35 A	P-Ch		0.630	0.756	
		V_{GS} = 2.5 V, I_D = 0.2 A	N-Ch		0.380	0.456	
		V_{GS} = - 2.5 V, I_D = - 0.35 A	P-Ch		0.865	1.038	
		V_{GS} = 1.8 V, I_D = 0.2 A	N-Ch		0.420	0.546	
		V_{GS} = - 1.8 V, I_D = - 0.1 A	P-Ch		1.2	1.44	
		V_{GS} = 1.5 V, I_D = 0.05 A	N-Ch		0.505	0.760	
		V_{GS} = - 1.5 V, I_D = - 0.05 A	P-Ch		1.6	2.4	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 0.5 A	N-Ch		2		S
		V_{DS} = - 10 V, I_D = - 3.6 A	P-Ch		1		
Input Capacitance	C_{iss}	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch		43		pF
			P-Ch		45		
Output Capacitance	C_{oss}		N-Ch		14		
			P-Ch		15		
Reverse Transfer Capacitance	C_{rss}		N-Ch		8		
			P-Ch		10		
Dynamic[a]							
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 0.6 A	N-Ch		1.3	2	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 0.4 A	P-Ch		1.65	2.50	
		N-Channel V_{DS} = 10 V, V_{GS} = 2.5 V, I_D = 0.6 A P-Channel V_{DS} = - 10 V, V_{GS} = - 2.5 V, I_D = - 0.4 A	N-Ch		0.75	1.2	
			P-Ch		1	2	
Gate-Source Charge	Q_{gs}		N-Ch		0.15		
			P-Ch		0.2		
Gate-Drain Charge	Q_{gd}		N-Ch		0.13		
			P-Ch		0.26		
Gate Resistance	R_g	f = 1 MHz	N-Ch	2.4	12.2	24.4	Ω
			P-Ch	2.4	12	24	

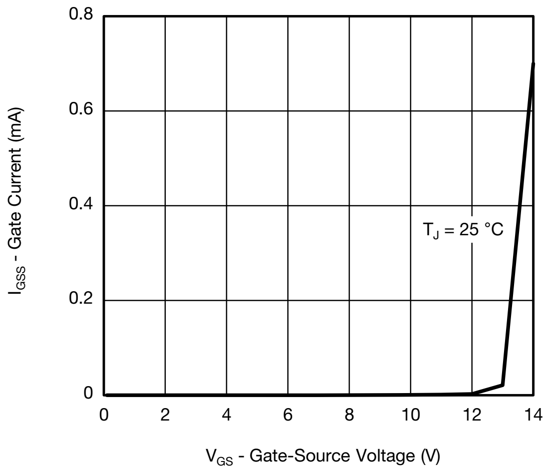
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Dynamic[a]							
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 20 Ω $I_D \cong$ 0.5 A, V_{GEN} = 4.5 V, R_g = 1 Ω P-Channel V_{DD} = - 10 V, R_L = 33.3 Ω $I_D \cong$ - 0.3 A, V_{GEN} = - 4.5 V, R_g = 1 Ω	N-Ch		11	20	ns
			P-Ch		9	18	
Rise Time	t_r		N-Ch		16	24	
			P-Ch		10	20	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		26	39	
			P-Ch		10	20	
Fall Time	t_f		N-Ch		11	20	
			P-Ch		8	16	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 20 Ω $I_D \cong$ 0.5 A, V_{GEN} = 8 V, R_g = 1 Ω P-Channel V_{DD} = - 10 V, R_L = 33.3 Ω $I_D \cong$ - 0.3 A, V_{GEN} = - 8 V, R_g = 1 Ω	N-Ch		2	4	
			P-Ch		1	2	
Rise Time	t_r		N-Ch		13	20	
			P-Ch		8	16	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		7	14	
			P-Ch		9	18	
Fall Time	t_f		N-Ch		5	10	
			P-Ch		5	10	
Drain-Source Body Diode Characteristics							
Pulse Diode Forward Current[a]	I_{SM}		N-Ch			2	A
			P-Ch			- 1.5	
Body Diode Voltage	V_{SD}	I_S = 0.5 A, V_{GS} = 0 V	N-Ch		0.85	1.2	V
		I_S = - 0.3 A, V_{GS} = 0 V	P-Ch		- 0.87	- 1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel I_F = 0.5 A, dI/dt = 100 A/µs, T_J = 25 °C P-Channel I_F = - 0.3 A, dI/dt = - 100 A/µs, T_J = 25 °C	N-Ch		10	20	ns
			P-Ch		16	24	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		2	4	nC
			P-Ch		8	20	
Reverse Recovery Fall Time	t_a		N-Ch		5		ns
			P-Ch		11		
Reverse Recovery Rise Time	t_b		N-Ch		5		
			P-Ch		5		

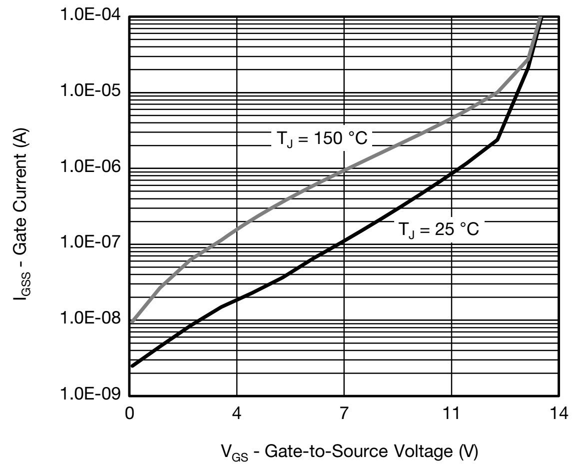
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

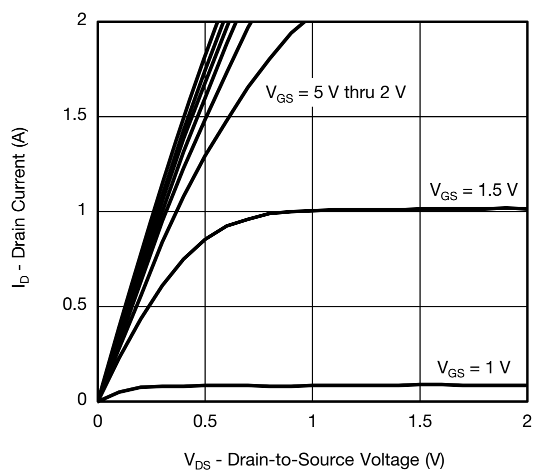
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



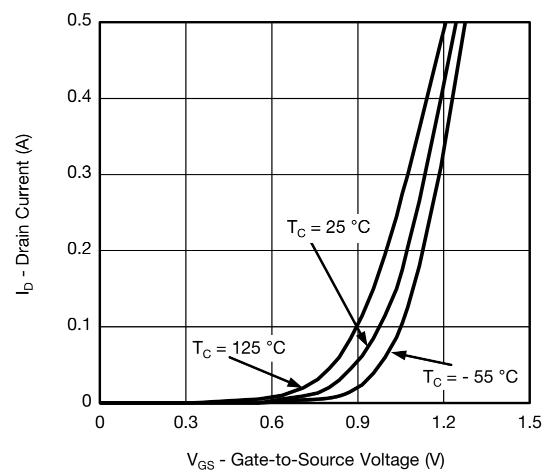
Gate Current vs. Gate-Source Voltage



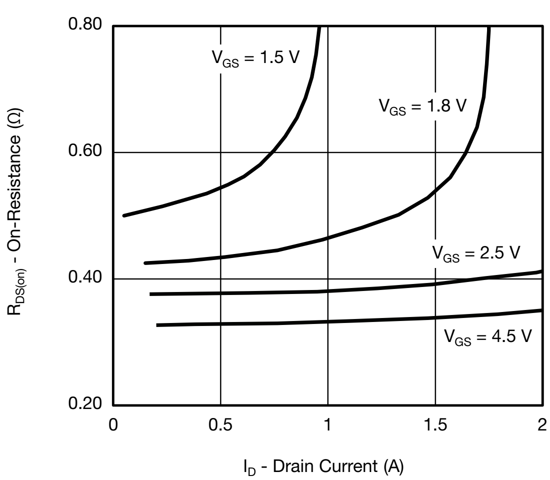
Gate Current vs. Gate-Source Voltage



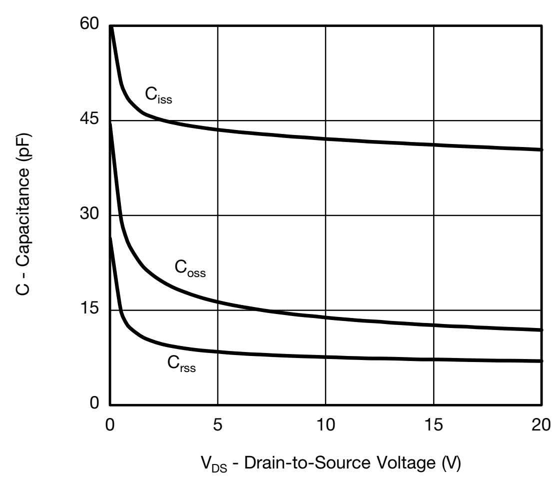
Output Characteristics



Transfer Characteristics

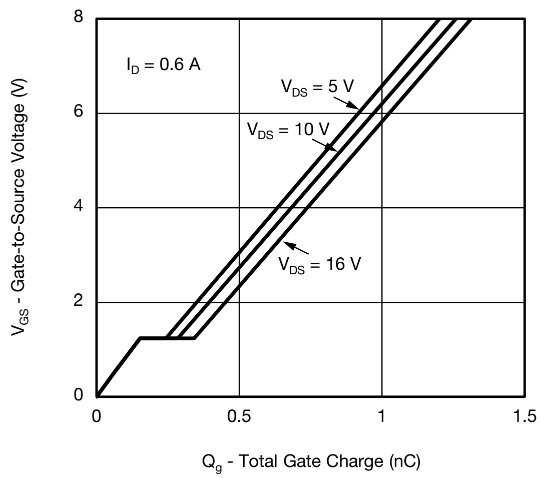


On-Resistance vs. Drain Current

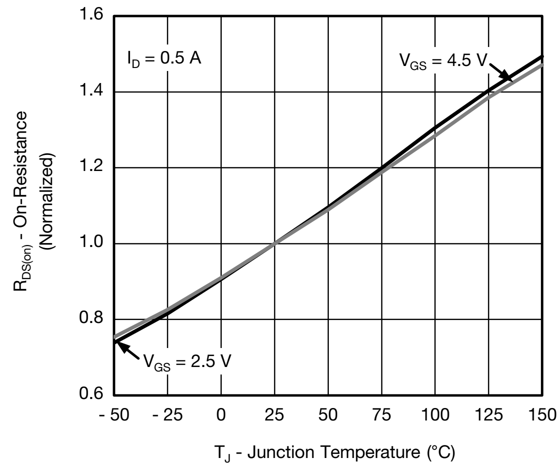


Capacitance

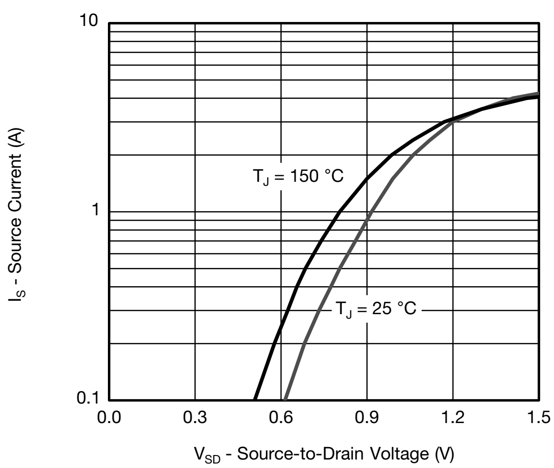
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



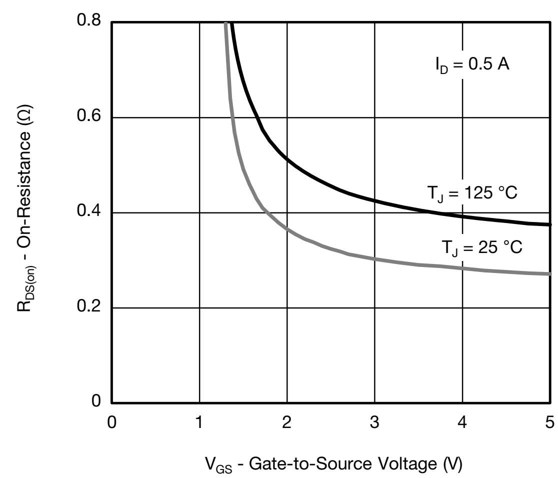
Gate Charge



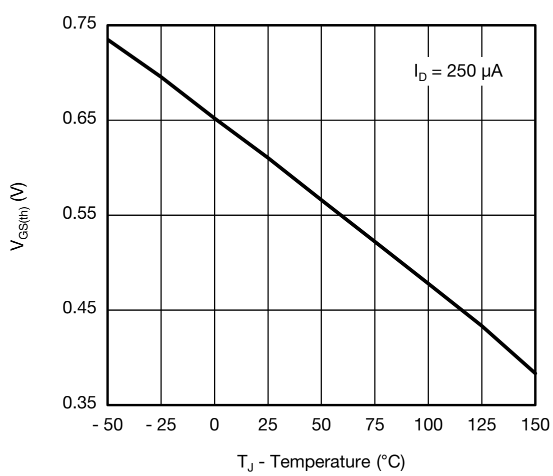
On-Resistance vs. Junction Temperature



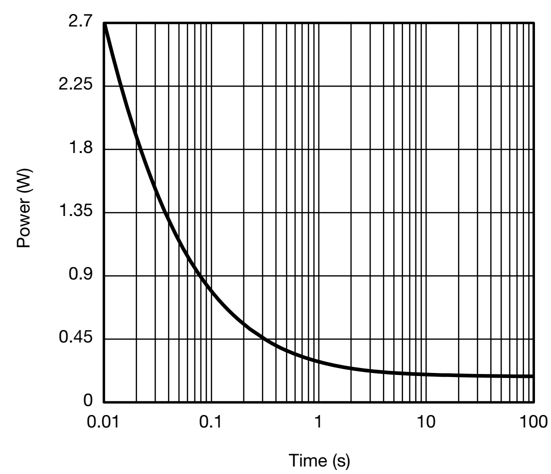
Soure-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

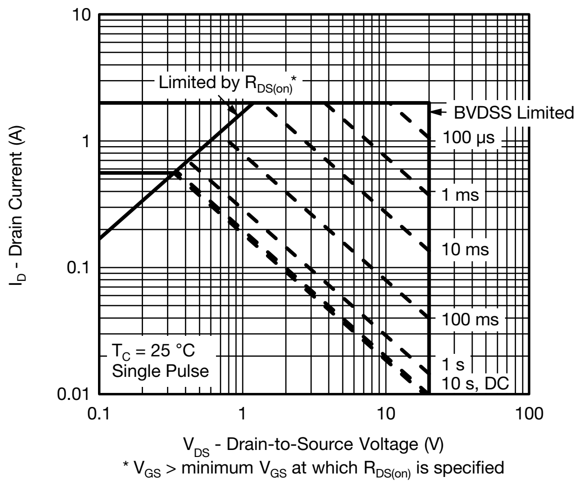


Threshold Voltage

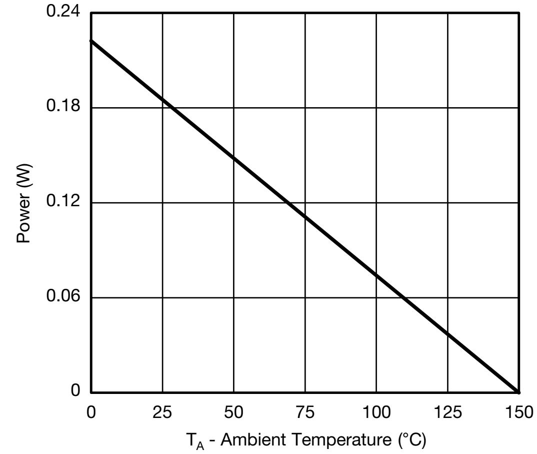


Single Pulse Power, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

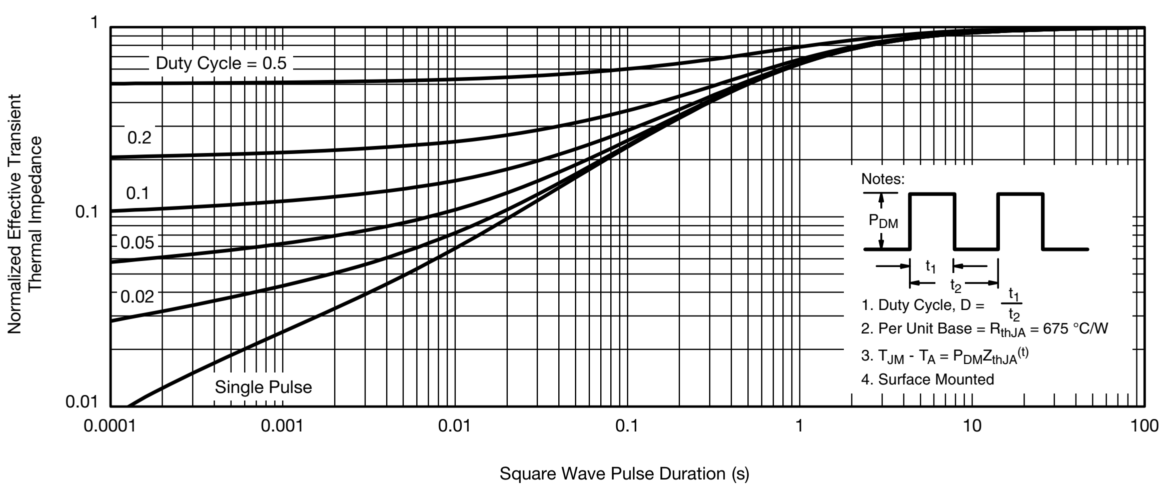


Safe Operating Area, Junction-to-Ambient



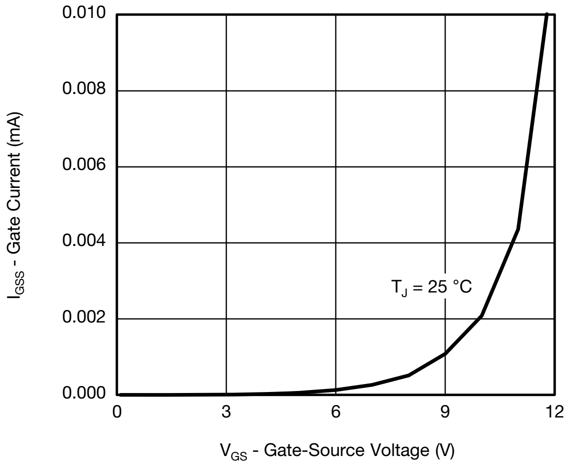
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

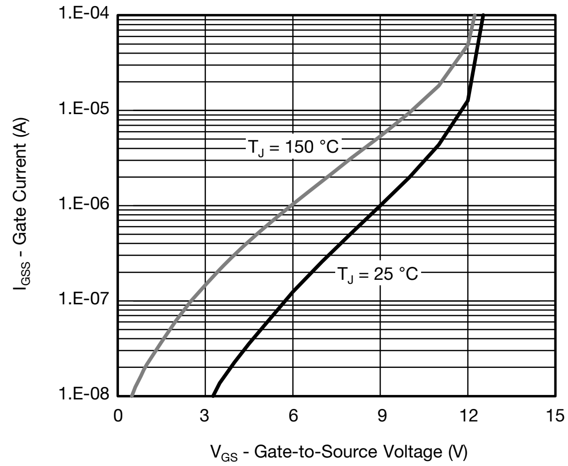


Normalized Thermal Transient Impedance, Junction-to-Ambient

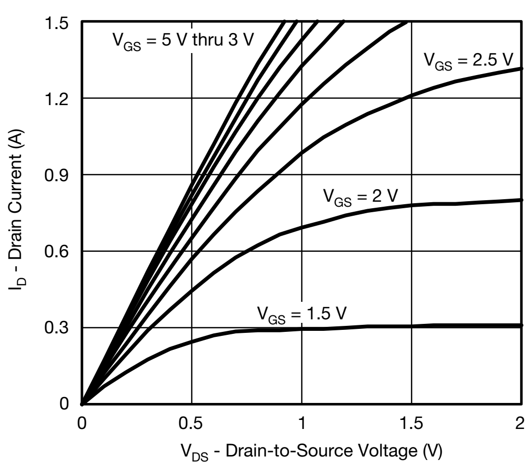
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



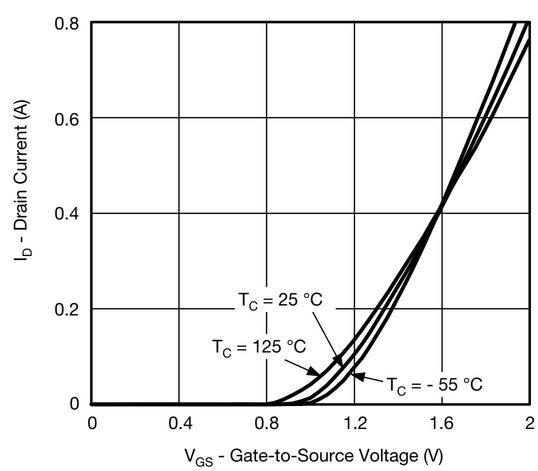
Gate Current vs. Gate-Source Voltage



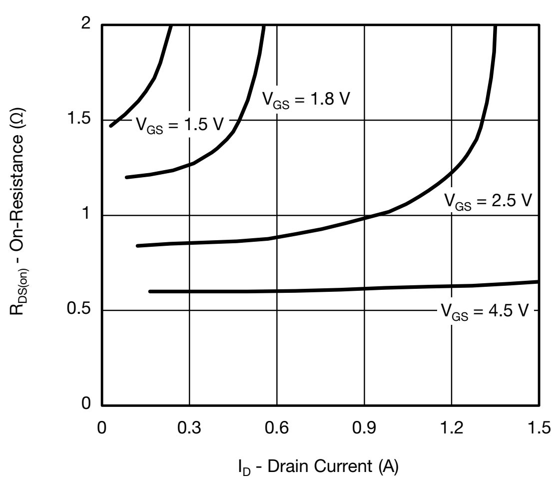
Gate Current vs. Gate-Source Voltage



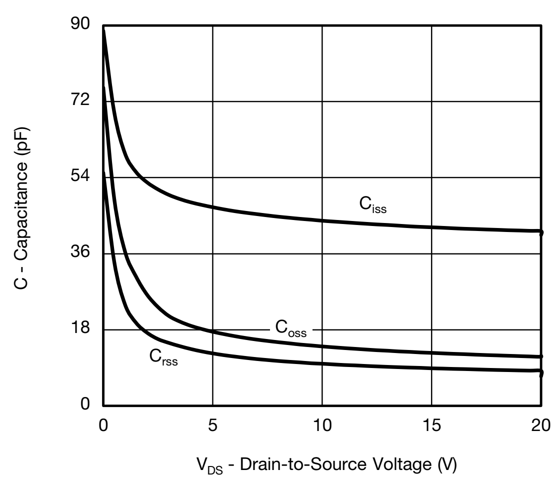
Output Characteristics



Transfer Characteristics

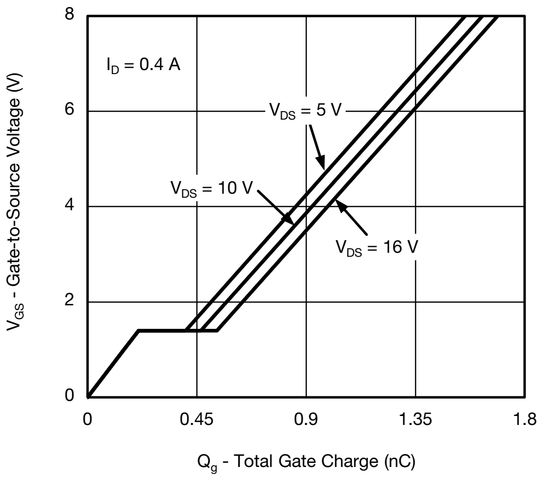


On-Resistance vs. Drain Current

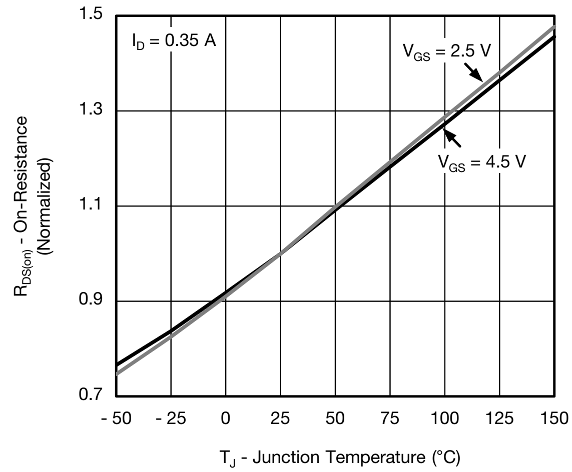


Capacitance

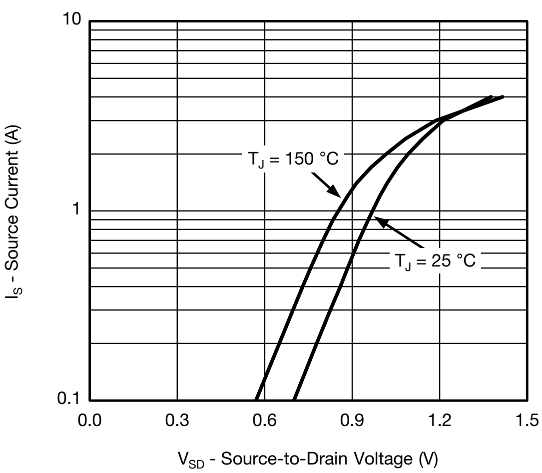
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



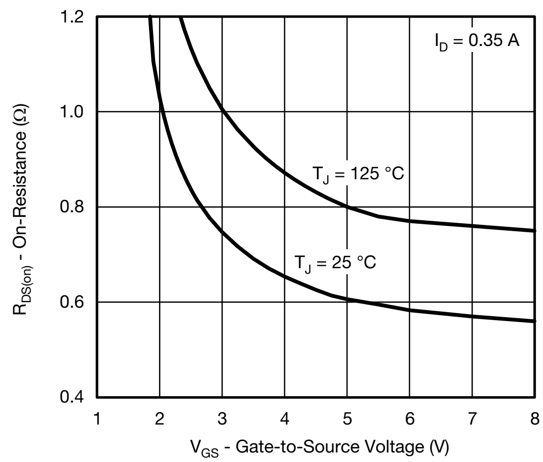
Gate Charge



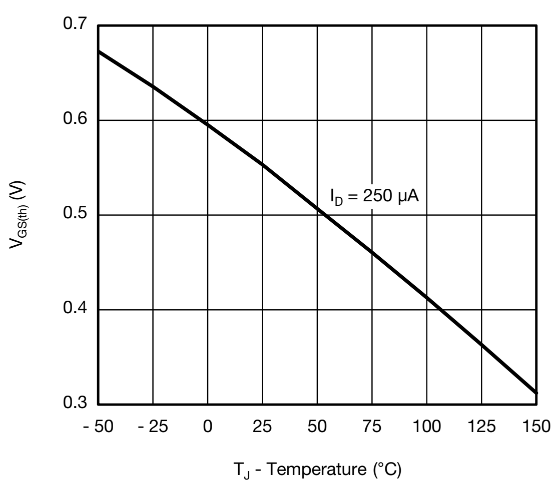
On-Resistance vs. Junction Temperature



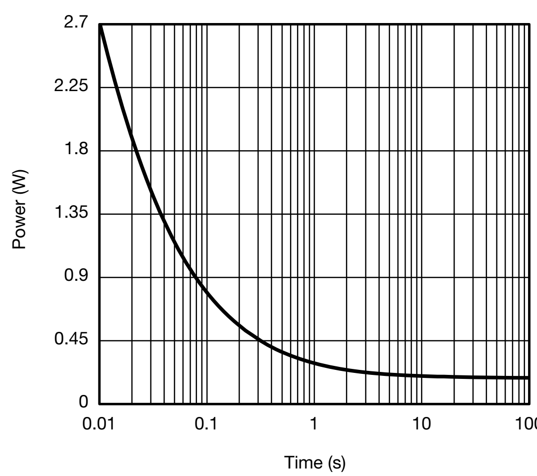
Soure-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

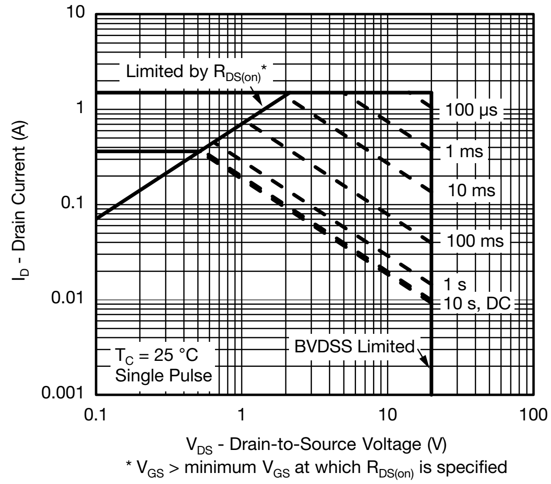


Threshold Voltage

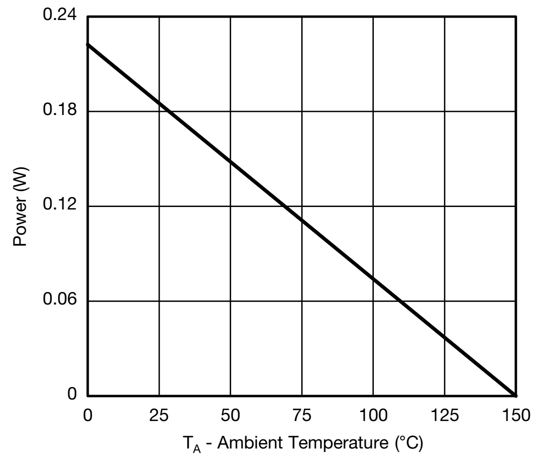


Single Pulse Power, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

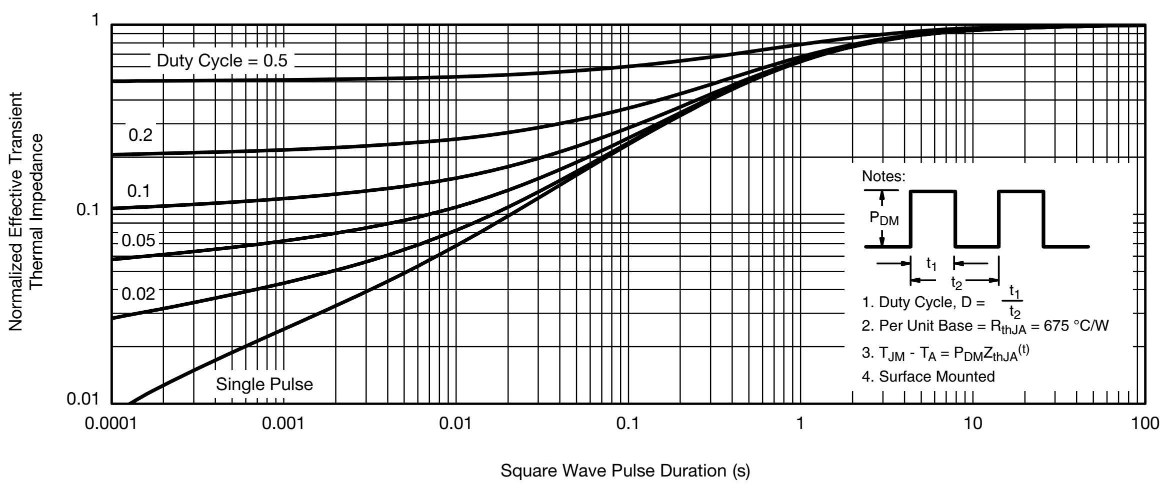


Safe Operating Area, Junction-to-Ambient



Power Derating, Junction-to-Ambient

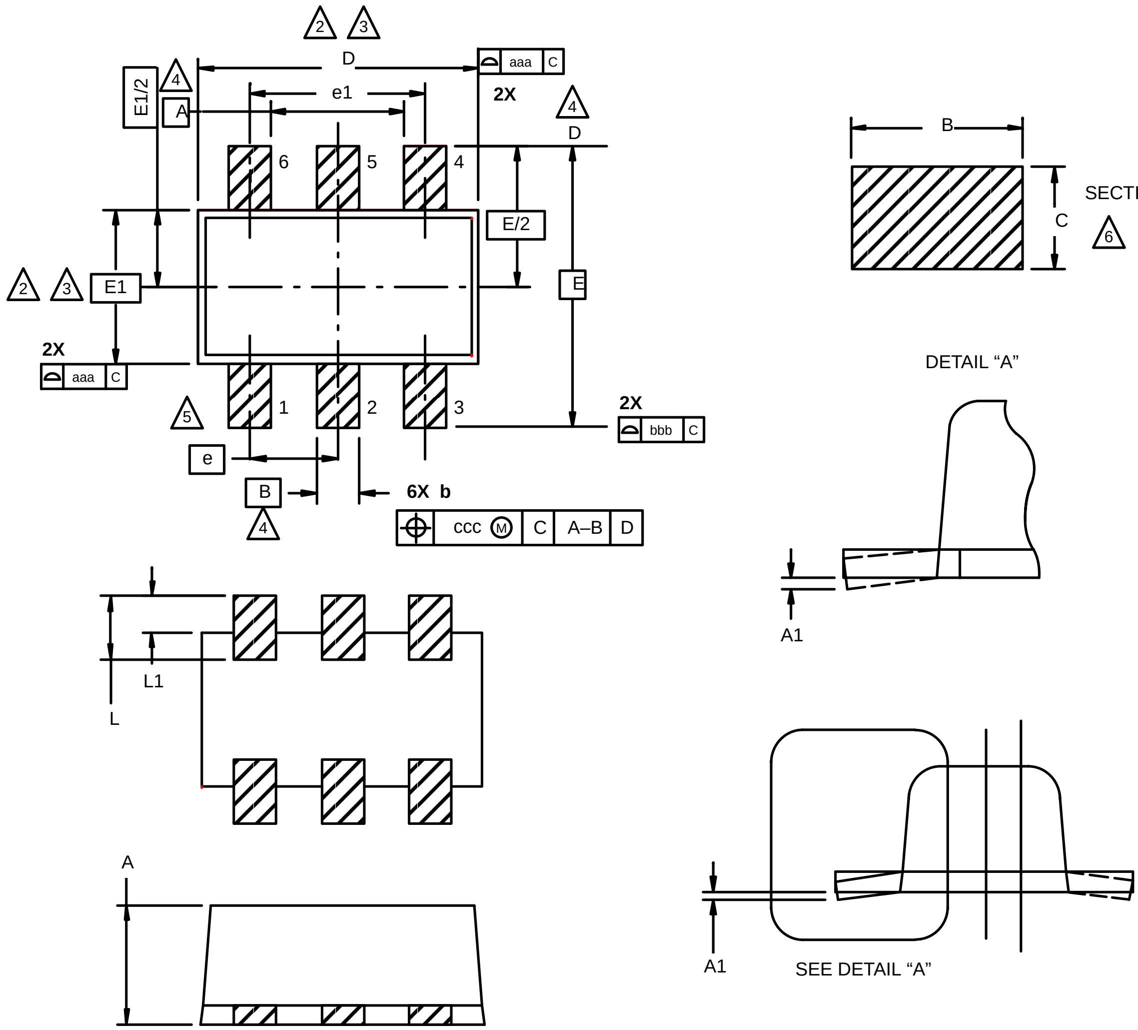
* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67535.

SC89: 6- LEADS (SOT-563F)



NOTES:

1. Dimensions in millimeters.

2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

3. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

4. Datums A, B and D to be determined 0.10 mm from the lead tip.

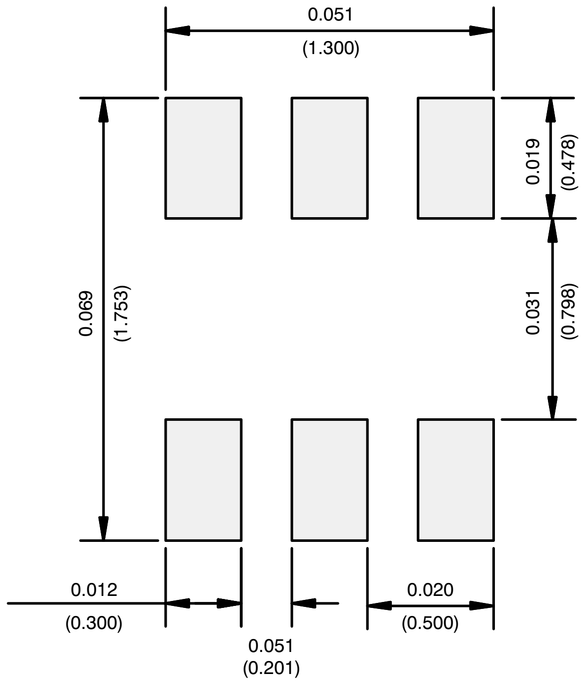
5. Terminal numbers are shown for reference only.

6. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

	MILLIMETERS				Tolerances Of Form And Position
Dim	Min	Max	Note	Symbol	
A	0.56	0.60		aaa	0.10
A1	0.00	0.10		bbb	0.10
b	0.15	0.30		ccc	0.10
c	0.10	0.18			
D	1.50	1.70	2, 3		
E	1.55	1.70			
E1	1.20 BSC		2, 3		
e	0.50 BSC				
e1	1.00 BSC				
L	0.35 BSC				
L1	0.20 BSC				

ECN: E-00499—Rev. B, 02-Jul-01
DWG: 5880

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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