Universal Input Switchmode Controller

FEATURES

- 10- to 450-V Input Range
- Current-Mode Control
- 125-mA Output Drive
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET

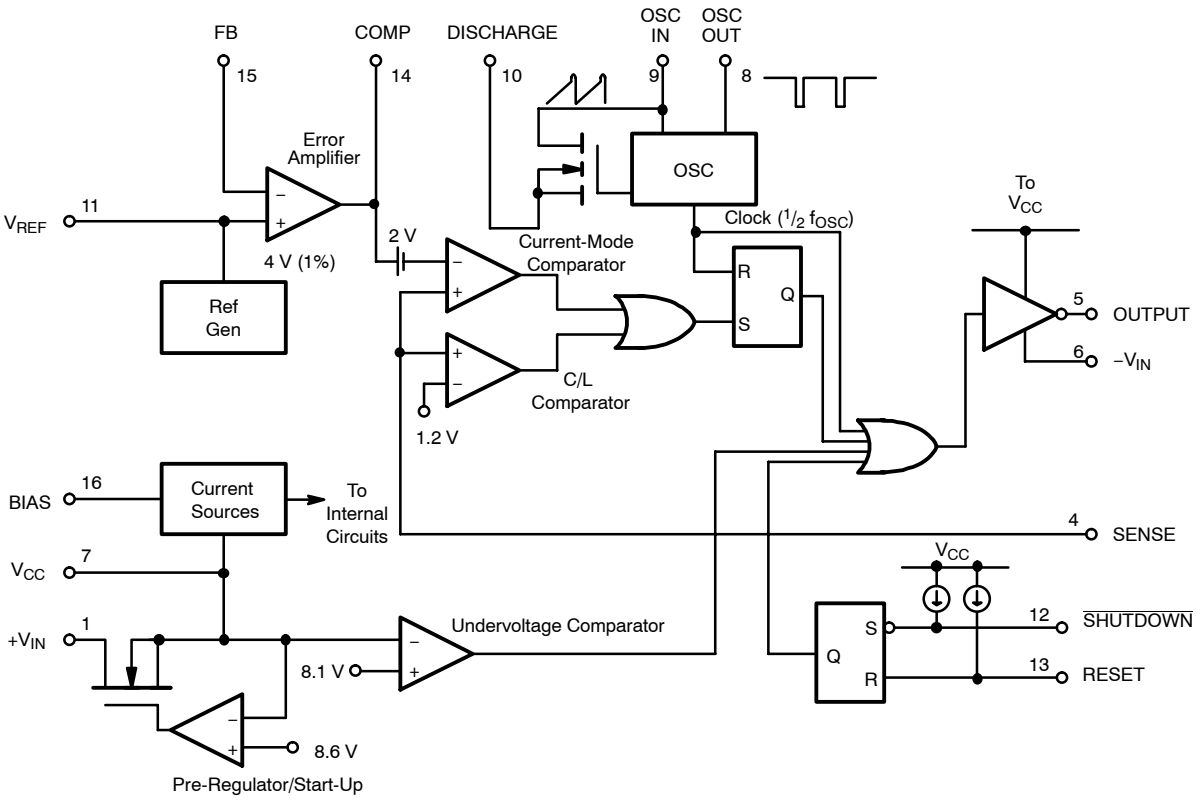
DESCRIPTION

The Si9120 is a BiC/DMOS integrated circuit designed for use in low-power, high-efficiency off-line power supplies. High-voltage DMOS inputs allow the controller to work over a wide range of input voltages (10- to 450-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce quiescent current to less than 1.5 mA.

A CMOS output driver provides high-speed switching for MOSFET devices with gate charge, Q_g, up to 25 nC, enough to supply 30 W of output power at 100 kHz. These devices, when combined with an output MOSFET and transformer, can be used to implement single-ended power converter topologies (i.e., flyback and forward).

The Si9120 is available in both standard and lead (Pb)-free 16-pin plastic DIP and SOIC packages which are specified to operate over the industrial temperature range of −40°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM



Applications information, see AN707 and AN708.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} . . . . . 15 V
$+V_{IN}$ . . . . . 450 V
Logic Inputs (RESET
$\overline{\text{SHUTDOWN}}$, OSC IN, OSC OUT) . . . . . −0.3 V to V_{CC} + 0.3 V
Linear Input
(FEEDBACK, SENSE, BIAS, V_{REF}) . . . . . −0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) . . . . . 5 mA[a]
Continuous Output Current (Source or Sink) . . . . . 125 mA
Storage Temperature . . . . . −65 to 150°C
Operating Temperature . . . . . −40 to 85°C
Junction Temperature (T_J) . . . . . 150°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP (J Suffix)[c] . . . . . 750 mW
16-Pin SOIC (Y Suffix)[d] . . . . . 900 mW
Thermal Impedance (Θ_{JA})
16-Pin Plastic DIP . . . . . 167°C/W
16-Pin SOIC . . . . . 140°C/W

Notes
a. Continuous current may be limited by the applications maximum input voltage and the package power dissipation.
b. Device mounted with all leads soldered or welded to PC board.
c. Derate 6 mW/°C above 25°C.
d. Derate 7.2 mW/°C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$
V_{CC} . . . . . 9.5 V to 13.5 V
$+V_{IN}$ . . . . . 10 V to 450 V
f_{OSC} . . . . . 40 kHz to 1 MHz

R_{OSC} . . . . . 25 kΩ to 1 MΩ
Linear Inputs . . . . . 0 to V_{CC} − 3 V
Digital Inputs . . . . . 0 to V_{CC}

SPECIFICATIONS[a]

Parameter	Symbol	Specific Test Conditions DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 300 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	TEMP[B]	LIMITS D Suffix −40 to 85°C MIN[C]	TYP[D]	MAX[C]	Unit
Reference							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	Room Full	3.88 3.82	4.0	4.12 4.14	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	μA
Temperature Stability[e]	T_{REF}		Full		0.5	1.0	mV/°C
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	C_{STRAY} Pin 9 ≤ 5 pF R_{OSC} = 330 kΩ	Room	80	100	120	kHz
		C_{STRAY} Pin 9 ≤ 5 pF R_{OSC} = 150 kΩ	Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = f(13.5 V) − f(9.5 V) / f(9.5 V)	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.92		4.08	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V	Room		25	500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$	Room		±15	±40	mV
Open Loop Voltage Gain[e]	A_{VOL}	OSC IN = $-V_{IN}$	Room	60	80		dB
Unity Gain Bandwidth[e]	BW	OSC IN = $-V_{IN}$	Room	1.0	1.5		MHz

SPECIFICATIONS[a]

Parameter	Symbol	Specific Test Conditions DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V + V_{IN} = 300 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	TEMP[b]	LIMITS D Suffix –40 to 85°C MIN[c]	TYP[d]	MAX[c]	Unit
Error Amplifier (Cont'd)							
Dynamic Output Impedance[e]	Z_{OUT}	Error Amp configured for 60 dB gain	Room		1000	2000	Ω
Output Current	I_{OUT}	Source V_{FB} = 3.4 V	Room		–2.0	–1.4	mA
		Sink V_{FB} = 4.5 V	Room	0.12	0.15		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	V_{SENSE} = 1.5 V, See Figure 1	Room		100	150	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 10 μA	Room	450			V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	Room			10	μA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 μA	Room	7.8	8.6	9.4	V
Undervoltage Lockout	V_{UVLO}		Room	7.0	8.1	8.9	
$V_{REG} - V_{UVLO}$	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}	C_L = 500 pF at Pin 5	Room		0.85	1.5	mA
Bias Current	I_{BIAS}		Room	10	15	20	μA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	C_L = 500 pF, $V_{SENSE} = -V_{IN}$ See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low[e]	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	μA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	–35	–25		
Output							
Output High Voltage	V_{OH}	I_{OUT} = –10 mA	Room Full	9.7 9.5			V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA	Room Full			0.3 0.5	
Output Resistance	R_{OUT}	I_{OUT} = 10 mA, Source or Sink	Room Full		20 25	30 50	Ω
Rise Time[e]	t_r	C_L = 500 pF	Room		40	75	ns
Fall Time[e]	t_f		Room	40	75		

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
a. 250 V ≤ $+V_{IN}$ 380 V place a 10-kΩ, $^1/_4$-W resistor in series with a $+V_{IN}$ (Pin1).
380 V ≤ $+V_{IN}$ 450 V place a 15-kΩ, $^1/_4$-W resistor in series with a $+V_{IN}$ (Pin1).
Connect a 0.01-μ*fd* capacitor between $+V_{IN}$ (Pin 1) and $-V_{IN}$ (Pin 6).

TIMING WAVEFORMS

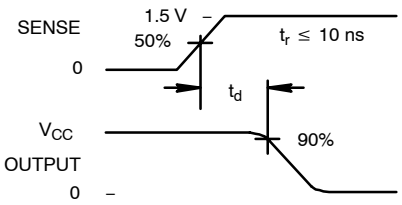


FIGURE 1.

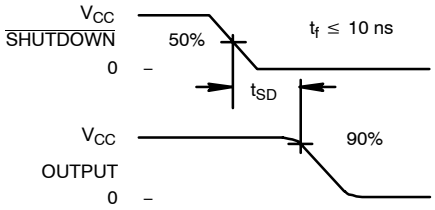


FIGURE 2.

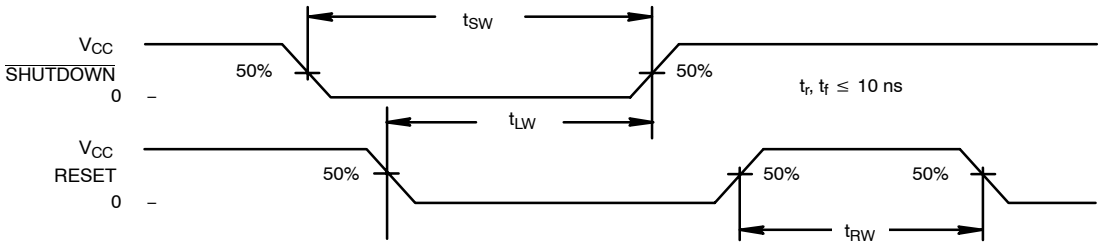
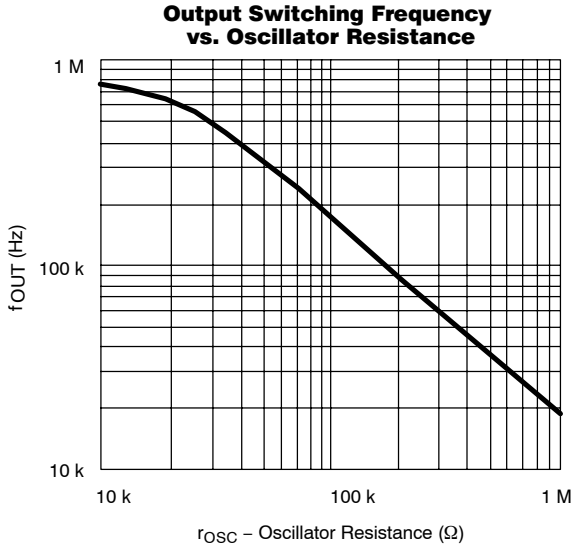


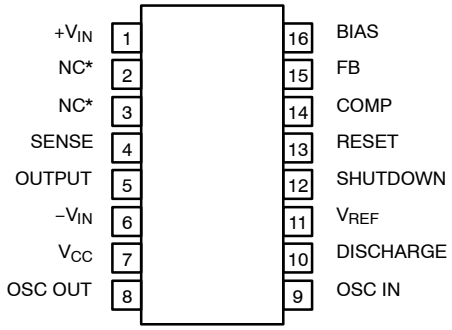
FIGURE 3.

TYPICAL CHARACTERISTICS



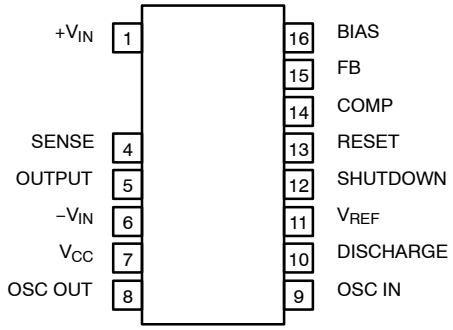
PIN CONFIGURATIONS AND ORDERING INFORMATION

Dual-In-Line



Top View

SOIC



Top View
Note: Pins 2 and 3 are removed

ORDERING INFORMATION

Part Number	Temperature Range	Package
Si9120DY	−40 to 85°C	SOIC-16
Si9120DY-T1		
Si9120DY-T1—E3		
Si9120DJ		PDIP-16
Si9120DJ—E3		

DETAILED DESCRIPTION

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9120 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary “bootstrap” winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ (pin 1) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET which is connected between $+V_{IN}$ and V_{CC} (pin 7). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6-V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: When driving large MOSFETs at high frequency without a bootstrap V_{CC} supply, power dissipation in the pre-regulator may exceed the power rating of the IC package. For operation of $+V_{IN}$ > 250 V, a 10-kΩ, $^1/_4$-W resistor should be placed in series with $+V_{IN}$ (Pin 1). For $+V_{IN}$ > 380 V, a 15-kΩ, $^1/_4$-W resistor is recommended.

BIAS

To properly set the bias for the Si9120, a 390-kΩ resistor should be tied from BIAS (pin 16) to $-V_{IN}$ (pin 6). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

DETAILED DESCRIPTION (CONT'D)

Reference Section

The reference section of the Si9120 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9120 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ± 2% of 4 V. This compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for high input impedance. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Typical Characteristics for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 12) and RESET (pin 13) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET. $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. See Table TABLE 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

TABLE 1.
TRUTH TABLE FOR $\overline{\text{SHUTDOWN}}$ AND RESET PINS

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
↑	L	Off (Latched—No Change)

Output Driver

The push-pull driver output has a typical on-resistance of 20-Ω maximum switching times are specified at 75 ns for a 500-pF load. This is sufficient to directly drive MOSFETs such as the IRF820, BUZ78 or BUZ80. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses.

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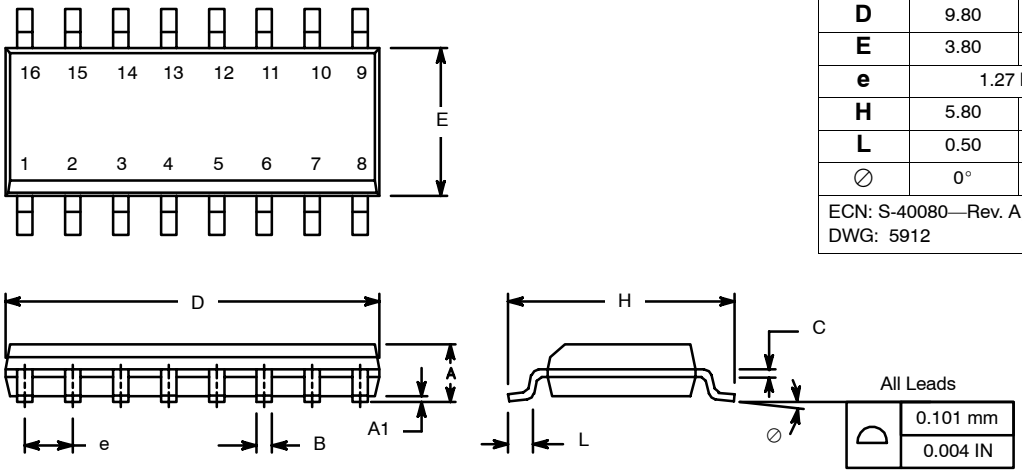
SOIC (NARROW): 16-LEAD (POWER IC ONLY)

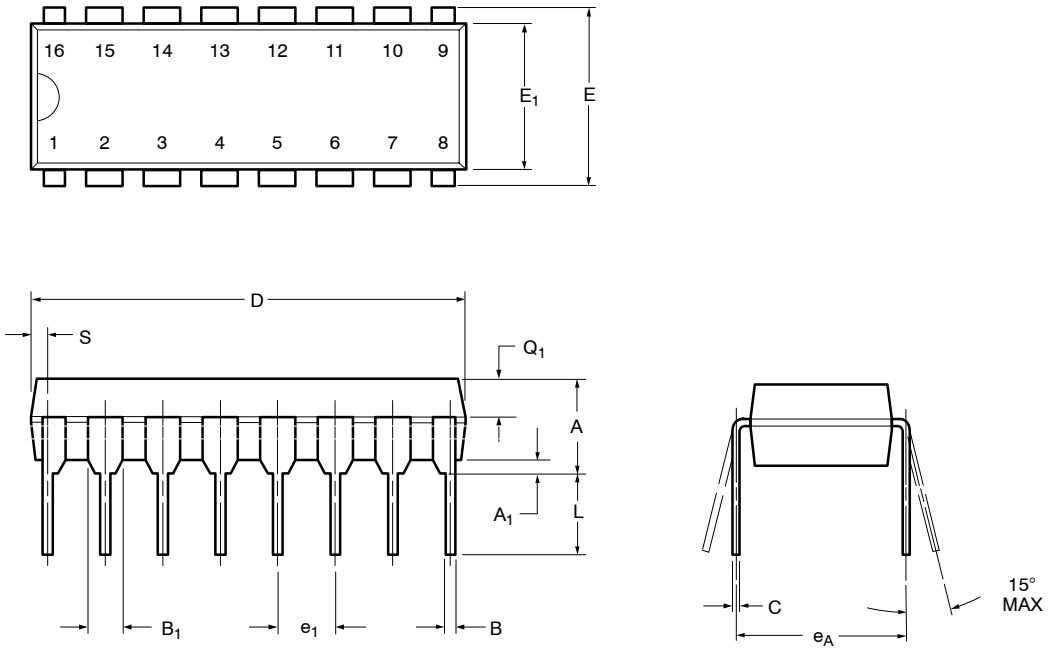
JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-40080—Rev. A, 02-Feb-04
DWG: 5912



PDIP: 16-LEAD (POWER IC ONLY)



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-40081—Rev. A, 02-Feb-04 DWG: 5920				

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