

Precision 8-Ch/Dual 4-Ch Low Voltage Analog Multiplexers

DESCRIPTION

The DG3408, DG3409 uses BiCMOS wafer fabrication technology that allows the DG3408/3409 to operate on single and dual supplies. Single supply voltage ranges from 3 to 12 V while dual supply operation is recommended with ± 3 to ± 6 V.

The DG3408 is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0 , A_1 , A_2). The DG3409 is a dual 4-channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A_0 , A_1). Break-before-make switching action to protect against momentary crosstalk between adjacent channels.

FEATURES

- 2.7 V to 12 V single supply or ± 3 to ± 6 V dual supply operation
- Low on-resistance - R_{ON} : 3.9 Ω typ.
- Fast switching: t_{ON} - 42 ns, t_{OFF} - 24 ns
- Break-before-make guaranteed
- Low leakage
- TTL, CMOS, LV logic (3 V) compatible
- 2000 V ESD protection (HBM)
- MICRO FOOT® package
- Lead (Pb)-free solder bumps


RoHS
COMPLIANT

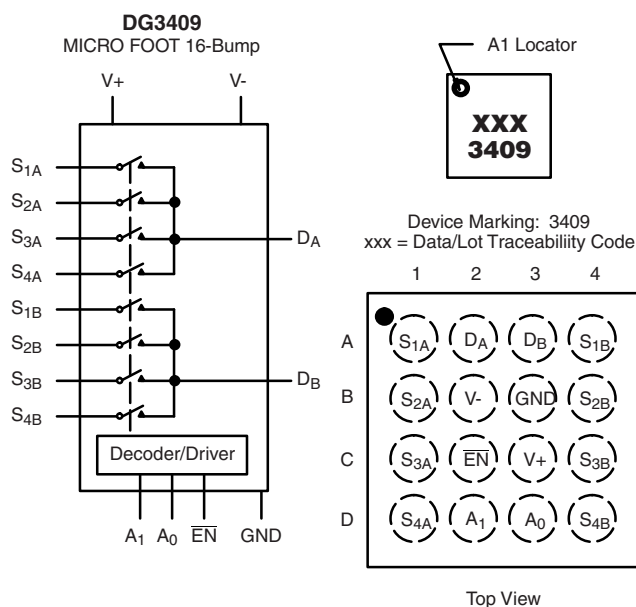
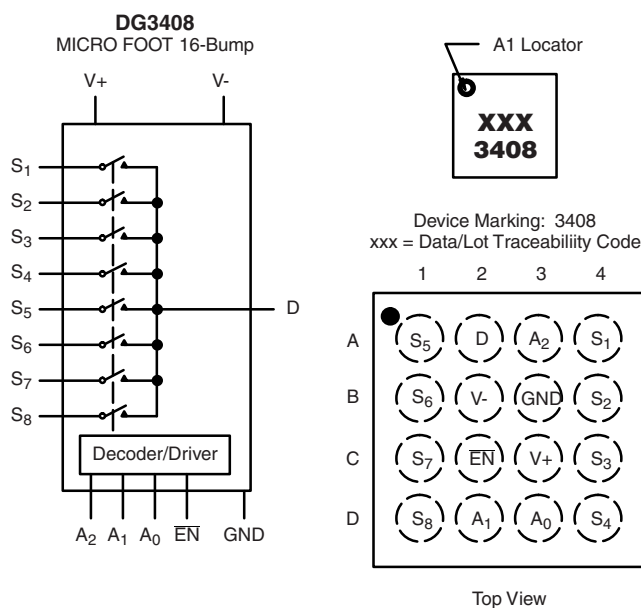
BENEFITS

- High accuracy
- Single and dual power rail capacity
- Wide operating voltage range
- Simple logic interface

APPLICATIONS

- Data acquisition systems
- Battery operated equipment
- Portable test equipment
- Sample and hold circuits
- Communication systems
- SDSL, DSLAM
- Audio and video signal routing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE (DG3408)				
A ₂	A ₁	A ₀	EN	On Switch
X	X	X	1	None
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8

TRUTH TABLE (DG3409)			
A ₁	A ₀	EN	On Switch
X	X	1	None
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

X = Do not care

For low and high voltage levels for V_{AX} and V_{EN} consult "Digital Control" Parameters for Specific V+ operation. See Specifications Tables for:

Single Supply 12 V

Dual Supply V+ = 5 V, V- = - 5 V

Single Supply 5 V

Single Supply 3 V

ORDERING INFORMATION (DG3408)		
Temperature Range	Package	Part Number
- 40 °C to 85 °C	MICRO FOOT: 16-Bump (4 x 4, 0.5 mm Pitch, 238 µm Bump Height)	DG3408DB-T2-E1 (Lead (Pb)-free)

ORDERING INFORMATION (DG3409)		
Temperature Range	Package	Part Number
- 40 °C to 85 °C	MICRO FOOT: 16-Bump (4 x 4, 0.5 mm Pitch, 238 µm Bump Height)	DG3409DB-T2-E1 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)		
Parameter	Limit	Unit
Voltage Referenced V+ to V-	14	V
GND	7	
Digital Inputs ^a , V _S , V _D	(V-) - 0.3 V to (V) + 0.3 V	
Current (Any Terminal Except S or D)	30	mA
Continuous Current, S or D)	100	
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max).	200	
Package Solder Reflow Conditions ^b	IR/Convection	°C
Storage Temperature	- 65 to 150	
Power Dissipation (Package) ^c , (T _A = 70 °C)	16-Bump (4 x 4 mm) MICRO FOOT ^d	mW

Notes:

a. Signals on S_X, D_X or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. Refer to IPC/JEDEC (J-STD-020B).

c. All bumps soldered or welded to PC board.

d. Derate 9.0 mW/°C above 70 °C.



SPECIFICATIONS (Single Supply 12 V)							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, ± 10 %, V- = 0 V VA, VEN = 0.8 V or 2.4 V ^f	Temp. ^b	Limits - 40 °C to 85 °C			Unit
				Min. ^c	Typ. ^d	Max. ^e	
Analog Switch							
Analog Signal Range ^e	VANALOG		Full	0		12	V
On-Resistance	RON	V+ = 10.8 V, VD = 2 V or 9 V, IS = 50 mA Sequence Each Switch On	Room Full		4	7 7.5	Ω
RON Match Between Channels ^g	ΔRON	V+ = 10.8 V, VD = 2 V or 9 V, IS = 50 mA	Room			3.6	
On-Resistance Flatness ⁱ	RON Flatness		Room			8	
Switch Off Leakage Current	IS(off)	VEN = 2.4 V, VD = 11 V or 1 V, VS = 1 V or 11 V	Room Full	- 2 - 20		2 20	nA
	ID(off)		Room Full	- 2 - 20		2 20	
Channel On Leakage Current	ID(on)	VEN = 0 V, VS = VD = 1 V or 11 V	Room Full	- 2 - 20		2 20	
Digital Control							
Logic High Input Voltage	VINH		Full	2.4			V
Logic Low Input Voltage	VINL		Full			0.8	
Input Current	IIN	VAX = VEN = 2.4 V or 0.8 V	Full	- 1		1	μA
Dynamic Characteristics							
Transition Time	tTRANS	VS1 = 8 V, VS8 = 0 V, (DG3408) VS1b = 8 V, VS4b = 0 V, (DG3409) see figure 2	Room Full		42	71 75	ns
Break-Before-Make Time	tBBM	VS(all) = VDA = 5 V see figure 4	Room Full	2	24		
Enable Turn-On Time	tON(EN)	VAX = 0 V, VS1 = 5 V (DG3408) VAX = 0 V, VS1b = 5 V (DG3409) see figure 3	Room Full		42	70 75	
Enable Turn-Off Time	tOFF(EN)		Room Full		24	44 46	
Charge Injection ^e	Q	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω	Room		29		pC
Off Isolation ^{e, h}	OIRR	f = 100 kHz, RL = 1 kΩ	Room		- 80		dB
Crosstalk ^e	XTALK		Room		- 85		
Source Off Capacitance ^e	CS(off)	f = 1 MHz, VS = 0 V, VEN = 2.4 V	DG3408	Room		21	pF
			DG3409	Room		23	
Drain Off Capacitance ^e	CD(off)	f = 1 MHz, VD = 0 V, VEN = 2.4 V	DG3408	Room		211	
			DG3409	Room		112	
Drain On Capacitance ^e	CD(on)	f = 1 MHz, VD = 0 V, VEN = 0 V	DG3408	Room		238	
			DG3409	Room		137	
Power Supplies							
Power Supply Current	I+	VEN = VA = 0 V or V+	Room			1.0	μA

SPECIFICATIONS (Dual Supply V+ = 5 V, V- = - 5 V)							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V- = - 5 V, ± 10 % VA, VEN = 0.8 V or 2.0 V ^f	Temp. ^b	Limits - 40 °C to 85 °C			Unit
				Min. ^c	Typ. ^d	Max. ^c	
Analog Switch							
Analog Signal Range ^e	VANALOG		Full	- 5		5	V
On-Resistance	RON	V+ = 4.5 V, V- = - 4.5 V, VD = ± 3.5 V, IS = 50 mA, sequence each switch on	Room Full		5	8 8.5	Ω
rON Match Between Channels ^g	ΔRON	V+ = 4.5 V, V- = - 4.5 V, VD = ± 3.5 V, IS = 50 mA	Room			3.6	
On-Resistance Flatness ⁱ	RON Flatness		Room			8.2	
Switch Off Leakage Current ^a	IS(off)	V+ = 5.5, V- = - 5.5 V VEN = 2.4 V, VD = ± 4.5 V, VS = ± 4.5 V	Room Full	- 2 - 20		2 20	nA
	ID(off)		Room Full	- 2 - 20		2 20	
Channel On Leakage Current ^a	ID(on)	V+ = 5.5 V, V- = - 5.5 V VEN = 0 V, VD = ± 4.5 V, VS = ± 4.5 V	Room Full	- 2 - 20		2 20	
Digital Control							
Logic High Input Voltage	VINH		Full	2.0			V
Logic Low Input Voltage	VINL		Full			0.8	
Input Current ^a	IIN	VAX = VEN = 2.0 V or 0.8 V	Full	- 1		1	μA
Dynamic Characteristics							
Transition Time ^e	tTRANS	VS1 = 3.5 V, VS8 = - 3.5 V, (DG3408) VS1b = 3.5 V, VS4b = - 3.5 V, (DG3409) see figure 2	Room Full		68	89 94	ns
Break-Before-Make Time ^e	tBBM	VS(all) = VDA = 3.5 V see figure 4	Room Full	1	16		
Enable Turn-On Time ^e	tON(EN)	VAX = 0 V, VS1 = 3.5 V (DG3408) VAX = 0 V, VS1b = 3.5 V (DG3409) see figure 3	Room Full		68	88 94	
Enable Turn-Off Time ^e	tOFF(EN)		Room Full		58	78 81	
Source Off Capacitance ^e	CS(off)	f = 1 MHz, VS = 0 V, VEN = 2.0 V	DG3408 Room		23		pF
Drain Off Capacitance ^e	CD(off)	f = 1 MHz, VD = 0 V, VEN = 2.0 V	DG3409 Room		23		
			DG3408 Room		223		
Drain On Capacitance ^e	CD(on)	f = 1 MHz, VD = 0 V, VEN = 0 V	DG3409 Room		113		
			DG3408 Room		246		
		DG3409 Room		137			
Power Supplies							
Power Supply Current	I+	VEN = VA = 0 V or V+	Room			1.0	μA
	I-		Room	- 1.0			



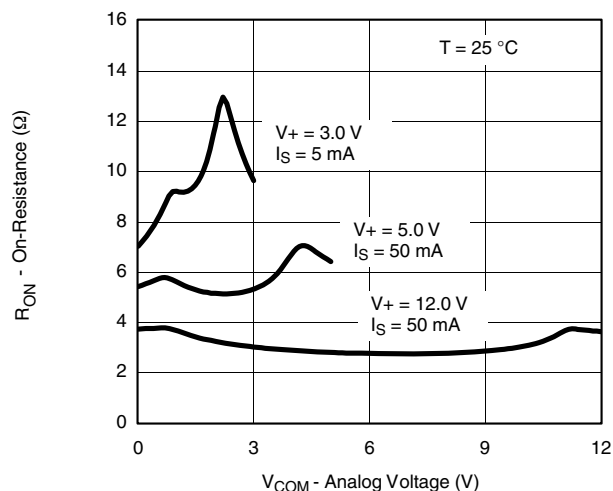
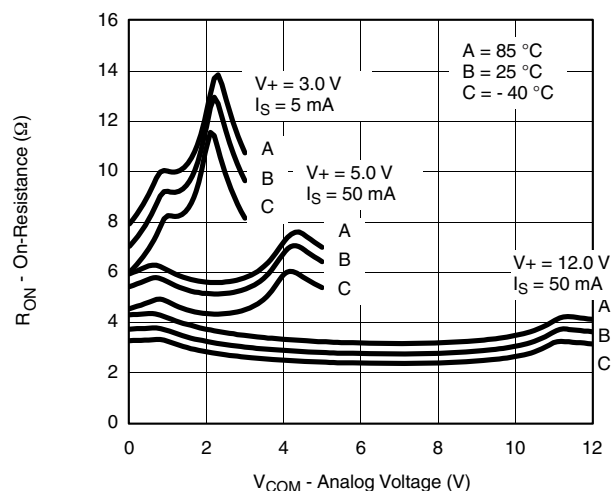
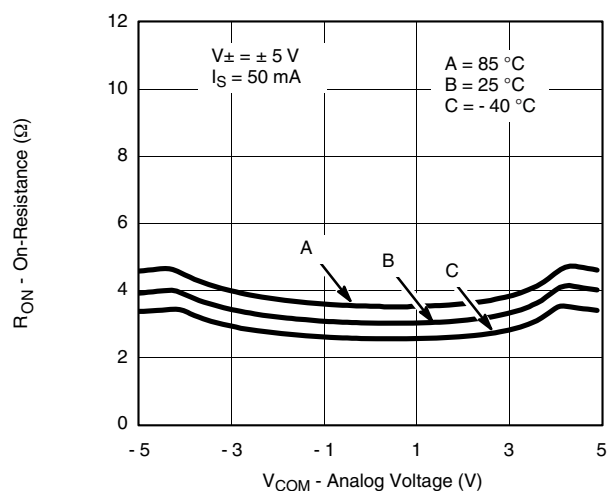
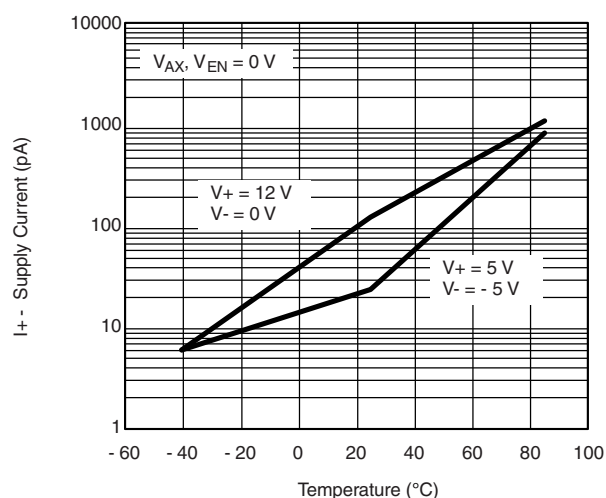
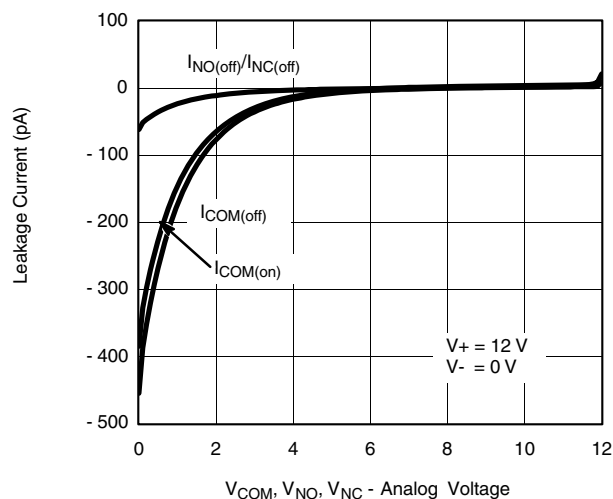
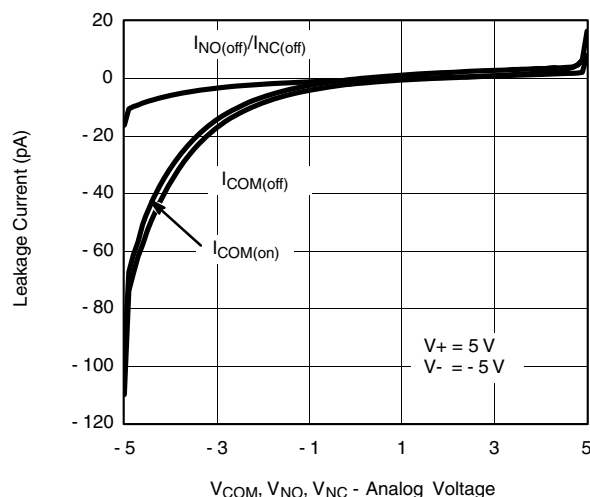
SPECIFICATIONS (Single Supply 5 V)								
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, ± 10 %, V- = 0 V VA, VEN = 0.8 V or 2.0 V ^f		Temp. ^b	Limits - 40 °C to 85 °C			Unit
					Min. ^c	Typ. ^d	Max. ^c	
Analog Switch								
Analog Signal Range ^e	VANALOG			Full	0		5	V
On-Resistance	RON	V+ = 4.5 V, VD or VS = 1 V or 3.5 V, IS = 50 mA		Room Full		7	10.5 11	Ω
rON Match Between Channels ^g	ΔRON	V+ = 4.5 V, VD = 1 V or 3.5 V, IS = 50 mA		Room			3.6	
On-Resistance Flatness ⁱ	RON Flatness			Room			9	
Switch Off Leakage Current ^a	IS(off)	V+ = 5.5 V VS = 1 V or 4 V, VD = 4 V or 1 V		Room Full	- 2 - 20		2 20	nA
	ID(off)			Room Full	- 2 - 20		2 20	
Channel On Leakage Current ^a	ID(on)	V+ = 5.5 V VD = VS = 1 V or 4 V, sequence each switch on		Room Full	- 2 - 20		2 20	
Digital Control								
Logic High Input Voltage	VINH	V+ = 5 V		Full	2.0			V
Logic Low Input Voltage	VINL			Full			0.8	
Input Current ^a	IIN	VAX = VEN = 2.0 V or 0.8 V		Full	- 1		1	μA
Dynamic Characteristics								
Transition Time ^e	tTRANS	VS1 = 3.5 V, VS8 = 0 V, (DG3408) VS1b = 3.5 V, VS4b = 0 V, (DG3409) see figure 2		Room Full		73	94 104	ns
Break-Before-Make Time ^e	tOPEN	VS(all) = VDA = 3.5 V see figure 4		Room Full	2	29		
Enable Turn-On Time ^e	tON(EN)	VAX = 0 V, VS1 = 3.5 V (DG3408) VAX = 0 V, VS1b = 3.5 V (DG3409) see figure 3		Room Full		74	94 104	
Enable Turn-Off Time ^e	tOFF(EN)			Room Full		38	57 61	
Charge Injection ^e	Q	CL = 1 nF, RGEN = 0 Ω, VGEN = 0 V		Room		20		pC
Off Isolation ^{e, h}	OIRR	RL = 1 kΩ, f = 100 kHz		Room		- 81		dB
Crosstalk ^e	XTALK			Room		- 85		
Source Off Capacitance ^e	CS(off)	f = 1 MHz, VS = 0 V, VEN = 0 V	DG3408	Room		22		pF
			DG3409	Room		24		
Drain Off Capacitance ^e	CD(off)	f = 1 MHz, VD = 0 V, VEN = 2.0 V	DG3408	Room		223		
			DG3409	Room		113		
Drain On Capacitance ^e	CD(on)	f = 1 MHz, VD = 0 V, VEN = 0 V	DG3408	Room		244		
			DG3409	Room		143		
Power Supplies								
Power Supply Current	I+	VEN = VA = 0 V or V+		Room			1.0	μA

SPECIFICATIONS (Single Supply 3 V)							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3 V, ± 10 %, V- = 0 V V _{EN} = 0.4 V or 1.8 V ^f	Temp ^b	Limits - 40 °C to 85 °C			Unit
				Min ^c	Typ ^d	Max ^c	
Analog Switch							
Analog Signal Range ^e	V _{ANALOG}		Full	0		3	V
On-Resistance	R _{ON}	V+ = 2.7 V, V _D = 0.5 or 2.2 V, I _S = 5 mA	Room Full		12	25.5 26.5	Ω
R _{ON} Match Between Channels ^g	ΔR _{ON}	V+ = ± 2.7 V, V _D = 0.5 V or 2.2 V, I _S = 5 mA	Room			3.6	
On-Resistance Flatness ⁱ	R _{ON} Flatness		Room			13	
Switch Off Leakage Current ^a	I _{S(off)}	V+ = 3.3 V V _S = 2 or 1 V, V _D = 1 or 2 V	Room Full	- 2 - 20		2 20	nA
	I _{D(off)}		Room Full	- 2 - 20		2 20	
Channel On Leakage Current ^a	I _{D(on)}	V+ = 3.3 V V _D = V _S = 1 or 2 V, sequence each switch on	Room Full	- 2 - 20		2 20	
Digital Control							
Logic High Input Voltage	V _{INH}		Full	1.8			V
Logic Low Input Voltage	V _{INL}		Full			0.4	
Input Current ^a	I _{IN}	V _{AX} = V _{EN} = 1.8 V or 0.4 V	Full	- 1		1	μA
Dynamic Characteristics							
Transition Time	t _{TRANS}	V _{S1} = 1.5 V, V _{S8} = 0 V, (DG3408) V _{S1b} = 1.5 V, V _{S4b} = 0 V, (DG3409) see figure 2	Room Full		140	165 182	ns
Break-Before-Make Time	t _{BBM}	V _{S(all)} = V _{DA} = 1.5 V see figure 4	Room Full	2	63		
Enable Turn-On Time	t _{ON(EN)}	V _{AX} = 0 V, V _{S1} = 1.5 V (DG3408) V _{AX} = 0 V, V _{S1b} = 1.5 V (DG3409) see figure 3	Room Full		140	162 178	
Enable Turn-Off Time	t _{OFF(EN)}		Room Full		76	97 104	
Charge Injection ^e	Q	C _L = 1 nF, R _{GEN} = 0, V _{GEN} = 0 V	Room		7		pC
Off Isolation ^{e, h}	OIRR	f = 100 kHz, R _L = 1 kΩ	Room		- 81		dB
Crosstalk ^e	X _{TALK}		Room		- 85		
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz, V _S = 0 V, V _{EN} = 1.8 V	DG3408	Room	23		pF
			DG3409	Room	25		
Drain Off Capacitance ^e	C _{D(off)}	f = 1 MHz, V _D = 0 V, V _{EN} = 1.8 V	DG3408	Room	230		
			DG3409	Room	120		
Drain On Capacitance ^e	C _{D(on)}	f = 1 MHz, V _D = 0 V, V _{EN} = 0 V	DG3408	Room	256		
			DG3409	Room	147		
Power Supplies							
Power Supply Current	I+	V _{EN} = V _A = 0 V or V+	Room			1.0	μA

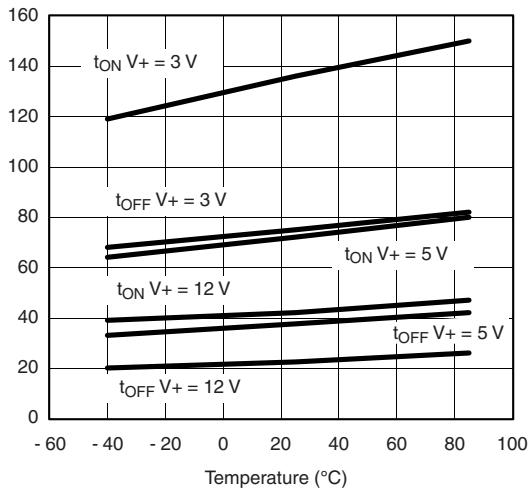
Notes:

- Leakage parameters are guaranteed by worst case test condition and not subject to production test.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.
- $\Delta R_{\text{DON}} = R_{\text{DON Max}} - R_{\text{DON Min}}$.
- Worst case isolation occurs on Channel 4 due to proximity to the drain pin.
- R_{DON} flatness is measured as the difference between the minimum and maximum measured values across a defined Analog signal.

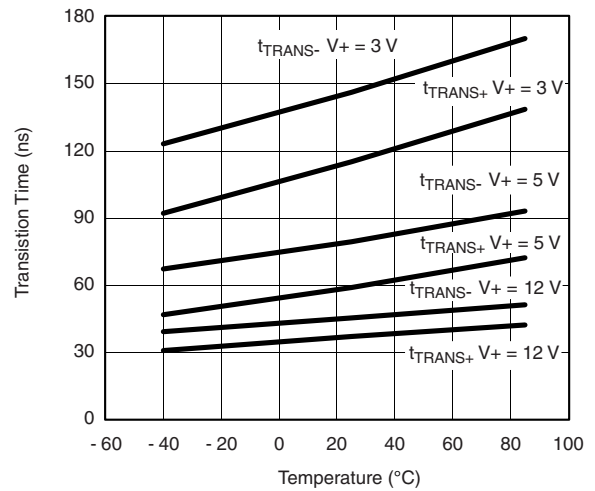
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

 R_{ON} vs. V_{COM} and Single Supply Voltage

 R_{ON} vs. Analog Voltage and Temperature

 R_{ON} vs. Analog Voltage and Temperature

Supply Current vs. Temperature

Leakage Current vs. Analog Voltage

Leakage Current vs. Analog Voltage

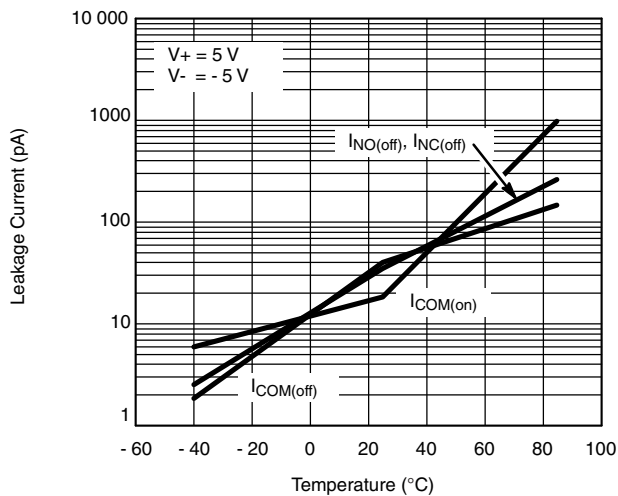
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



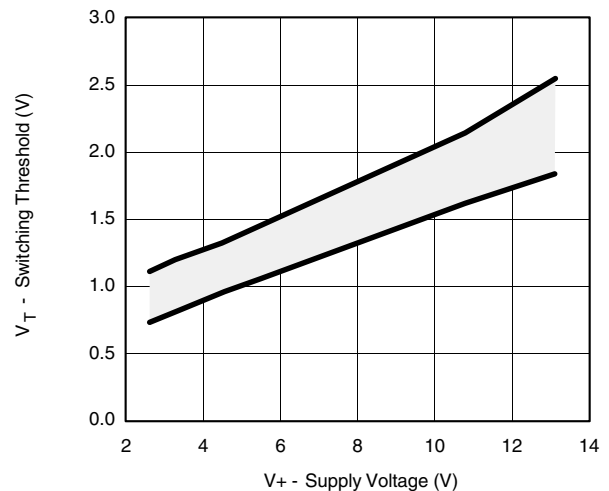
Switching Time vs. Temperature and Single Supply Voltage



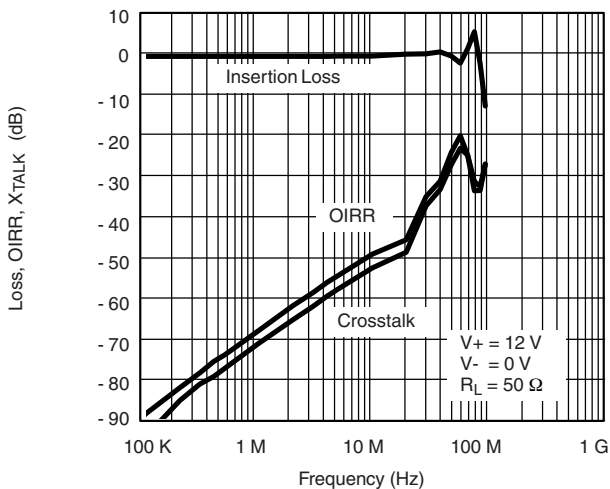
Transition Time vs. Temperature and Single Supply Voltage



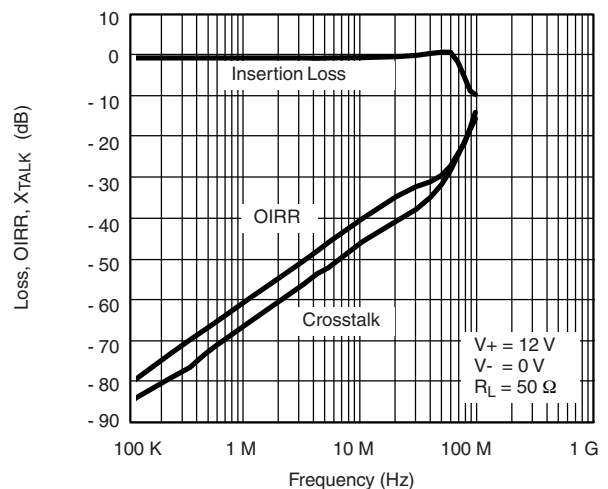
Leakage Current vs. Temperature



Switching Threshold vs. Supply Voltage

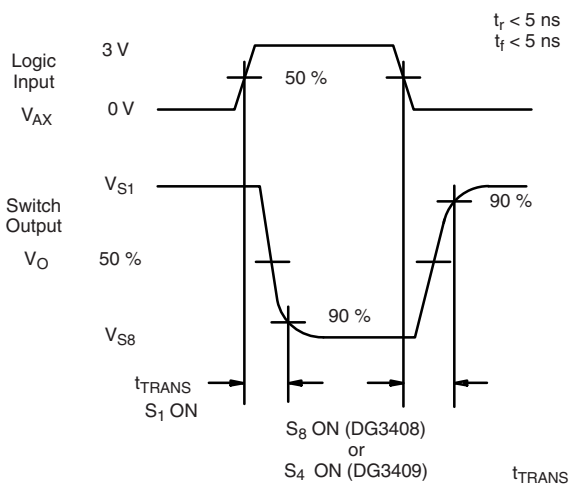
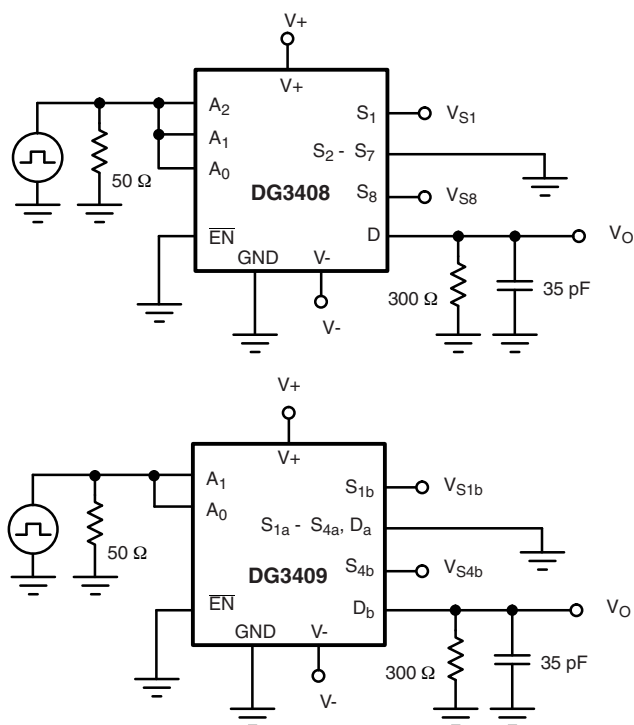


Insertion Loss, Off Isolation and Crosstalk vs. Frequency (DG3408)



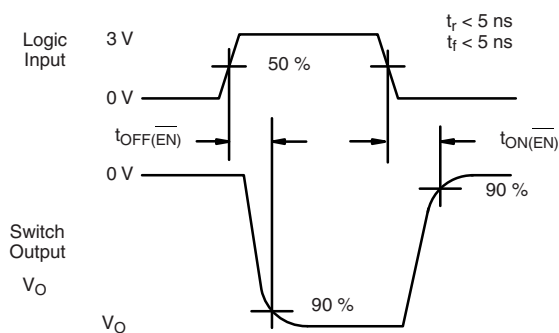
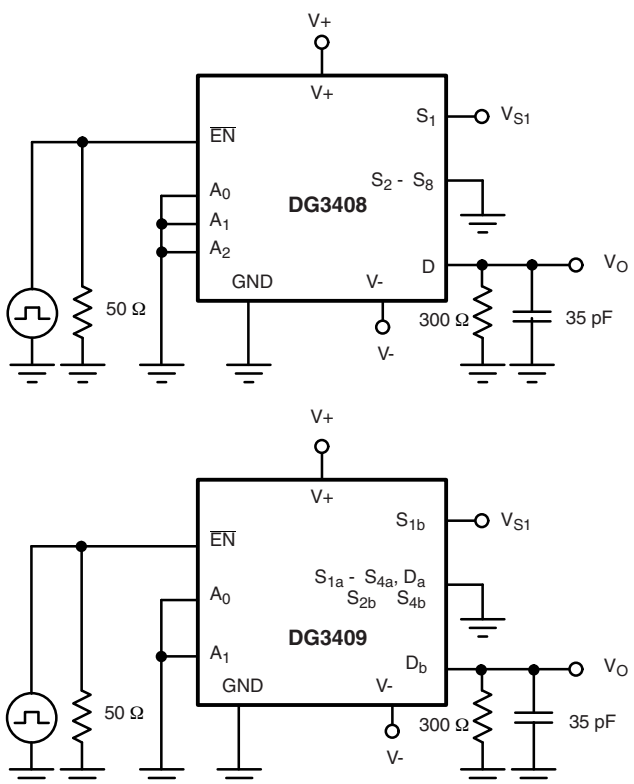
Insertion Loss, Off Isolation and Crosstalk vs. Frequency (DG3409)

TEST CIRCUITS



Return to Specifications:
 Single Supply 12 V
 Dual Supply $V_+ = 5\text{ V}$, $V_- = -5\text{ V}$
 Single Supply 5 V
 Single Supply 3 V

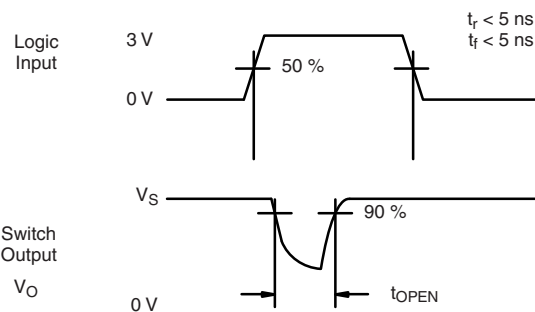
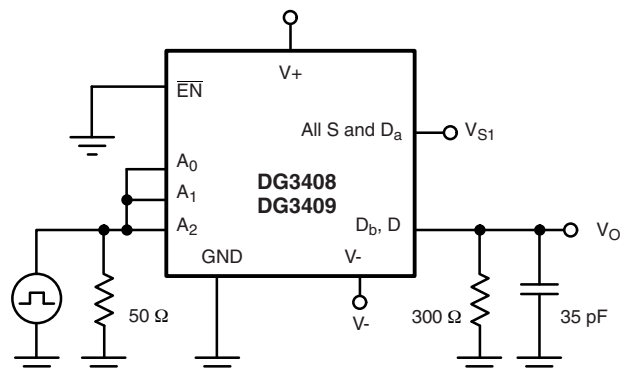
Figure 2. Transition Time



Return to Specifications:
 Single Supply 12 V
 Dual Supply $V_+ = 5\text{ V}$, $V_- = -5\text{ V}$
 Single Supply 5 V
 Single Supply 3 V

Figure 3. Enable Switching Time

TEST CIRCUITS



Return to Specifications:
 Single Supply 12 V
 Dual Supply $V_+ = 5\text{ V}$, $V_- = -5\text{ V}$
 Single Supply 5 V
 Single Supply 3 V

Figure 4. Break-Before-Make Interval

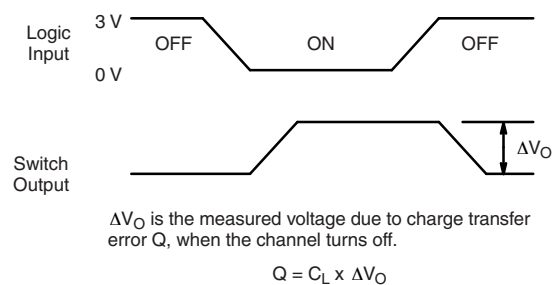
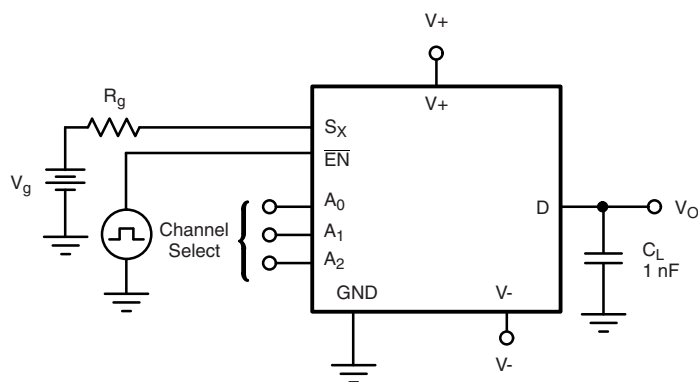


Figure 5. Charge Injection

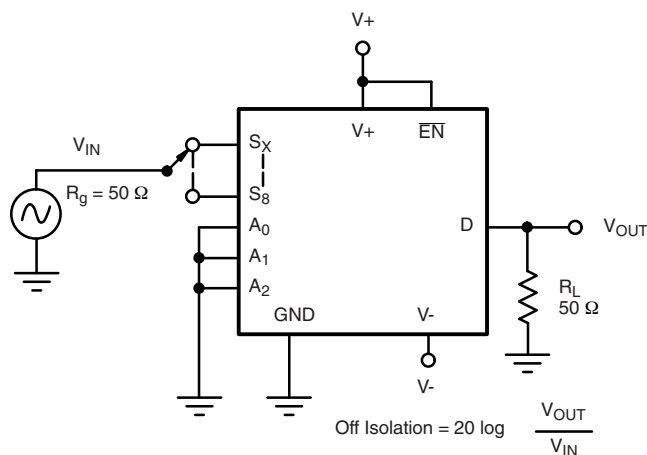


Figure 6. Off Isolation

TEST CIRCUITS

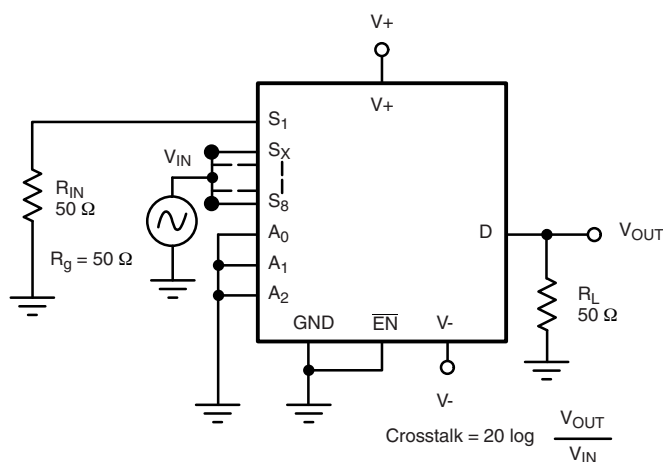


Figure 7. Crosstalk

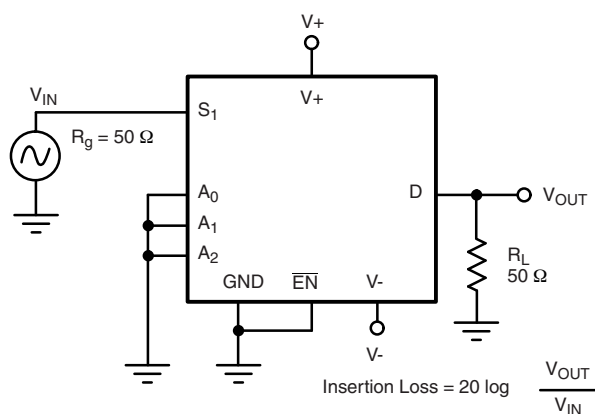


Figure 8. Insertion Loss

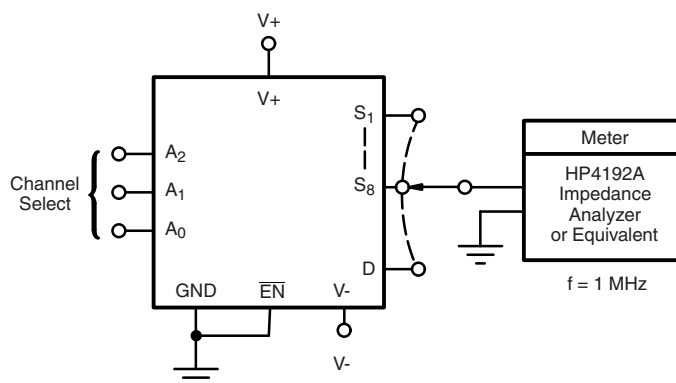
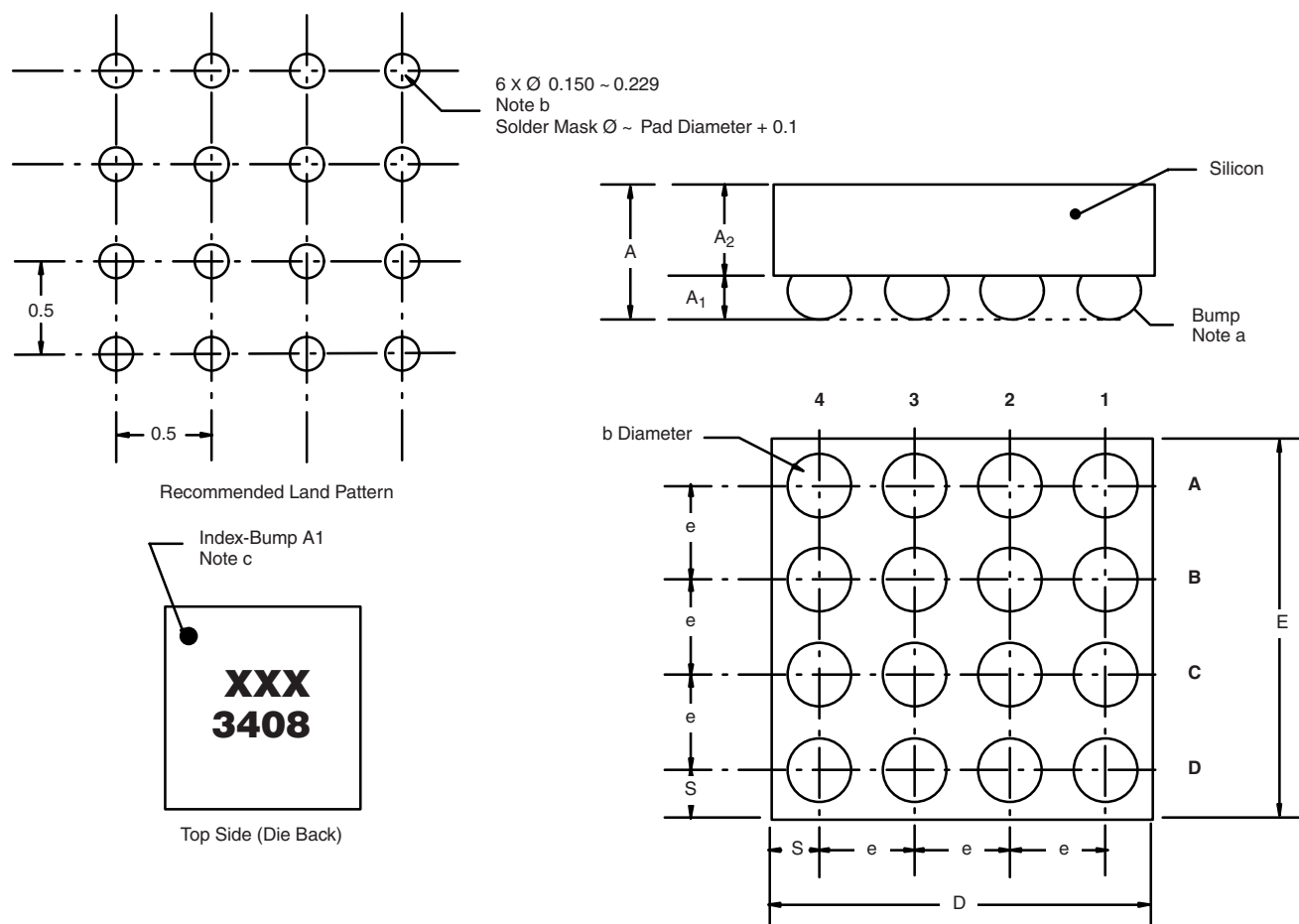


Figure 9. Source Drain Capacitance

PACKAGE OUTLINE
MICRO FOOT: 16-BUMP (4 x 4, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)


Notes (Unless Otherwise Specified):

- a. Bump is Lead Free Sn/Ag/Cu.
- b. Non-solder mask defined copper landing pad.
- c. Laser Mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

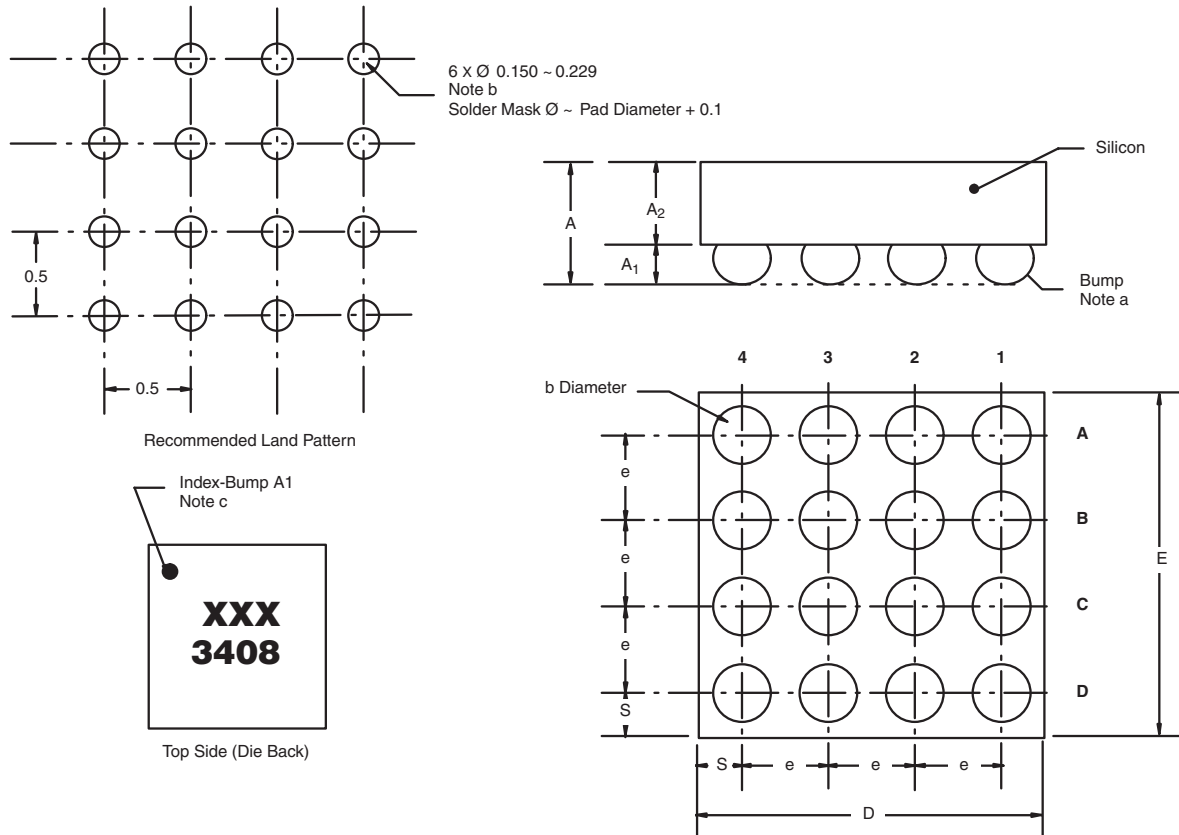
Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.688	0.753	0.0271	0.0296
A₁	0.218	0.258	0.0086	0.0102
A₂	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.980	2.020	0.0780	0.0795
E	1.980	2.020	0.0780	0.0795
e	0.5 BASIC		0.0197 BASIC	
S	0.230	0.270	0.0091	0.0106

Notes:

- a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72858.

MICRO FOOT: 16-BUMP (4 mm x 4 mm, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Notes

(unless otherwise specified)

- Bump is lead (Pb)-free Sn/Ag/Cu.
- Non-solder mask defined copper landing pad.
- Laser mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

DIM.	MILLIMETERS ^a		INCHES	
	MIN.	MAX.	MIN.	MAX.
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Note

- Use millimeters as the primary measurement.

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DWG: 6000



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