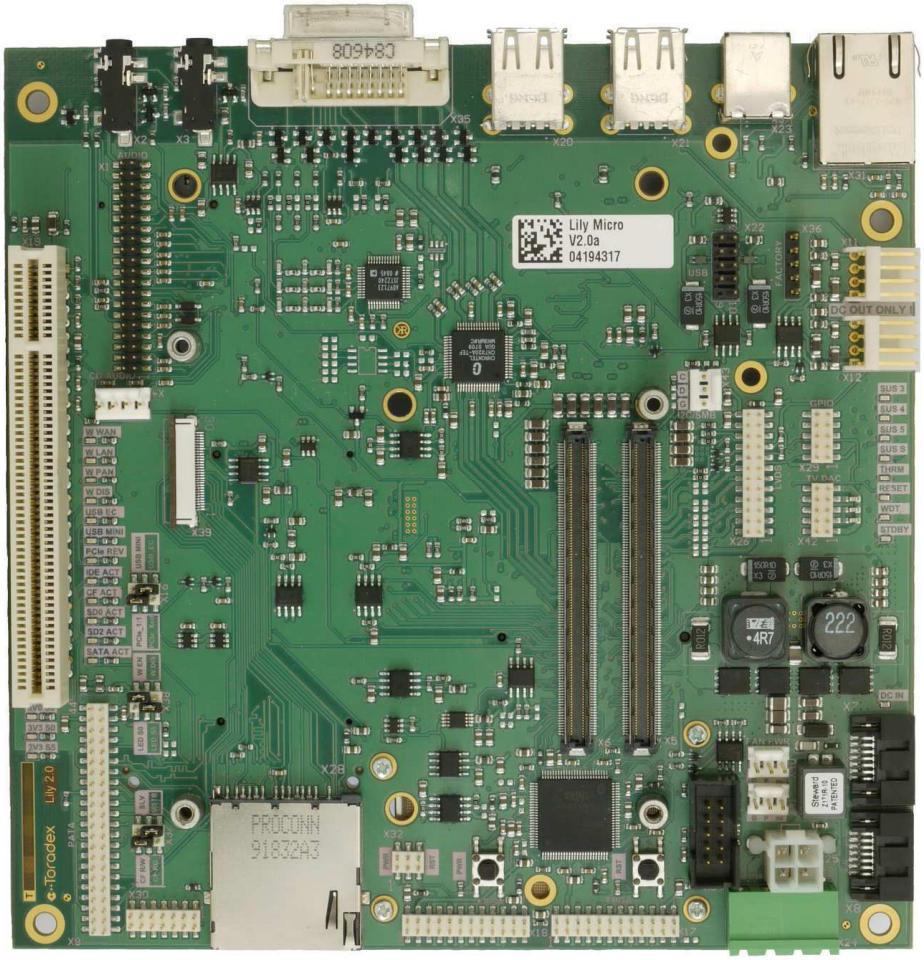
Lily V2.0 COM Express Baseboard

Datasheet



Revision History

Date	Doc. Rev.	Lily Version	Changes
05-Aug-09	Rev. 0.9	V2.00	Initial Release
07-Sept-09	Rev. 0.91	V2.00	LVDS header X26
01-Feb-11	Rev. 1.0	V2.0	New Disclaimer

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1. Introduction

Lily is a COM Express compliant carrier board that allows the convenient evaluation of Woodpecker and Robin COM Express computer modules. Since the Robin Module features only one COM Express Connector, a different assembly version of the Lily is needed for using the Robin module.

1.1. Reference Documents

For detailed technical information about suitable computer modules and the COM Express™ standard, please refer to the documents listed below.

1.1.1 COM Express™ Design Guide

Guidelines for designing a COM Express™ carrier board
http://www.picmg.org/pdf/PICMG_COMDG_100.pdf

1.1.2 Woodpecker Computer Module

http://www.toradex.com/En/Products/Woodpecker_modules

1.1.3 Robin Computer Module

http://www.toradex.com/En/Products/Robin_Z530_Z510

2. Features

2.1. Overview

Lily Micro implements all the peripherals required to evaluate COM Express Type 2 compliant modules such as the Toradex Woodpecker modules.

- Power management
- Connectivity such as USB, Ethernet, PATA, CF Card & SATA
- Video ports (VGA/DVI) on a DVI-I Connector
- A SDVO to DVI converter
- HD-Audio functionality with pin headers carrying all (unfiltered) analog signals
- GPIO header
- Mini PCIe including SIM holder for wireless modems

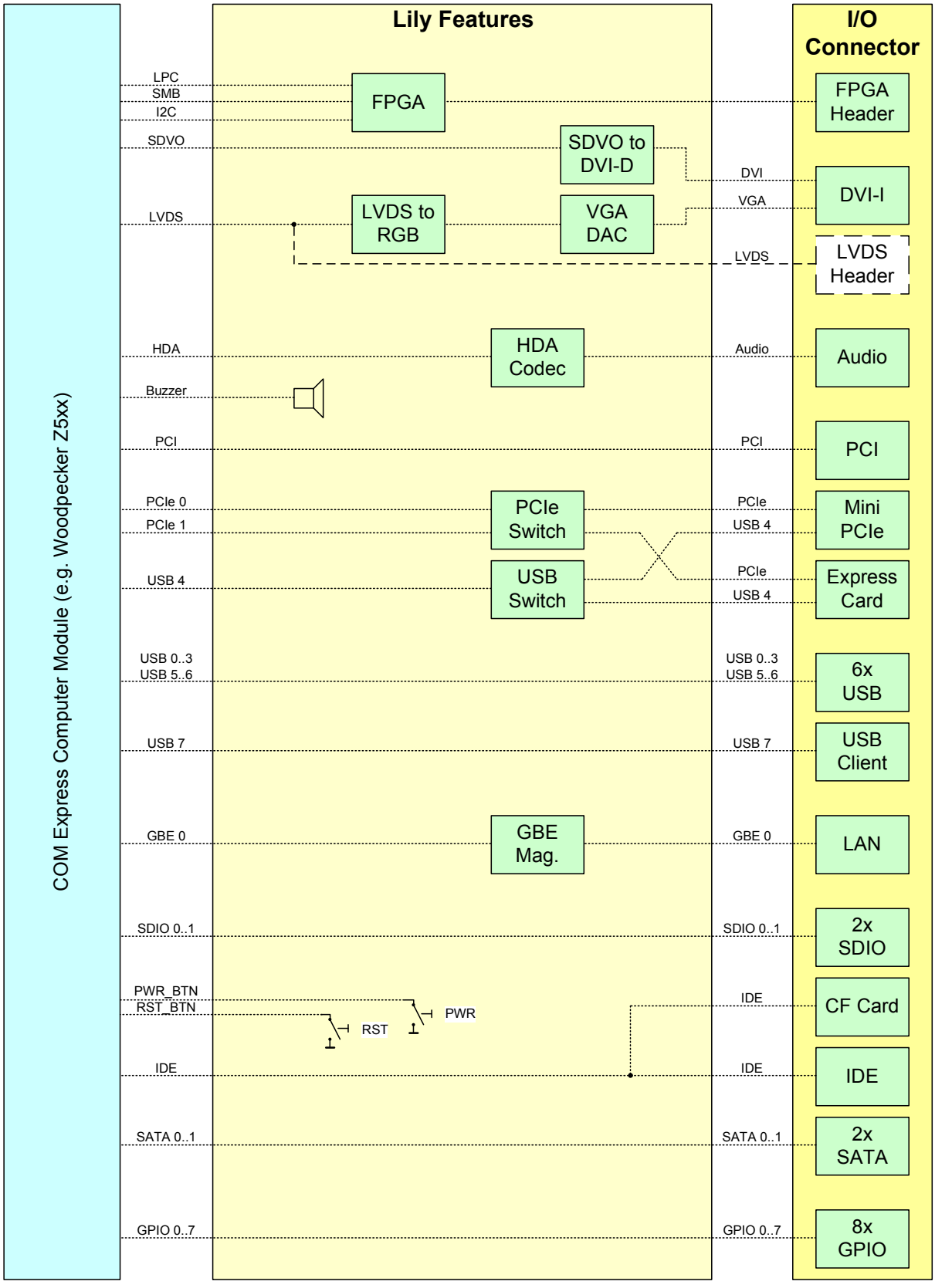
In addition to the usual features of a COM Express carrier board, Lily offers several unique enhancements not found on other evaluation platforms:

- A Xilinx Spartan 3A100 FPGA is tied to the LPC, I2C and SMB bus. The FPGA is fully user configurable and can be used for bus expansions or system management
- A LVDS to RGB converter in combination with a RGB to VGA DAC provides the VGA output of the DVI-I connector
- Two SDIO card slots, one of which (X8) with support for 8 bit wide data transfers
- Express-Card slot with card cage supporting 54mm and 34mm cards
- PCI-Express Lane switch

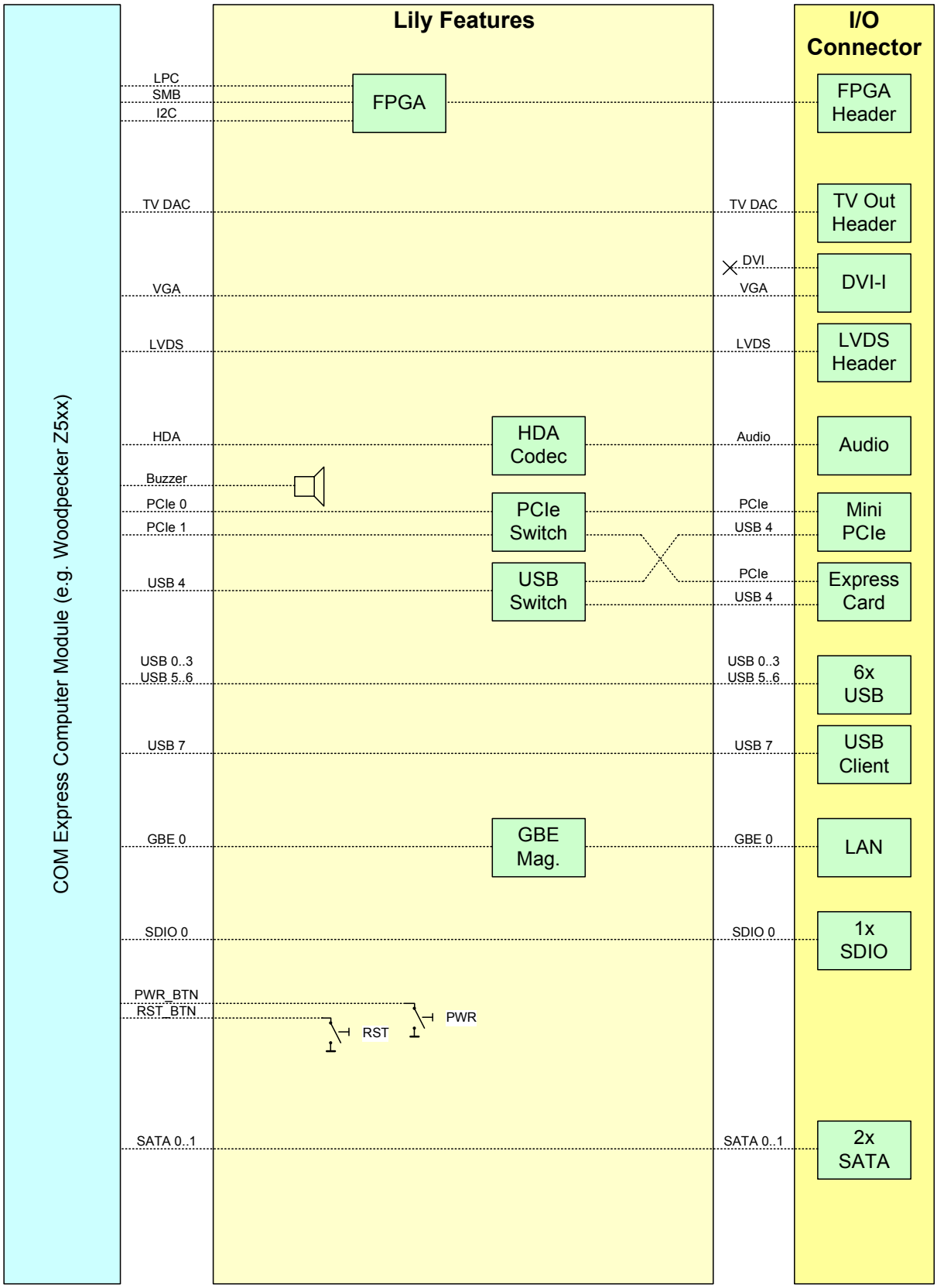
The Lily Nano is designed for COM Express Type 1 modules in the Nano form factor such as the Toradex Robin module. Due to the missing second module connector some of the Lily Micro features are not available.

2.2. Block Diagram

2.2.1 Lily Micro

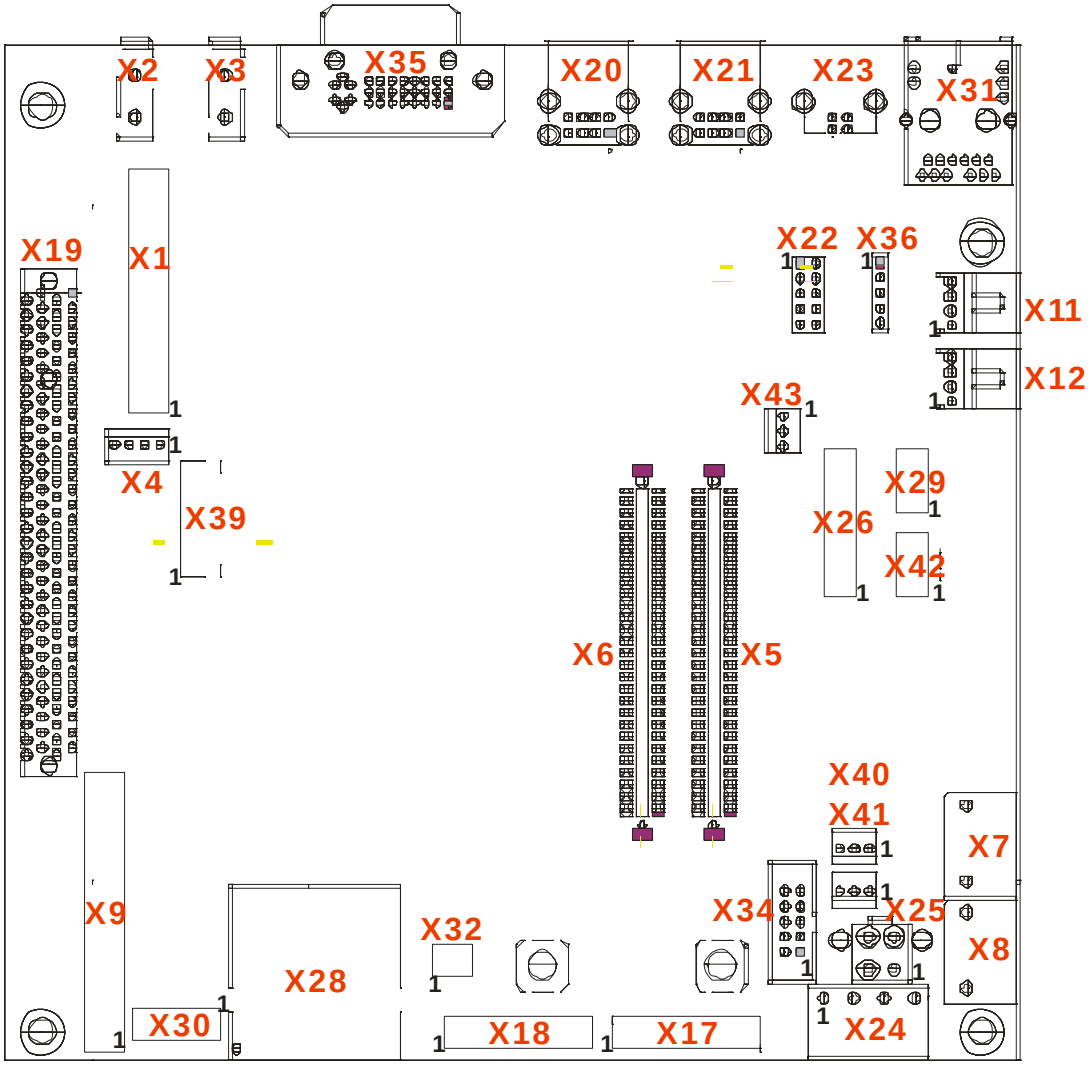


2.2.2 Lily Nano



3. Interfaces

3.1. Upper Side Connectors: Physical Drawing



	Description	Lily Micro	Lily Nano	Remarks
X1	Audio Header	X	X	
X2	Mic 2 Jack	X	X	
X3	Line 2 Jack	X	X	
X4	CD Audio Input	X	X	
X5	COM Express Connector Row AB	X	X	
X6	COM Express Connector Row CD	X		
X7	SATA 0	X	X	
X8	SATA 1	X	X	SATA 1 not supported by Robin
X9	IDE (PATA)	X		
X11	Hard Disk Power Out	X	X	12V is UNREGULATED!
X12	Hard Disk Power Out	X	X	12V is UNREGULATED!

	Description	Lily Micro	Lily Nano	Remarks
X17	FPGA Expansion Header Bank 3	X	X	
X18	FPGA Expansion Header Bank 0	X	X	
X19	PCI	X		12V is UNREGULATED!
X20	USB Ports 0 and 1	X	X	
X21	USB Ports 2 and 3	X	X	
X22	USB Ports 5 and 6	X	X	
X23	USB Client (USB Port 7)	X	X	
X24	DC IN 8 – 14V	X	X	12V if PCI or HD power used!
X25	ATX DC IN 8 – 14V	X	X	12V if PCI or HD power used!
X26	LVDS Header	X	X	
X28	8bit MMC / SDIO 2	X	X	
X29	GPIO	X		
X30	FPGA JTAG Header	X	X	
X31	Ethernet Jack	X	X	
X32	External Reset and Power Button Header	X	X	
X34	Micro Controller Debug Header	X	X	
X35	DVI-I	X	X	Nano: only DVI-A
X36	PSoC Programming Adaptor Header	X		
X39	Additional FFC Connector for SDIO	X	X	
X40	Switched Fan 12V Power	X	X	12V is UNREGULATED!
X41	Switched Fan 12V Power	X	X	12V is UNREGULATED!
X42	TV DAC	X	X	Not supported by Woodpecker
X43	I^2C Header	X	X	

3.2. Upper Side Connectors: Pin Assignments

3.2.1 Audio Header (X1)

Pin	Description	Voltage	Active	Remarks
1	GND			
2	SUR L			
3	VREF A			
4	SUR R			
5	GND			
6	MIC 1 L			
7	MIC 1 BIAS L			
8	MIC 1 R			
9	MIC 1 BIAS R			
10	GND			
11	FRONT L			
12	FRONT R			
13	GND			
14	MIC 2 L			Only if no Plug in X2
15	MIC 2 VREF			
16	MIC 2 R			Only if no Plug in X2
17	GND			
18	CENTER			
19	LOW FREQ			
20	GND			
21	SIDE L			
22	SIDE R			
23	GND			
24	LINE 1 L			
25	VREF C			
26	LINE 1 R			
27	GND			
28	LINE 2 L			Only if no Plug in X3
29	VREF E			
30	LINE2 R			Only if no Plug in X2
31	GND			
32	GND			
33	S/PDIF IN	3.3V		
34	S/PDIF OUT	3.3V		
35	GND			
36	SENSE B			

Pin	Description	Voltage	Active	Remarks
37	SENSE A			
38	GND			
39	GND			
40	+5V OUT	5V	S0	For S/PDIF

3.2.2 CD Audio (X4)

Pin	Description	Voltage	Active	Remarks
1	CD AUDIO L			ANALOG
2	DC AUDIO GND			
3	DC AUDIO GND			
4	CD AUDIO R			ANALOG

3.2.3 PATA Header (X9)

Pin	Description	Voltage	Active	Remarks
1	IDE RESET#	3.3V		
2	GND			
3	IDE D7	3.3V		
4	IDE D8	3.3V		
5	IDE D6	3.3V		
6	IDE D9	3.3V		
7	IDE D5	3.3V		
8	IDE D10	3.3V		
9	IDE D4	3.3V		
10	IDE D11	3.3V		
11	IDE D3	3.3V		
12	IDE D12	3.3V		
13	IDE D2	3.3V		
14	IDE D13	3.3V		
15	IDE D1	3.3V		
16	IDE D14	3.3V		
17	IDE D0	3.3V		
18	IDE D15	3.3V		
19	GND			
20	NC			
21	IDE REQ	3.3V		
22	GND			
23	IDE IOW#	3.3V		
24	GND			
25	IDE IOR#	3.3V		
26	GND			
27	IDE IORDY#	3.3V		
28	PD TO GND			

Pin	Description	Voltage	Active	Remarks
29	IDE ACK#	3.3V		
30	GND			
31	IDE IRQ	3.3V		
32	NC			
33	IDE A1	3.3V		
34	IDE CBLID#	3.3V		
35	IDE A0	3.3V		
36	IDE A2	3.3V		
37	IDE CS1#	3.3V		
38	IDE CS3#	3.3V		
39	IDE ACTIVE	3.3V		
40	GND	3.3V		
41	+5V DRIVE	+5V	S0	
42	+5V DRIVE	+5V	S0	
43	GND			
44	NC			

3.2.4 Hard Disk Power Out (X11/X12)

Pin	Description	Voltage	Active	Remarks
1	12V Output Unregulated	12V	S0	
2	GND			
3	GND			
4	5V Output	5V	S0	

3.2.5 FPGA Expansion Header Bank 3 (X17)

Pin	Description	Voltage	Active	Remarks
1	3.3V Output	3.3V	S0	
2	3.3V Output	3.3V	S0	
3	Bank 3 IO Power Input (default assembly: 0R to 3.3V)			NC[1]
4	Bank 3 IO Power Input (default assembly: 0R to 3.3V)			NC
5	B3_0			
6	B3_1			
7	B3_2			
8	B3_3			
9	GND			
10	B3_4			
11	B3_5			
12	B3_6			
13	B3_7			

[1] Since 0R to 3.3V is assembled on baseboard these pins can be left unconnected. If other IO levels required, unsolder 0R and supply IO bank voltage with this pin.

Pin	Description	Voltage	Active	Remarks
14	GND			
15	B3_8			
16	B3_9			
17	B3_10			
18	GND			
19	B3_11			
20	B3_12			
21	B3_13			
22	5V Output	5V	S0	
23	5V Output	5V	S0	
24	5V Output	5V	S0	

3.2.6 FPGA Expansion Header Bank 0 (X18)

Pin	Description	Voltage	Active	Remarks
1	3.3V Output	3.3V	S0	
2	3.3V Output	3.3V	S0	
3	Bank 0 IO Power Input (default assembly: 0R to 3.3V)			NC[2]
4	Bank 0 IO Power Input (default assembly: 0R to 3.3V)			NC
5	B0_0			
6	B0_1			
7	B0_2			
8	B0_3			
9	GND			
10	B0_4			
11	B0_5			
12	B0_6			
13	B0_7			
14	GND			
15	B0_8			
16	B0_9			
17	B0_10			
18	GND			
19	B0_11			
20	B0_12			
21	B0_13			
22	5V Output	5V	S0	
23	5V Output	5V	S0	
24	5V Output	5V	S0	

[2] Since 0R to 3.3V is assembled on baseboard these pins can be left unconnected. If other IO levels required, unsolder 0R and supply IO bank voltage with this pin.

3.2.7 DC IN 8-14V (X24)

Pin	Description	Voltage	Active	Remarks
1	+12V IN	8-14V DC		CAUTION[3]
2	+12V IN	8-14V DC		CAUTION
3	GND			
4	GND			

3.2.8 ATX DC IN 8-14V (X25)

This connector can be used alternatively to X24 to supply the module. The connector is compatible with the 2x2 ATX 12V Connector

Pin	Description	Voltage	Active	Remarks
1	GND			
2	GND			
3	+12V IN	8-14V DC		CAUTION[4]
4	+12V IN	8-14V DC		CAUTION

3.2.9 LVDS Header (X26)

Pin	Description	Voltage	Active	Remarks
1	LVDS A0 P			Micro NA[5]
2	LVDS A0 N			Micro NA
3	GND			
4	LVDS A1 P			Micro NA
5	LVDS A1 N			Micro NA
6	GND			
7	LVDS A2 P			Micro NA
8	LVDS A2 N			Micro NA
9	GND			
10	LVDS A3 P			Micro NA
11	LVDS A3 N			Micro NA
12	GND			
13	LVDS AC P			Micro NA
14	LVDS AC N			Micro NA
15	GND			
16	LVDS DDC CLK	3.3V		

[3] CAUTION!! The supply voltage is forwarded **UNREGULATED** to all nominally 12V driven ports => Modules can operate over the entire range of 8 – 14V DC as specified; however user must take care to power peripherals (such as hard disk drives or PCI cards) within their specified voltage range.

[4] CAUTION!! The supply voltage is forwarded **UNREGULATED** to all nominally 12V driven ports => Modules can operate over the entire range of 8 – 14V DC as specified; however user must take care to power peripherals (such as hard disk drives or PCI cards) within their specified voltage range..

[5]The LVDS signals are only available for Lily Nano variant. The LVDS signals of Lily Micro are wired by default to the RGB converter. Ask Toradex for assembly options.

Pin	Description	Voltage	Active	Remarks
17	LVDS DDC DAT	3.3V		
18	GND			
19	LVDS VDD EN	3.3V		
20	LVDS BKLT EN	3.3V		
21	LVDS BKLT CTRL	3.3V		
22	GND			
23	3.3V Out	3.3V	S0	
24	3.3V Out	3.3V	S0	

3.2.10 COM Express GPIO (X29)

Pin	Description	Voltage	Active	Remarks
1	+3V3 EXP	3.3V	S5-S0	
2	GPIO4	3.3V		
3	GPIO0	3.3V		
4	GPIO5	3.3V		
5	GPIO1	3.3V		
6	GPIO6	3.3V		
7	GPIO2	3.3V		
8	GPIO7	3.3V		
9	GPIO3	3.3V		
10	GND			

3.2.11 FPGA JTAG Header (X30)

Pin	Description	Voltage	Active	Remarks
1	GND			
2	VREF (VCC AUX FPGA)	3.3V	S0	
3	GND			
4	TMS	3.3V		
5	GND			
6	TCK	3.3V		
7	GND			
8	TDO	3.3V		
9	GND			
10	TDI	3.3V		
11	GND			
12	NC			
13	GND			
14	NC			

3.2.12 External Reset and Power Button Header (X32)

Pin	Description	Voltage	Active	Remarks
1	Reset Button	3.3V		
2	GND			
3	NC			
4	NC			
5	Power Button	3.3V		
6	GND			

3.2.13 Micro Controller Debug Header (X34)

Pin	Description	Voltage	Active	Remarks
1	VREF (3.3V STDBY)	3.3V	S5-0	
2	GND			
3	GND			
4	C2D (8051 Debug Interface)	3.3V		
5	RBC2CK (8051 Debug Interface)	3.3V		
6	RBC2D (8051 Debug Interface)	3.3V		
7	C2CK (8051 Debug Interface)	3.3V		
8	NC			
9	GND			
10	NC			

3.2.14 PSoC Programming Adaptor Header (X36)

This pin header can be used for programming the embedded controller of the Woodpecker Module with a PSoC MiniProg. The programming signals are not available for Robin Modules.

Pin	Description	Voltage	Active	Remarks
1	VDD IN	5V		
2	GND			
3	NC			
4	SCLK (GPIO 1)	3.3V		
5	SDATA (GPIO 0)	3.3V		

3.2.15 Additional FFC Connector for SDIO (X39)

Pin	Description	Voltage	Active	Remarks
1	SD2 CLK	3.3V		
2	GND			
3	SD2 CMD	3.3V		
4	SD2 LED	3.3V		
5	SD2 CD#	3.3V		
6	SD2 WP	3.3V		
7	SD2 PWR#	3.3V		
8	NC			
9	SD2 DATA0	3.3V		
10	SD2 DATA1	3.3V		

Pin	Description	Voltage	Active	Remarks
11	GND			
12	SD2 DATA2	3.3V		
13	SD2 DATA3	3.3V		
14	SD2 DATA4	3.3V		
15	SD2 DATA5	3.3V		
16	GND			
17	SD2 DATA6	3.3V		
18	SD2 DATA7	3.3V		
19	NC			
20	USB CLIENT DET	3.3V		
21	SD0 LED	3.3V		
22	SD0 DATA0	3.3V		
23	SD0 DATA1	3.3V		
24	SD0 PWR#	3.3V		
25	SD0 DATA2	3.3V		
26	SD0 DATA3	3.3V		
27	SD0 WP	3.3V		
28	SD0 CMD	3.3V		
29	SD0 CD#	3.3V		
30	SD0 CLK	3.3V		

3.2.16 Switched Fan 12V Power (X40/X41)

Pin	Description	Voltage	Active	Remarks
1	NC			
2	SWITCHED POWER (FAN POWER)	12V	S0	Unregulated!
3	GND			

3.2.17 TV DAC (X42)

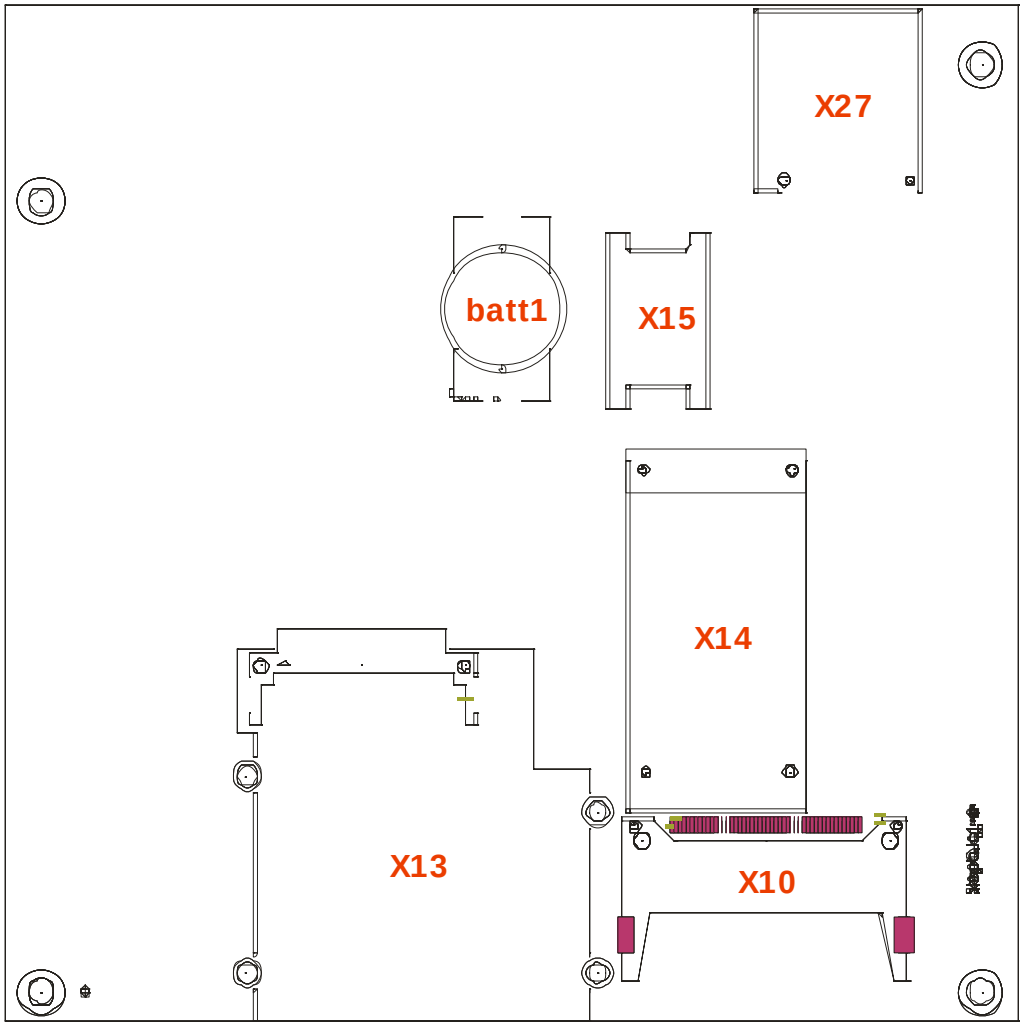
This pin header provides the TV out signals of the module connector. The standard Woodpecker does not provide these signals. The signals are only provided by the Robin module.

Pin	Description	Voltage	Active	Remarks
1	CONNECTOR EARTH			
2	CONNECTOR EARTH			
3	TV DAC C			
4	GND			
5	TV DAC B			
6	GND			
7	TV DAC A			
8	GND			
9	CONNECTOR EARTH			
10	CONNECTOR EARTH			

3.2.18 I²C Header (X43)

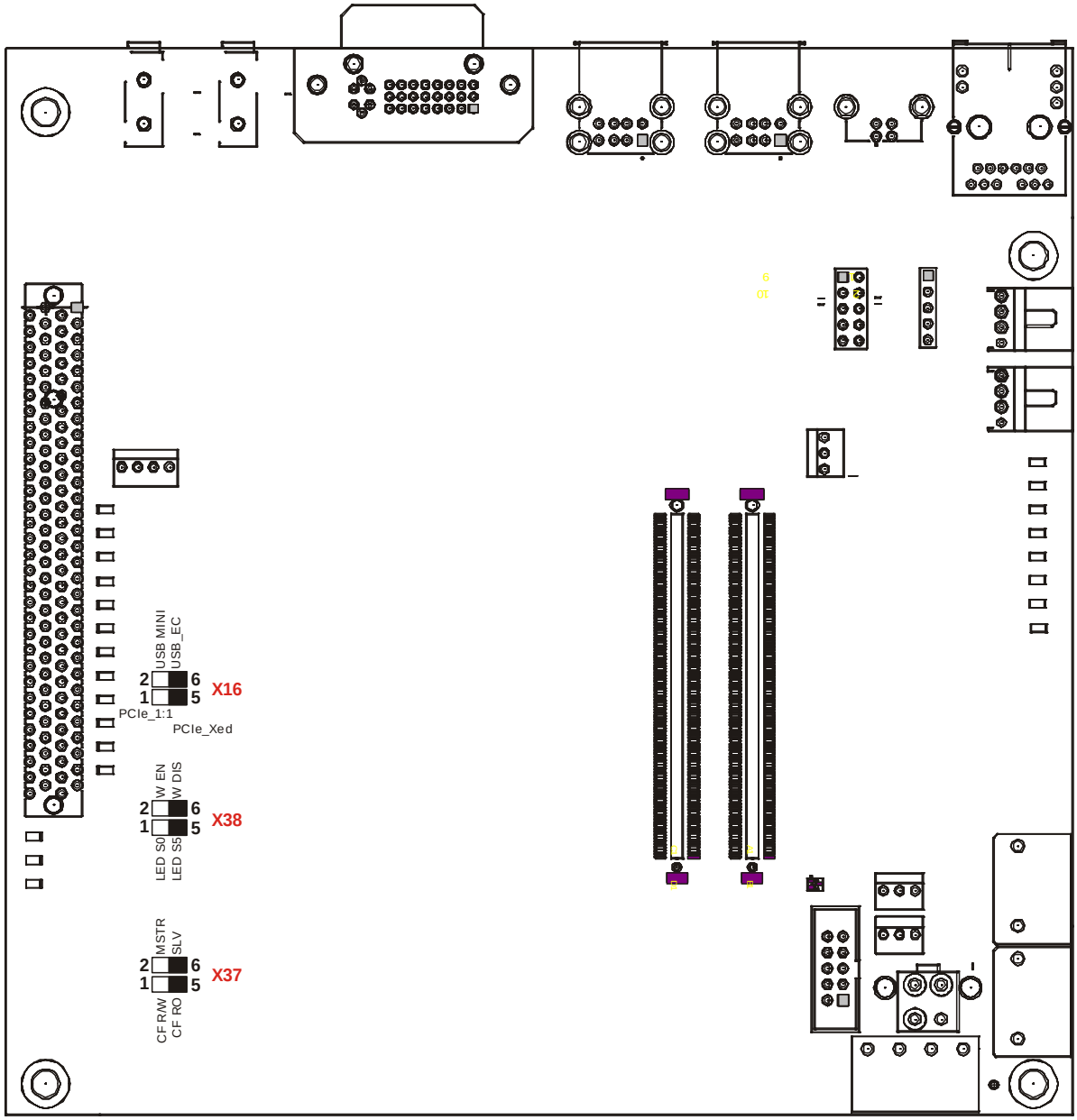
Pin	Description	Voltage	Active	Remarks
1	I²C Clock	3.3V		
2	I²C Data	3.3V		
3	GND			

3.3. Physical Drawing: Lower Side Connectors



	Description	Lily Micro	Lily Nano	Remarks
batt1	RTC Battery	X	X	Suitable Battery CR2032
X10	Compact Flash (IDE mode only)	X		Parallel to IDE Connector
X13	Express Card	X	X	USB Shared with Mini PCIe
X14	Mini PCIe	X	X	USB Shared with Express Card
X15	SIM Holder for Mini PCIe	X	X	
X27	4bit MMC / SDIO 0	X		

3.4. Jumpers



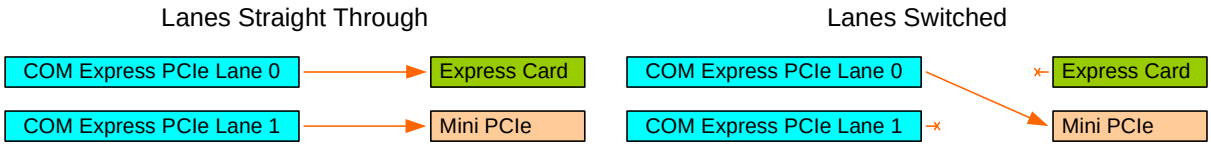
	Description	Lily Micro	Lily Nano	Remarks
X16a	PCI Express Routing	X	X	
X16b	USB 4 Routing	X	X	
X37a	Compact Flash Write Protection	X		Do not use Write Protection
X37b	Compact Flash Master/Slave	X		
X38a	LED Power Enable	X	X	
X38b	Mini PCIe Wireless Enable	X	X	

3.4.1 PCIe Routing (X16a)

Pin	Signal	Set_0	Set_1	Remarks
1	PCIE_SEL	■		
3	PCIE_SEL	■	■	
5	GND		■	

Set_0 is the default. PCIe Lanes 0 and 1 are routed straight (PCIe Lane 0 to the Express Card and PCIe Lane 1 to Mini PCIe).
Use this setting for Woodpecker Z530 and third party COM Express Modules.

Set_1 is an option for Woodpecker Z510 and Robin modules that do not have PCIe Lane 1 available. With this setting lane 0 is crossed from the Express Card to the Mini PCIe. A red LED signals this condition (LED D14).

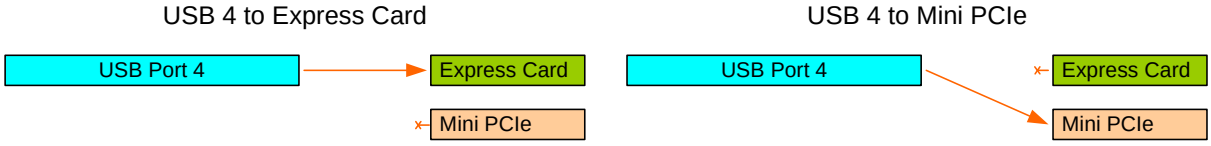


3.4.2 USB 4 Routing (X16b)

Pin	Signal	Set_0	Set_1	Remarks
2	USB_SEL	■		
4	USB_SEL	■	■	
6	GND		■	

Set_0 routes the USB 4 to the Mini PCIe. LED D12 signals this condition.

Set_1 is the default. It routes the USB 4 to the Express Card. LED D11 signals this condition.



3.4.3 Compact Flash Write Protection (X37a)

Pin	Signal	Set_0	Set_1	Remarks
1	CF_WE	■		
3	GND	■	■	
5	GND		■	

Set_0 is the default. It allows reading and writing to the Compact Flash Card.

Set_1 protects the Card against writing. Most of the Compact Flash Cards do not support the write protection in the IDE mode. Please **do not use** this option for these cards.

3.4.4 Compact Flash Master/Slave (X37b)

Pin	Signal	Set_0	Set_1	Remarks
2	CF_MASTER_SLAVE			
4	GND			
6	GND			

Set_0: The Compact Flash Card will be recognized as IDE master device. Use this option if no slave device connected at the PATA channel.

Set_1 is the default. The Compact Flash Card will be recognized as IDE slave device. Use this option if the card is used together with at IDE Master Hard Drive.

3.4.5 LED Power Enable (X38a)

Pin	Signal	Set_0	Set_1	Remarks
1	3V3_S0			
3	3V3_LED			
5	3V3_S5			

Set_0: The LEDs on the baseboard are only active in the S0 (running) state. This option saves energy in the standby mode.

Set_1 is the default. The LEDs on the Baseboard are always active.

Without a jumper, the LEDs are never active. This saves energy even in the S0 state.

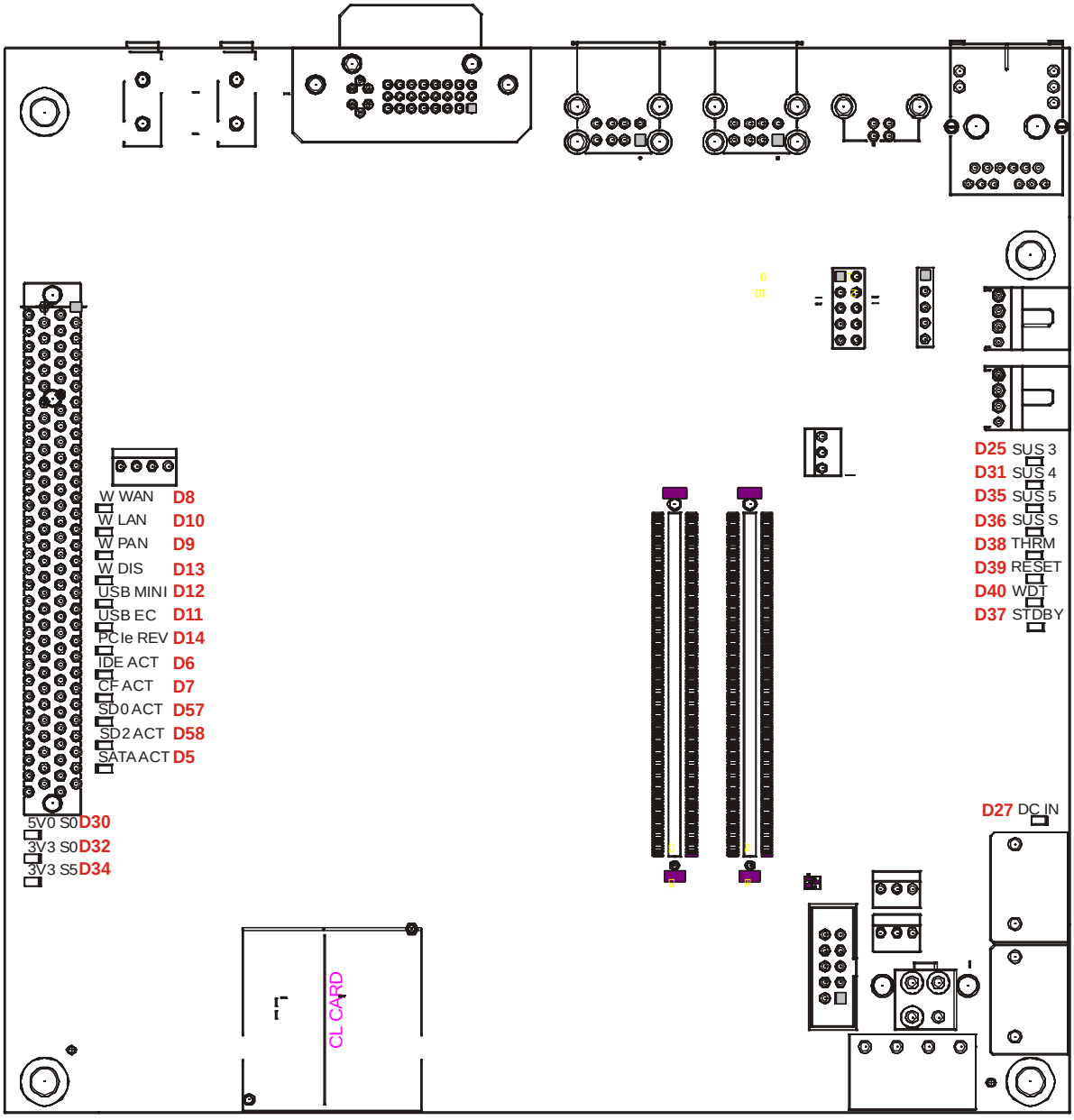
3.4.6 Mini PCIe Wireless Enable (X38b)

Pin	Signal	Set_0	Set_1	Remarks
2	W_DISABLE#			
4	W_DISABLE#			
6	GND			

Set_0 is the default. The wireless of the Mini PCIe is enabled.

Set_1 disables the wireless of the Mini PCIe. The function of this setting is depending on the used Mini PCIe Card. LED D13 indicates this option.

3.5. LEDs



	Name	Off	On	Remarks
D5	SATA ACT	SATA no traffic	SATA traffic load	
D6	IDE ACT	IDE HD no traffic	IDE HD traffic load	Only HD, not CF
D7	CF ACT	IDE Compact Flash no traffic	IDE Compact Flash traffic load	
D8	W WAN	Mini PCIe no W WAN traffic	Mini PCIe W WAN traffic load	Depending on Card
D9	W PAN	Mini PCIe no W PAN traffic	Mini PCIe W PAN traffic load	Depending on Card
D10	W LAN	Mini PCIe no W LAN traffic	Mini PCIe W LAN traffic load	Depending on Card
D11	USB EC	USB 4 routed to Mini PCIe	USB 4 routed to Express Card	
D12	USB MINI	USB 4 routed to Express Card	USB 4 routed to Mini PCIe	
D13	W DIS	Mini PCIe Wireless enabled	Mini PCIe Wireless disabled	Depending on Card
D14	PCIe REV	PCIe Lanes normal routed	PCIe 0 routed to Mini PCIe	

	Name	Off	On	Remarks
D25	SUS 3	System in S0	System in S5, S4 or S3	
D27	DC IN	No 12V Main Power	12V Main Power available	
D30	5V0 S0	5V S0 not available	5V S0 available	
D31	SUS 4	System in S3 or S0	System in S5 or S4	
D32	3V3 S0	3.3V S0 not available	3.3V S0 available	
D34	3V3 S5	3.3V S5 not available	3.3V S5 available	
D35	SUS 5	System in S4, S3 or S0	System in S5	
D36	SUS S	System normal running	Imminent Suspend Operation	
D37	STDBY	Baseboard in running mode	Baseboard in standby mode	
D38	THRM	No thermal Shutdown occurred	Thermal Shutdown occurred	
D39	RESET	System normal running	System Reset active	
D40	WDT	No Watchdog Event occurred	Watchdog Event occurred	
D57	SD0 ACT	SDIO 0 no traffic	SDIO 0 traffic load	
D58	SD2 ACT	SDIO 2 no traffic	SDIO 2 traffic load	

4. FPGA: IO Pin Mapping

4.1. Bank0 Signals

Pin	Signal	Description	I/O Voltage[6]	Direction
90	B0_0	GPIO to X18 pin 5	3.3	I/O
78	B0_1	GPIO to X18 pin 6	3.3	I/O
77	B0_2	GPIO to X18 pin 7	3.3	I/O
84	B0_3	GPIO to X18 pin 8	3.3	I/O
83	B0_4	GPIO to X18 pin 10	3.3	I/O
86	B0_5	GPIO to X18 pin 11	3.3	I/O
85	B0_6	GPIO to X18 pin 12	3.3	I/O
89	B0_7	GPIO to X18 pin 13	3.3	I/O
88	B0_8	GPIO to X18 pin 15	3.3	I/O
94	B0_9	GPIO to X18 pin 16	3.3	I/O
93	B0_10	GPIO to X18 pin 17	3.3	I/O
99	B0_11	GPIO to X18 pin 19	3.3	I/O
98	B0_12	GPIO to X18 pin 20	3.3	I/O
82	B0_13	GPIO to X18 pin 21	3.3	I/O
97	NC	Not Connected		

4.2. Bank1 Signals

Pin	Signal	Description	I/O Voltage	Direction
57	NC	Not Connected		
56	LPC_FRAME#	LPC Bus from/to Com Express Module	3.3V	I/O
60	LPC_SERIRQ	LPC Bus from/to Com Express Module	3.3V	I/O
59	LPC_CLK	LPC Bus from/to Com Express Module	3.3V	I/O
62	LPC_AD0	LPC Bus from/to Com Express Module	3.3V	I/O
61	LPC_AD1	LPC Bus from/to Com Express Module	3.3V	I/O
65	LPC_AD2	LPC Bus from/to Com Express Module	3.3V	I/O
64	LPC_AD3	LPC Bus from/to Com Express Module	3.3V	I/O
71	LPC_DRQ0#	LPC Bus from/to Com Express Module	3.3V	I/O
70	LPC_DRQ1#	LPC Bus from/to Com Express Module	3.3V	I/O
73	NC	Not Connected		
72	NC	Not Connected		
68	NC	Not Connected		

[6] In standard assembly option, the I/O Voltage of the bank 0 signals is 3.3V. This voltage can be changed by disassembly a 0R and provide the I/O Voltage at the pin header. Please contact Toradex for more details.

4.3. Bank2 Signals

Pin	Signal	Description	I/O Voltage	Direction
46	MOSI	DATA to FLASH dedicated to configuration	3.3V	O
25	M0	Mode select dedicated to configuration	3.3V	N/A
23	M1	Mode select dedicated to configuration	3.3V	N/A
27	CSO_B	CS to FLASH dedicated to configuration	3.3V	O
24	M2	Mode select dedicated to configuration	3.3V	N/A
30	VS1	Flash select dedicated to configuration	3.3V	N/A
28	NC	Not Connected		
31	VS0	Flash select dedicated to configuration	3.3V	N/A
29	VS2	Flash select dedicated to configuration	3.3V	N/A
34	HK_KBD_A20_GATE	Legacy Signal	3.3V	I
32	W_DISABLE_CONTROL	Overrides the Jumper X38b setting	3.3V	O
35	NC	Not Connected		
33	DBG_RX	Serial Debug Port to Micro Controller P0.5	3.3V	O
37	DBG_TX	Serial Debug Port to Micro Controller P0.4	3.3V	I
36	HK_KBD_RST#	Legacy Signal	3.3V	I
41	HK_BIOS_DISABLE#	Leave OPEN for normal operation	3.3V	OC
40	HK_ RESET#	System Reset Signal	3.3V	I
44	HK_SMB_DAT	SMBus Data Line	3.3V	I / OC
43	HK_SMB_CLK	SMBus Clock Line	3.3V	I
49	HK_SUS_STAT	Status Signal from CPU	3.3V	I
48	INIT_B	Dedicated to configuration	3.3V	N/A
51	D_IN	Data from FLASH dedicated to configuration	3.3V	I
50	HK_I2C_DAT	I^2C Data Line	3.3V	I / OC
53	CCLK	Clock to FLASH dedicated to configuration	3.3V	O
52	HK_I2C_CLK	I^2C Clock Line	3.3V	I
39	NC	Not Connected		

4.4. Bank3 Signals

Pin	Signal	Description	I/O Voltage[7]	Direction
4	B3_0	GPIO to X17 pin 5	3.3	I/O
3	B3_1	GPIO to X17 pin 6	3.3	I/O
6	B3_2	GPIO to X17 pin 7	3.3	I/O
5	B3_3	GPIO to X17 pin 8	3.3	I/O
10	B3_4	GPIO to X17 pin 10	3.3	I/O
9	B3_5	GPIO to X17 pin 11	3.3	I/O
13	B3_6	GPIO to X17 pin 12	3.3	I/O
12	B3_7	GPIO to X17 pin 13	3.3	I/O
16	B3_8	GPIO to X17 pin 15	3.3	I/O
15	B3_9	GPIO to X17 pin 16	3.3	I/O
20	B3_10	GPIO to X17 pin 17	3.3	I/O
19	B3_11	GPIO to X17 pin 19	3.3	I/O
21	B3_12	GPIO to X17 pin 20	3.3	I/O
7	B3_13	GPIO to X17 pin 21	3.3	I/O

[7] In standard assembly option, the I/O Voltage of the bank 3 signals is 3.3V. This voltage can be changed by disassembly a 0R and provide the I/O Voltage at the pin header. Please contact Toradex for more details.