Colibri XScale® PXA270

Datasheet

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Revision history

Date	Doc. Rev.	Colibri PXA270 HW-Version	Changes
03-Feb-05	Rev. 0.7	V1.0	Initial Release
14-Jul-05	Rev. 1.0	V1.0	Corrected SODIMM pin 28, 30, 95, 99 Added JTAG / Additional GPIO connectors Added Compatibility to Trizeps III/IV Added list of SODIMM200 socket manufacturer Added RoHS compliance
22-Feb-06	Rev. 1.1	V1.0	Various erratums concerning signal names Added additional OS supported by third party
26-Jun-06	Rev. 1.2	V1.0 / V1.2	Administrative changes
13-Sep-06	Rev. 1.3	V1.0 / V1.2	Improved picture quality
24-Dec-06	Rev. 1.4	V1.0 / V1.2	Colibri mechanical drawing updated, pins renamed (MA to ADDRESS, MD to DATA)
24-Sep-09	Rev. 1.5	V1.0/V1.2	nRESET_IN description changed. Added description for pin (+3.3 /VCC_BATT) in chapter 3.20 Added notes 5 to 7 for SODIMM pins Added typical current consumption and threshold values for Reset, VDD_FAULT in chapter 6.1 Corrected chapter 4.2 JTAG connector RESET_In to input Added Tolerance value for PCB outline Do not use RDY pin (SODIMM 95) Added some typical current consumption values
25-May-10	Rev. 2.0	V1.2/V2.1	Added PXA270 V2.1 description: - New Processor: PXA270M (for testing only) - New Codec: WM9715L instead of UCB1400 Added description for VDDA_AUDIO and VSSA_AUDIO
04-Jun-10	Rev. 2.1	V1.2/V2.1	Added analog input voltage range description (chap. 3.18)
10-Jun-10	Rev. 2.2	V1.2/V2.1	Added some clarifications to chap. 3.18
6-Sep-10	Rev. 2.3	V1.2/V2.2	Added HW V2.2
23-Nov-11	Rev. 2.4	V1.2/V2.2	Changed Disclaimer
25-May-12	Rev. 2.5	V1.2/V2.2 upwards	Add PXA270M references.

Contents

1. Introduction

1.1 Hardware

Colibri XScale® PXA270 is a SODIMM sized computer module based on the Marvell XScale® PXA270/PXA270M processor. It runs at up to 520 MHz and consumes as little as 800mW. The module delivers state of the art technology, targeting low power systems that still require high CPU performance.

It also offers all the interfaces needed in a modern embedded device: beside the internal Flash memory, there are plenty of interfaces available for data storage: Memory Stick, CompactFlash/ PCMCIA and SDCard. The module provides glueless connectivity to passive and active LCDs with resolutions of up to 1024x768, as well as 4-wire resistive touch screens. An integrated 16 bit stereo codec allows Colibri PXA270 to play and record sound. Colibri PXA270 can directly connect to a CMOS/CCD camera sensor or take advantage of the new Intel Mobile Scalable Link that offers transfer speeds of up to 416 Mbps.
In addition Colibri PXA270 offers a 100 MBit Ethernet as well as USB host and USB device functionality.

The entire 32 bit wide CPU bus is available for custom extensions, such as special interfaces for high bandwidth applications.

1.2 Software

Various operating systems are available for the Colibri PXA270 module:

1.2.1 Windows CE

At the time of writing this document, Colibri PXA270 modules are shipped with a valid Windows CE 5.0 core license. Toradex provides an image that contains drivers for the most common interfaces and is easily customizable by registry settings to adapt to specific hardware. Windows Embedded CE 6.0 is also available for download on the Toradex download website. Since the Colibri modules are shipped with a Windows Embedded CE 6.0 license it is allowed to switch to CE 6 without acquiring a new license.

1.2.2 Other Operating Systems

Other operating systems for the Colibri PXA270 modules which are available from third parties:
- Embedded Linux (Kernels 2.4 and 2.6)
- QNX

1.3 Features Summary

CPU:
PXA270 312 / 520 MHz

Memory:
64 MByte of SDRAM (32 Bit)
32 MByte of FLASH (32 Bit)

Interfaces:
32 Bit processor bus
CompactFlash / PCMCIA
LCD (SVGA)
Touch screen
Audio I/O (16 Bit stereo)
CMOS/CCD image sensor interface
MSL (up to 416 Mbps)
I2C
SPI
SDCard
Memory Stick
85 GPIOs
USB host / device
100 MBit Ethernet

Supported operating systems:
WinCE
Embedded Linux Kernel 2.4 and 2.6 (supported by third party)
QNX (supported by third party)

1.4 Reference Documents

For detailed technical information about the Colibri PXA270 components, please refer to the documents listed below.

1.4.1 Marvell PXA270/PXA270M Processor Based on Intel Xscale Technology

Intel/Marvell PXA270/PXA270M
The datasheets and other technical documents about the PXA270 processor are available on the Marvell web page:
http://www.marvell.com

1.4.2 Ethernet Controller

Davicom DM9000 Datasheet:
http://www.davicom.com.tw

1.4.3 Audio Codec and Touch Screen Controller

Up to module HW V1.2: NXP UCB1400:
http://www.nxp.com

Module HW V2.1 and higher: Wolfson WM9715L:
http://www.wolfsonmicro.com

1.4.4 Power Management IC

Texas Instrument TPS65020 / TPS65021:
http://www.ti.com

2. Functional Description

2.1 Block Diagram

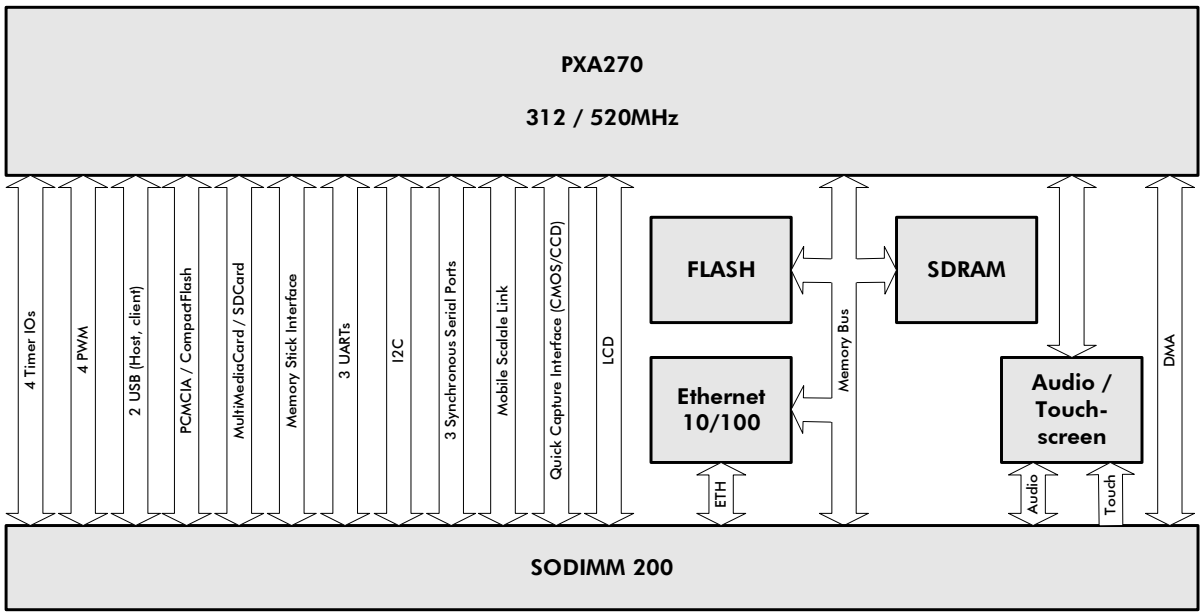

Figure 1: Colibri PXA270 block diagram

Figure 1 shows the Colibri PXA270 interfaces. However, some PXA270 pins are mapped to multiple interfaces. Therefore not all functions can be used simultaneously (for example there are only three of the four UARTs available in parallel on the SODIMM200 connector).

Colibri PXA270 features full 32 bit interfaces to on board FLASH, SDRAM and the Ethernet controller. This results in maximum bandwidth for any data transfers.

Wireless Intel Speedstep® Technology, which adjusts the CPU core voltage dynamically according to the CPU load, and four low-power modes both enable excellent MIPS/mW performance for the Colibri PXA270 module.

3. Signal Description

This chapter describes the signals grouped by their function. Some of the Colibri PXA270 pins have dedicated functionality, but most are highly multiplexed, so that the same pin can have up to 6 different roles and the same functionality is sometimes available alternatively on different pins. Each of these multiplexed pins is additionally also usable as a General Purpose Input/Output pin (GPIO).

IO Types notation:

I:	Digital CMOS input
O:	Digital CMOS output
IO:	Digital CMOS input / output
AIN:	Analog input
AOUT:	Analog output
AINOUT:	Analog input / output
PWR:	Power supply

3.1 Memory Bus

Pin Name	Description	IO type	Multiplexed
DATA[[31:0]	Memory Data Bus: data bus to and from external memory devices.	IO	Dedicated Pins
ADDRESS[[25:0]	Memory Address Bus: Drives the requested address for external memory accesses.	O	Dedicated Pins
nOE	Memory Output Enable: Connect to the output enables of static memory devices to control data bus drivers.	O	Dedicated Pin
nWE	Memory Write Enable: Connect to the write enables of SDRAM and static memory devices.	O	Dedicated Pin
DQM[3:0]	DQM Data Byte Mask Control (Bytes 3 through 0): Connect to the data output mask enables (DQM). DQM0 corresponds to DATA[<7:0>, DQM1 corresponds to DATA[<15:8>, and so forth.	O	Dedicated Pin
RDnWR	Read/Write: Indicates that the current transaction is a read (high) or a write (low)	O	Dedicated Pin
nCS1 nCS3 nCS4	Static Chip Selects: Chip selects to static memory devices such as ROM and flash, individually programmable in the memory configuration registers. nCS<5:0> can be used with variable-latency I/O devices. nCS<3:0> can be used with synchronous flash.	O	GPIO15 GPIO79 GPIO80
RDY	Variable Latency I/O Ready Pin: An external variable-latency I/O (VLIO) device asserts RDY when it is ready to transfer data. This signal is pulled-up with a 4k7 resistor. Up to HW V1.2: Do not connect this pin because it's driven internally (push/pull).	I	GPIO18

3.2 PCMCIA / CF

Pin Name	Description	IO Type	Multiplexed
nPOE	PC Card Output Enable: Output enable for reads from PC Card memory and PC Card attribute space.	O	GPIO48
nPWE	PC Card Write Enable: Enables writes to PC Card memory and PC Card attribute space. Also serves as the write enable signal for variable-latency I/O.	O	GPIO49
nPIOW	PC Card I/O Write: Asserted for writes to PC Card I/O space.	O	GPIO51
nPIOR	PC Card I/O Read: Asserted for reads from PC Card I/O space.	O	GPIO50

Pin Name	Description	IO Type	Multiplexed
nPCE1 nPCE2	PC Card Enable 1 and 2: Selects a PC Card. nPCE<2> enables the high byte lane, and nPCE<1> enables the low byte lane.	O	GPIO15 / 85 / 86 GPIO54 / 87
nIOIS16	I/O Select 16: Input from the PC Card indicating that the data bus: 0 = Data bus is 8 bits wide 1 = Data bus is 16 bits wide	I	GPIO57
nPWAIT	PC Card Wait: Driven low by the PC Card to insert wait states, which extend transfers to and from the PXA270 processor.	I	GPIO56
PSKTSEL	PC Card Socket Select: Used by external steering logic to route control, address, and data signals to one of the two PC Card sockets. Active-low output enable that can be used as nOE for the data transceivers. The signal has the same timing as the address bus. In a single socket solution: 0 = Output enable selected 1 = Output enable not selected In a dual socket solution, the socket select: 0 = Socket 0 selected 1 = Socket 1 selected	O	GPIO79 / 104
nPREG	PC Card Register Select: Functions as address bit 26 to select register space (I/O or attribute) or memory space. Has the same timing as the address bus.	O	GPIO55

3.3 LCD Controller

Pin Name	Description	IO Type	Multiplexed
LDD[17:0]	LCD Display Data: Transfers pixel information from the LCD controller to the external LCD panel. These pins become inputs driven by the panel during a read from a panel with an integrated frame buffer.	IO	GPIO[87:86] GPIO[73:58]
L_CS	LCD Chip Select: Chip select signal for LCD panels with an internal frame buffer.	O	GPIO19
L_FCLK_RD	LCD Frame Clock: Frame clock used by the LCD display module to signal the start of a new frame of pixels that resets the line pointers to the top of the screen. This pin is also the vertical synchronization signal for active (TFT) displays. This pin is the read signal during reads from a panel with an internal frame buffers.	O	GPIO74
L_LCLK_A0	LCD Line Clock: Indicates the start of a new line. Also referred to as HSync (or horizontal synchronization) for active panels. For LCDs with an internal frame buffer, this signal indicates a command or data transaction.	O	GPIO75
L_PCLK_WR	LCD Pixel Clock: Pixel clock used by the LCD display module to clock the pixel data into the line shift register. In passive mode, the pixel clock toggles only when valid data is available on the data pins. In active mode, the pixel clock toggles continuously, and the AC bias pin is used as an output to signal when data is valid on the LCD data pins. This pin also functions as a write signal for LCD panels with an internal frame buffer.	O	GPIO76
L_VSYNC	LCD Refresh Sync: Sync input driven by LCDs with an internal frame buffer	I	GPIO14
L_BIAS	LCD Bias Drive: AC bias that signals the LCD display module to switch the polarity of the power supplies to the row and column axis of the screen to counteract DC offset. In active (TFT) mode, it is used as the output enable to signal when data should be latched from the data pins using the pixel clock.	O	GPIO77

3.4 UARTS

3.4.1 Full-Function UART

Pin Name	Description	IO Type	Multiplexed
FF_RXD	Full-Function UART Receive Data	I	GPIO19 / 33 / 34 / 41 / 53 / 85
FF_TXD	Full-Function UART Transmit Data	O	GPIO16 / 37 / 39 83 / 99
FF_CTS	Full-Function UART Clear-to-Send	I	GPIO26 / 35 / 100
FF_DCD	Full-Function UART Data-Carrier-Detect	I	GPIO10 / 36
FF_DSR	Full-Function UART Data-Set-Ready	I	GPIO33 / 37
FF_RI	Full-Function UART Ring Indicator	I	GPIO38 / 89
FF_DTR	Full-Function UART Data-Terminal-Ready	O	GPIO40 / 82
FF_RTS	Full-Function UART Request-to-Send	O	GPIO27 / 41 / 83

3.4.2 Bluetooth UART

Pin Name	Description	IO Type	Multiplexed
BT_RXD	Bluetooth UART Receive Data	I	GPIO42
BT_TXD	Bluetooth UART Transmit Data	O	GPIO43
BT_CTS	Bluetooth UART Clear-to-Send	I	GPIO44
BT_RTS	Bluetooth UART Request-to-Send	O	GPIO45

3.4.3 Standard UART

Pin Name	Description	IO Type	Multiplexed
STD_RXD	Receive Pin for Standard UART and Slow Infrared Functions	I	GPIO46
STD_TXD	Transmit Pin for Standard UART and Slow Infrared Functions	O	GPIO47

3.4.4 IRDA UART (Infrared Communication Port)

Pin Name	Description	IO Type	Multiplexed
ICP_RXD	IrDA Receive Data: Receive data pin for the fast infrared port function	I	GPIO42 / 46
ICP_TXD	IrDA Transmit Data: Transmit data pin for the fast infrared port function	O	GPIO43 / 47

3.4.5 MultiMediaCard (MMC) / SecureDigitalCard (SD)

Pin Name	Description	IO Type	Multiplexed
MMCLK	MultiMediaCard and SD/SDIO Card Bus Clock	O	GPIO32
MMCMD	MultiMediaCard Command: MMC and SD/SDIO: Bidirectional line for command and response tokens. SPI: Output for command and write data.	IO	GPIO112
MMDAT0	MultiMediaCard Data 0: MMC and SD/SDIO: Bidirectional line for read and write data. SPI: Input for response token and read data.	IO	GPIO92
MMDAT1	MultiMediaCard Data 1: SD/SDIO: Bidirectional line for read and write data. Used only for SD 4-bit data transfers and to signal SDIO interrupts to the controller. SPI: Used only to signal SDIO interrupts to the controller.	IO	GPIO109

Pin Name	Description	IO Type	Multiplexed
MMDAT2/ MMCS0	MMC Chip Select 0: SD/SDIO: Bidirectional line for read and write data. Used only for SD 4-bit data transfers. SPI: Chip select 0	IO	GPIO110
MMDAT3/ MMCS1	MMC Chip Select 1: SD/SDIO: Bidirectional line for read and write data. Used only for SD 4-bit data transfers. SPI: Chip select 1	IO	GPIO111

3.5 Synchronous Serial Port (SSP)

Pin Name	Description	IO Type	Multiplexed
SSPSCLK	Synchronous Serial Port 1 Clock: The serial bit-clock can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO23
SSPSFRM	Synchronous Serial Port 1 Frame: The serial frame sync can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO24
SSPTXD	Synchronous Serial Port 1 Transmit Data: Serial data driven out synchronously with the bit-clock.	O	GPIO25 / 57
SSPRXD	Synchronous Serial Port 1 Receive Data: Serial data latched using the bit-clock.	I	GPIO26
SSPEXTCLK/ SSPSCLKEN	Synchronous Serial Port 1 External Clock: This input supplies an external bit-clock or an external enable request for the internally generated bit-clock.	I	GPIO27
SSPSYSCLK	Synchronous Serial Port 1 System Clock: When enabled, provides a reference clock at four times the port 1 bit-clock.	O	GPIO53 / 27
SSPSCLK2	Synchronous Serial Port 2 Clock: The serial bit-clock can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO50 / 19 / 36
SSPSFRM2	Synchronous Serial Port 2 Frame: The serial frame sync can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO14 / 87 / 37 / 88
SSPTXD2	Synchronous Serial Port 2 Transmit Data: Serial data driven out synchronously with the bit-clock.	O	GPIO87 / 38 / 89
SSPRXD2	Synchronous Serial Port 2 Receive Data: Serial data latched using the bit-clock.	I	GPIO86 / 11 / 40 / 88
SSPSCLK3	Synchronous Serial Port 3 Clock: The serial bit-clock can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO52 / 84 / 34 / 40
SSPSFRM3	Synchronous Serial Port 3 Frame: The serial frame sync can be configured as an output (master-mode operation) or an input (slave-mode operation).	IO	GPIO83 / 35 / 39
SSPTXD3	Synchronous Serial Port 3 Transmit Data: Serial data driven out synchronously with the bit-clock.	O	GPIO81 / 35 / 38
SSPRXD3	Synchronous Serial Port 3 Receive Data: Serial data latched using the bit-clock.	I	GPIO82 / 89 / 41
SSPSYSCLK3	Synchronous Serial Port 3 System Clock: When enabled, provides a reference clock at four times the port 3 bit-clock.	O	GPIO45

3.6 USB

Pin Name	Description	IO Type	Multiplexed
USBH_P	USB Host Positive Line: Differential signal connects to the USB host interface.	IO	Dedicated Pin
USBH_N	USB Host Negative Line: Differential signal connects to the USB host interface.	IO	Dedicated Pin
USBHPWR1	USB Host Power Indicator: Over-current indicator from USB power IC for USB host port.	I	GPIO88
USBHPEN1	USB Host Power Enable: Controls power IC for USB host port.	O	GPIO89
USBC_P	USB Client Positive Line: Differential signal connects to the USB client interface.	IO	Dedicated Pin
USBC_N	USB Client Negative Line: Differential signal connects to the USB client interface.	IO	Dedicated Pin
USBC_ID	USB OTG configuration pin: Input signals client or host	I	GPIO41

3.7 Quick Capture Interface

Pin Name	Description	IO Type	Multiplexed
CIF_MCLK	Quick Capture Interface Master Clock: Programmable output clock used by the camera capture sensor.	O	GPIO23 / 42 / 53
CIF_PCLK	Quick Capture Interface Pixel Clock: Pixel clock used by the quick capture interface of the camera to clock the pixel data into the input FIFO	I	GPIO26 / 45 / 54
CIF_DD0 CIF_DD1 CIF_DD2 CIF_DD3 CIF_DD4 CIF_DD5 CIF_DD6 CIF_DD7 CIF_DD8 CIF_DD9	Quick Capture Interface Data: Data lines to transmit 4,5,6,7,8,9 or 10 bits at a time.	I	GPIO27 / 47 / 81 GPIO55 GPIO51 / 104 GPIO50 GPIO52 / 83 GPIO48 / 82 GPIO17 GPIO12 GPIO107 GPIO106
CIF_FV	Quick Capture Interface Frame Synchronization: Frame start or alternate synchronization signal used by the sensor to signal frame read-out or as an external vertical synchronization.	IO	GPIO24 / 43 / 84
CIF_LV	Quick Capture Interface Line Synchronization: Line start or alternate synchronization signal used by the sensor to signal line read-out or as an external horizontal synchronization	IO	GPIO25 / 44 / 85

3.8 Memory Stick Host Controller

Pin Name	Description	IO Type	Multiplexed
MSBS	Memory Stick Bus State: Serial protocol bus-state signal.	O	GPIO92
MSSDIO	Memory Stick Data: Serial protocol data signal.	IO	GPIO109
nMSINS	Memory Stick Insert Signal: Detects memory stick insertion and extraction.	I	GPIO112
MSSCLK	Memory Stick Serial Clock: Serial protocol clock signal.	O	GPIO32

3.9 Mobile Scalable Link

Pin Name	Description	IO Type	Multiplexed
BB_OB_DAT0 BB_OB_DAT1 BB_OB_DAT2 BB_OB_DAT3	MSL Outbound Data: This bus carries up to four bits of parallel data to be transmitted to the baseband processor.	O	GPIO81 GPIO48 GPIO50 GPIO51
BB_OB_CLK	MSL Outbound Clock: This clock provides timing for outbound transmissions to the baseband processor.	O	GPIO52
BB_OB_STB	MSL Outbound Strobe: This signal qualifier indicates that a channel identifier is on the data pins when it is asserted, and that a data nibble is on the data pins when it is deasserted.	O	GPIO53
BB_OB_WAIT	MSL Outbound Wait: This input provides flow control for the outbound link from the baseband processor.	I	GPIO54
BB_IB_DAT0 BB_IB_DAT1 BB_IB_DAT2 BB_IB_DAT3	MSL Inbound Data: This bus carries up to four-bits of parallel data received from the baseband processor.	I	GPIO82 GPIO55 GPIO56 GPIO57
BB_IB_CLK	MSL Inbound Clock: This clock provides timing for inbound transmissions from the baseband processor.	I	GPIO83
BB_IB_STB	MSL Inbound Strobe: This signal qualifier indicates that a channel identifier is on the data pins when it is asserted, and that a data nibble is on the data pins when it is deasserted.	I	GPIO84
BB_IB_WAIT	MSL Inbound Wait: This output provides flow-control for the inbound link back to the baseband processor.	O	GPIO85

3.10 I2C

Pin Name	Description	IO Type	Multiplexed
I2C_CLK	I2C Clock: Serial clock.	IO	GPIO117
I2C_DATA	I2C Data: Serial data/address bus.	IO	GPIO118

3.11 PWM

Pin Name	Description	IO Type	Multiplexed
PWM_OUT0	Pulse Width Modulation Channel 0	O	GPIO16
PWM_OUT1	Pulse Width Modulation Channel 1	O	GPIO17 / 38
PWM_OUT2	Pulse Width Modulation Channel 2	O	GPIO11 / 46 / 79
PWM_OUT3	Pulse Width Modulation Channel 3	O	GPIO12 / 47 / 80

3.12 DMA

Pin Name	Description	IO Type	Multiplexed
DREQ1	DMA Request 1: DMA request from an external companion chip.	I	GPIO80
DREQ2	DMA Request 2: DMA request from an external companion chip.	I	GPIO85 / 100

3.13 Clocks

Pin Name	Description	IO Type	Multiplexed
HZ_CLK	Real-Time 1 Hz Clock: Real-time 1-Hz clock (after RTC trim adjustment).	O	GPIO10
CLK_TOUT	Timekeeping Clock Output: CLK_TOUT signal is an output that drives a buffered version of the TXTAL_IN oscillator input when the TOUT_EN bit of the OSCC register is set. When enabled, this clock is output in sleep mode, but it is always disabled in deep-sleep mode.	O	GPIO10
48_MHz	48-MHz Output Clock: Generates peripheral timing from 312-MHz peripheral clock.	O	GPIO11 / 12

3.14 Timers

Pin Name	Description	IO Type	Multiplexed
EXT_SYNC0	External Sync 0: This input provides a reset for any timer channels enabled to use it.	I	GPIO11
EXT_SYNC1	External Sync 1: This input provides a reset for any timer channels enabled to use it.	I	GPIO12
CHOUT0	Timer Channel Output 0: Periodic clock output from timer channel 10.	O	GPIO11
CHOUT1	Timer Channel Output 1: Periodic clock output from timer channel 10.	O	GPIO12 / 10

3.15 Misc

Pin Name	Description	IO Type	Multiplexed
nBATT_FAULT (BATT_SENSE) [8]	Main Battery Fault: This input signals that the main battery is low or removed. Assertion causes the PXA270 processor to enter sleep mode or, if PMCR[BIDAE] is set, forces an imprecise-data abort, which cannot be masked. The PXA270 processor does not recognize a wake-up event while this signal is asserted.	I	Dedicated Pin
nVDD_FAULT (VDD_SENSE) [7]	VDD Fault: This input signals that the main power source is going out of regulation. nVDD_FAULT causes the PXA270 processor to enter sleep mode or, if PMCR[VIDAE] is set, forces an imprecise-data abort, which cannot be masked. nVDD_FAULT is ignored after a wake-up event until the power supply timer completes (approximately 10 ms).	I	Dedicated Pin
nRESET_IN [9]	Reset: This active-low, level-sensitive input starts the processor from the reset vector at address 0. Assertion causes the current instruction to terminate abnormally and causes a reset. When nRESET is driven high, the processor starts execution from address 0. nRESET must remain low until the power supply is stable. PXA270 V1.2 and higher: The nRESET_IN has a deglitch feature. That means, you have to pull the reset low for at least 35ms.	I	Dedicated Pin
nRESET_OUT	Reset Out: Asserted when nRESET is asserted, it deasserts after nRESET is deasserted but before the first instruction fetch occurs. nRESET_OUT is asserted during power-on, hardware, watchdog, and sleep-exit resets. It is configurable for GPIO reset.	O	Dedicated Pin

3.16 JTAG

Pin Name	Description	IO Type	Multiplexed
nTRST	JTAG Test Reset: IEEE 1194.1 test reset.	I	Dedicated Pin
TDI	JTAG Test Data Input: Data from the JTAG controller is sent to the PXA270 processor using this signal. This pin has an internal pull-up resistor.	I	Dedicated Pin
TDO	JTAG Test Data Output: Data from the PXA270 processor is returned to the JTAG controller using this signal.	O	Dedicated Pin
TMS	JTAG Test Mode Select: Selects the test mode required from the JTAG controller. This pin has an internal pull-up resistor.	I	Dedicated Pin
TCK	JTAG Test Clock: For all transfers on the JTAG test interface.	I	Dedicated Pin

3.17 Audio

Pin Name	Description	IO Type	Multiplexed
MIC_IN	Microphone Input	AIN	Dedicated Pin
MIC_GND	Microphone Ground	PWR	Dedicated Pin
LINEIN_L	Line Input (Left Channel)	AIN	Dedicated Pin
LINEIN_R	Line Input (Right Channel)	AIN	Dedicated Pin
HEADPHONE_GND	Headphone Ground	PWR	Dedicated Pin
HEADPHONE_L	Headphone Output (Left Channel)	AOUT	Dedicated Pin
HEAPHONE_R	Headphone Output (Right Channel)	AOUT	Dedicated Pin

3.18 Touch / ADC

Pin Name	Description	IO Type	Multiplexed
AD[3:0]	AD Converter Inputs Input Voltage Range is different depending on module version: Colibri PXA270 up to V1.2 - AD[3:0]: 0V to 7.5V Colibri PXA270 V2.1 and higher: - AD[3, 1, 0]: 0V to 3.3V - AD[2]: 0V to 5V We recommend using 3.3V as maximum voltage on all AD inputs to ensure the compatibility to future Colibri modules.	AIN	Dedicated Pin
TSPX	4wire Resistive Touch Panel (X Plus Terminal)	AINOUT	Dedicated Pin
TSMX	4wire Resistive Touch Panel (X Minus Terminal)	AINOUT	Dedicated Pin
TSPY	4wire Resistive Touch Panel (Y Plus Terminal)	AINOUT	Dedicated Pin
TSMY	4wire Resistive Touch Panel (Y Minus Terminal)	AINOUT	Dedicated Pin

3.19 Ethernet

Pin Name	Description	IO Type	Multiplexed
nETH_LINK_AKT	Ethernet Activity Indicator	O	Dedicated Pin
nETH_SPEED100	Ethernet Speed Indicator	O	Dedicated Pin
ETH_TXO-	Ethernet TX Differential Output (minus)	O	Dedicated Pin
ETH_TXO+	Ethernet TX Differential Output (plus)	O	Dedicated Pin
ETH_RXI-	Ethernet RX Differential Input (minus)	I	Dedicated Pin
ETH_RXI+	Ethernet RX Differential Input (plus)	I	Dedicated Pin

3.20 Power

Pin Name	Description	IO Type	Multiplexed
+3V3 (VCC_BATT)	Backup power supply. In case there is no backup battery present connect this supply to +3V3. This supply is needed for booting.	PWR	Dedicated Pin
+3V3	Main power supply, connect to 3.3V	PWR	Dedicated Pin
VDDA_AUDIO	Power supply for the audio and touch-screen controller. Also connect this pins if audio and touch are unused. You can connect this to main 3.3V or to a filtered 3.3V depending on your application.	PWR	Dedicated Pin
GND	System ground	PWR	Dedicated Pin
VSSA_AUDIO	Audio and touch-screen controller ground. Connect to GND or filtered GND.	PWR	Dedicated Pin

4. Colibri PXA270 Connectors

4.1 Physical Locations

Along with the main 200Pin SODIMM connector the Colibri PXA270 is equipped with two additional FCC connectors. The position of the connectors is shown in the figure below.

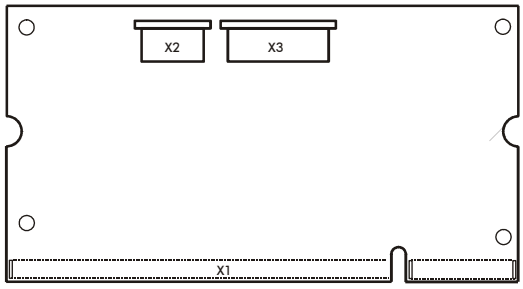

Figure 2: Location of Colibri PXA270's Connectors

4.2 SODIMM 200 (X1)

The signals after the slash ("/") are Toradex standard functions.

Pin#	Top side (Toradex logo)	Note
1	MIC_IN	2
3	MIC_GND	2
5	LINEIN_L	2
7	LINEIN_R	2
9	VSSA_AUDIO	5
11	VSSA_AUDIO	5
13	HEADPHONE_GND	
15	HEADPHONE_L	2
17	HEAPHONE_R	2
19	GPIO46 / STD_RXD	1
21	GPIO47 / STD_TXD	1
23	GPIO40 / FF_DTR	1
25	GPIO100 / FF_CTS	1
27	GPIO27 / FF_RTS	1
29	GPIO33 / FF_DSR	1
31	GPIO10 / FF_DCD	1
33	GPIO34 / FF_RXD	1
35	GPIO39 / FF_TXD	1
37	GPIO38 / FF_RI	1
39	GND	
41	GND	
43	GPIO0	1
45	GPIO1 / PRDY	1
47	GPIO32 / MMCLK	1

Pin#	Bottom side	Note
2	AD3	2
4	AD2	2
6	AD1	2
8	AD0	2
10	VDDA_AUDIO	5
12	VDDA_AUDIO	5
14	TSPX	2
16	TSMX	2
18	TSPY	2
20	TSMY	2
22	nVDD_FAULT (VDD_SENSE)	7
24	nBATT_FAULT (BATT_SENSE)	8
26	nRESET_IN	9
28	GPIO11	1
30	GPIO16	1
32	GPIO44 / BT_CTS	1
34	GPIO45 / BT_RTS	1
36	GPIO42 / BT_RXD	1
38	GPIO43 / BT_TXD	1
40	+3V3 (VCC_BATT)	6
42	+3V3	
44	GPIO77 / L_BIAS	1
46	GPIO65 / LDD07	1
48	GPIO67 / LDD09	1

Pin#	Top side (Toradex logo)	Note
49	GPIO109 / MMDAT1	1
51	GPIO110 / MMDAT2/MMCS0	1
53	GPIO111 / MMDAT3/MMCS1	1
55	GPIO19	1
57	GPIO86 / LDD16	1
59	GPIO12	1
61	GPIO87 / LDD17	1
63	GPIO14	1
65	GPIO106	1
67	GPIO17	1
69	GPIO20	1
71	GPIO81	1
73	GPIO52	1
75	GPIO53	1
77	GPIO82	1
79	GPIO83	1
81	GPIO84	1
83	GND	
85	GPIO107	1
87	nRESET_OUT	1
89	nWE	1
91	nOE	1
93	RDnWR	1
95	RDY(GPIO18)(DNU up to V1.2)	1, 4, 10
97	GPIO48 / nPOE	1
99	nPWE (GPIO49)	1, 4
101	GPIO51 / nPIOW	1
103	GPIO50 / nPIOR	1
105	GPIO15 / nCS1	1
107	GPIO79 / nCS3	1
109	GND	
111	ADDRESS[00]	1
113	ADDRESS[01]	1
115	ADDRESS[02]	1
117	ADDRESS[03]	1
119	ADDRESS[04]	1
121	ADDRESS[05]	1
123	ADDRESS[06]	1
125	ADDRESS[07]	1
127	GPIO36 / OTG_VBusEn	1
129	GPIO89 / USBHost1_PEN	1
131	GPIO88 / USBHost1_O	1

Pin#	Bottom side	Note
50	GPIO69 / LDD11	1
52	GPIO70 / LDD12	1
54	GPIO71 / LDD13	1
56	GPIO76 / L_PCLK_WR	1
58	GPIO61 / LDD03	1
60	GPIO60 / LDD02	1
62	GPIO66 / LDD08	1
64	GPIO73 / LDD15	1
66	GPIO72 / LDD14	1
68	GPIO75 / L_LCLK_A0	1
70	GPIO59 / LDD01	1
72	GPIO63 / LDD05	1
74	GPIO68 / LDD10	1
76	GPIO58 / LDD00	1
78	GPIO62 / LDD04	1
80	GPIO64 / LDD06	1
82	GPIO74 / L_FCLK_RD	1
84	+3V3	
86	GPIO24 / SSPSFRM	1
88	GPIO23 / SSPSCLK	1
90	GPIO26 / SSPRXD	1
92	GPIO25 / SSPTXD	1
94	GPIO85 / nPCE1	1
96	GPIO54 / nPCE2	1
98	GPIO55 / nPREG	1
100	GPIO104 / PSKTSEL	1
102	GPIO56 / nPWAIT	1
104	GPIO57 / nIOIS16	1
106	GPIO80 / nCS4	1
108	+3V3	
110	ADDRESS[08]	1
112	ADDRESS[09]	1
114	ADDRESS[10]	1
116	ADDRESS[11]	1
118	ADDRESS[12]	1
120	ADDRESS[13]	1
122	ADDRESS[14]	1
124	ADDRESS[15]	1
126	DQM0	1
128	DQM1	1
130	DQM2	1
132	DQM3	1

Pin#	Top side (Toradex logo)	Note
133	GPIO37 / OTG_VBusPulsing	1
135	GPIO35 / OTG_SRPDetect	1
137	GPIO41 / OTG_ID	1
139	USBH_P	1
141	USBH_N-	1
143	USBC_P	1
145	USBC_N	1
147	GND	
149	DATA[00]	1
151	DATA[01]	1
153	DATA[02]	1
155	DATA[03]	1
157	DATA[04]	1
159	DATA[05]	1
161	DATA[06]	1
163	DATA[07]	1
165	DATA[08]	1
167	DATA[09]	1
169	DATA[10]	1
171	DATA[11]	1
173	DATA[12]	1
175	DATA[13]	1
177	DATA[14]	1
179	DATA[15]	1
181	GND	
183	nETH_LINK_ACT	3
185	nETH_SPEED100	3
187	ETH_TXO-	3
189	ETH_TXO+	3
191	ETH_AGND	3
193	ETH_RXI-	3
195	ETH_RXI+	3
197	GND	
199	GND	

Pin#	Bottom side	Note
134	ADDRESS[25]	1
136	ADDRESS[24]	1
138	ADDRESS[23]	1
140	ADDRESS[22]	1
142	ADDRESS[21]	1
144	ADDRESS[20]	1
146	ADDRESS[19]	1
148	+3V3	
150	DATA[16]	1
152	DATA[17]	1
154	DATA[18]	1
156	DATA[19]	1
158	DATA[20]	1
160	DATA[21]	1
162	DATA[22]	1
164	DATA[23]	1
166	DATA[24]	1
168	DATA[25]	1
170	DATA[26]	1
172	DATA[27]	1
174	DATA[28]	1
176	DATA[29]	1
178	DATA[30]	1
180	DATA[31]	1
182	+3V3	
184	ADDRESS[18]	1
186	ADDRESS[17]	1
188	ADDRESS[16]	1
190	GPIO112 / MMCMD	1
192	GPIO92 / MMDAT0	1
194	GPIO118 / I2C_DATA	1
196	GPIO117 / I2C_CLK	1
198	+3V3	
200	+3V3	

Notes

1. For the electrical specification please refer to PXA270 Processor Electrical, Mechanical and Thermal Specification Datasheet.
2. For the electrical specification please refer to Audio and Touch Screen Controller datasheet. The input voltage ranges of the analog input pins (AD[3:0]) are different depending on the Colibri module version.
   See chapter 1.4.3 and 3.18
3. For the electrical specification please refer to Ethernet Controller datasheet.
   See chapter 1.4.2.
4. Dedicated function used on Colibri PXA270 module for Ethernet Controller
   (the GPIO function is only available if no variable latency peripherals are used).
5. Must be supplied by the carrier board even if audio is not used.
6. This supply is needed for booting.
7. VDD_SENSE is connected to the PMIC's (see chapter 1.4.4) PWRFAIL_SNS and a 1MOhm pull-up and 499kOhm pull-down resistor. VDD_SENSE threshold: 3.0V. Below this value the Colibri module will enter deep sleep mode (only RTC function running). This limit can be modified by adding a pullup of 10k on the carrier board or by software after booting.
8. BATT_SENSE is connected to the PMIC's (see chapter 1.4.4) LOWBAT_SNS and a 1MOhm pull-up resistor.
9. nRESET_IN is connected to the PMIC's (see chapter 1.4.4) HOT_RESET and a 100kOhm pull-up resistor.
10. Do not use this pin on HW V 1.2 or below because it is used on the module internally (push/pull).
    You can use this pin on HW V2.1 or higher as RDY signal for VLIO transfers. This signal is pulled-up with a 4.7kOhm resistor on the module.

JTAG (X2)
Connector: FCC 8 pins, 0.5mm pitch, bottom contact

Pin Nr.	Signal name	IO Type
1	+3V3	PWR
2	GND	PWR
3	TMS	I
4	nTRST	I
5	TCK	I
6	TDO	O
7	TDI	I
8	nReset_IN	I

4.3 Additional GPIOs (X3)

Connector: FCC 18 pins, 0.5mm pitch, bottom contact

Pin Nr.	Signal name	IO Type
1	GPIO9	IO
2	GPIO13	IO
3	GPIO21	IO
4	GPIO22	IO
5	GPIO90	IO
6	GPIO91	IO
7	GPIO93	IO
8	GPIO94	IO
9	GPIO96	IO
10	GPIO97	IO
11	GPIO99	IO
12	GPIO101	IO
13	GPIO102	IO
14	GPIO103	IO
15	GPIO105	IO
16	GPIO108	IO
17	GPIO115	IO
18	GPIO116	IO

5. Compatibility to Trizeps III/IV

Colibri PXA270 modules can be used as a replacement for Keith & Koep's Trizeps III / IV family of modules. This chapter points out the differences for a smooth transition.
For more details about the compatibility of the Colibri family please refer to the 'Colibri PXA Migration Guide' datasheet.

5.1 Alternate Function Mapping

Colibri PXA270 and Trizeps share a compatible pin mapping regarding all pins as GPIOs. However, the mapping GPIOxx to SODIMM pin yy is not identical.
This fact leads to the following consequences:

- As long as Colibri PXA270 pins are used only as general purpose IOs (GPIOs), Colibri PXA270 and Trizeps III/IV are hardware compatible. Slight Software adaptions are necessary in most projects to transition between Colibri PXA270 and Trizeps III / IV to remap the GPIO pins.
- Many of the PXA270 pins are multiplexed so that they can be configured for use as a general purpose I/O signal (GPIOxx) or as one of several alternate functions (for example as interface signals). Not all of these alternate functions are available on the same Colibri PXA270 and Trizeps III / IV pins. More detailed information is available from Toradex.

5.2 USB Channels

The Colibri PXA270 module has one USB host and one USB On-The-Go (selectable host/device) channel. A third USB channel is not available on the Colibri PXA270 module.
The Colibri PXA270 module can be configured to map the USB OTG channel to pins 28 and 30 by an assembly option.

6. Technical Specifications

6.1 Electrical - DC characteristics

Symbol	Description	Min	Typ	Max	Unit
VCC	Power supply voltage	2.97	3.3	3.63	V
IDD_312A	Operating at 312 MHz, Ethernet off, Display off, Idle		141		mA
IDD_312B	Operating at 312 MHz, Ethernet off, Display on, Idle		192		mA
IDD_312C	Operating at 312 MHz, Ethernet off, Display on, 100% CPU		299		mA
IDD_624A	Operating at 624 MHz, Ethernet off, Display off, Idle		168		mA
IDD_624B	Operating at 624 MHz, Ethernet off, Display on, Idle		219		mA
IDD_624C	Operating at 624 MHz, Ethernet off, Display on, 100% CPU		408		mA
IDD_ETHL	Ethernet on		+37		mA
IDD_ETHNL	Ethernet on, no link (probing with default timings)		+7		mA
IDD_SUSP	In Suspend-Mode		1.5		mA
VIH	Digital input high voltage	2.64		VCC+0.1	V
VIL	Digital input low voltage	-0.1		0.66	V
VDD_FAULT TH	Deep sleep Threshold of VCC when: VDD_FAULT is NC and default WinCE configuration		3.00		V
VCC_RESET	Reset voltage of VCC (TPS65020)		2.35		V
TRESET	Reset period nRESET_IN	35			ms

6.2 Mechanical

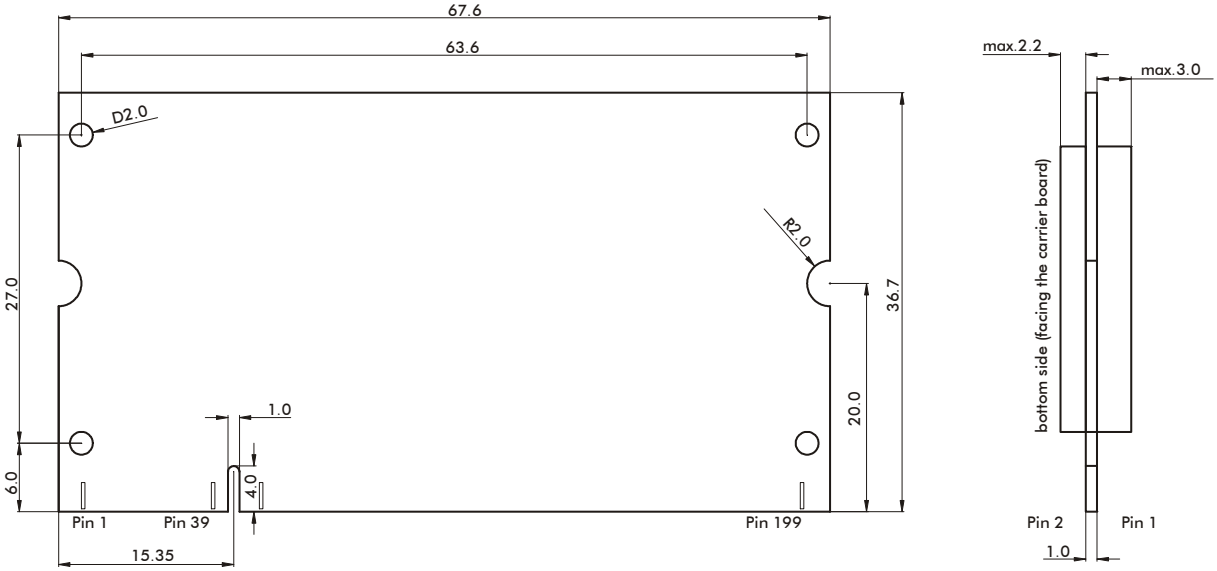

Figure 3: Mechanical dimensions of the Colibri PXA270 module
Tolerance for all measures: +/- 0.1mm

6.2.1 Sockets for the Colibri PXA270 Module

The Colibri PXA270 module fits into a regular 2.5V (DDR1) SODIMM200 memory socket. For a choice of SODIMM200 socket manufacturers please visit our wiki: http://wiki.toradex.com/

6.3 Temperature Range

Module	Description	Min	Typ	Max	Unit
Colibri PXA 270	Operating temperature range	-10		70[1]	°C

Notes:

1. The maximum temperature is limited by the case temperature of the PXA processor which must not exceed 85°C. For passive thermal solutions this may result in an ambient temperature lower than the stated value. For further details please refer to Marvell's EMTS datasheet.

6.4 RoHS Compliance

All Colibri PXA270 modules will comply with the European Union's Directive 2002/95/EC: "Restrictions of Hazardous Substances".