

General Description

The DS33M33 demo kit (DK) is an easy-to-use evaluation board for the DS33M33 and the DS33M33 Ethernet-over-SONET/SDH devices. The demo kit contains an option for either T3 or E3. The T3E3 links are complete with line interface, transformers, and network connections. Maxim's ChipView software is provided with the demo kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

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Demo Kit Contents

DS33M33DK Board

CD Including:

ChipView Software

DS33M33 Definition Files

DS33M33DK Definition File

DS33M33DK Data Sheet

DS33M33 Data Sheet

Features

- ◆ Demonstrates Key Functions of DS33M33 Ethernet Transport Chipset
- ◆ Includes Ethernet PHY Supporting 10/100 and Gigabit Modes
- ◆ Includes Optical SFP Module for SONET/SDH Interface
- ◆ Network Connectors, Transformers, and Termination Ease Connectivity
- ◆ Careful Layout Provides Signal Integrity
- ◆ On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS33M33 and DS3154 Register Set
- ◆ Software-Controlled (Register Mapped) Configuration Switches Facilitate Clock and Signal Routing
- ◆ All System Side and Overhead Pins are Easily Accessible for External Data Source/Sink
- ◆ LEDs Programmed Through GPIO Pins Provide Status
- ◆ Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

Ordering Information

PART	TYPE
DS33M33DK	Demo Kit for DS33M33

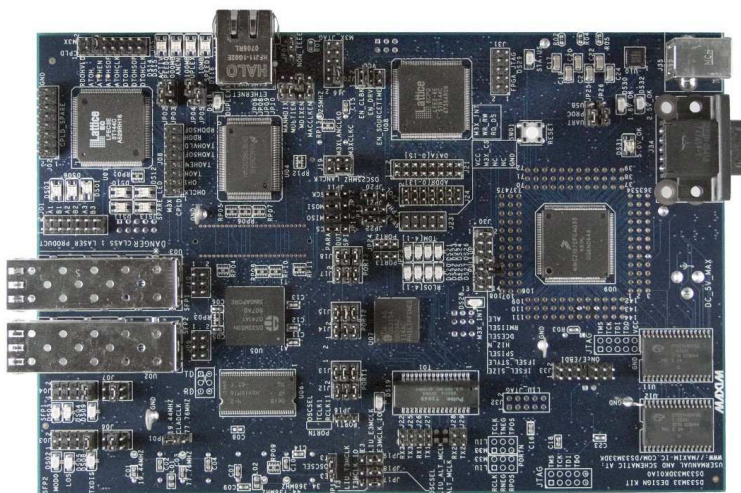


Table of Contents

1. BOARD FLOORPLAN	3
2. PC BOARD ERRATA.....	3
3. FILE LOCATIONS	4
4. BASIC OPERATION	5
4.1 POWERING UP THE DEMO KIT.....	5
4.1.1 General	5
4.2 BASIC DS33M33 INITIALIZATION.....	5
4.2.1 Additional configuration for DS33M33	5
4.3 MONITOR AND CAPTURE ETHERNET TRAFFIC	5
5. JUMPERS AND CONNECTORS	6
6. LINE-SIDE CONNECTIONS	9
7. SYSTEM CONNECTORS	9
8. MICROCONTROLLER.....	9
9. POWER-SUPPLY CONNECTORS	9
10. CONNECTING TO A COMPUTER	9
11. INSTALLING AND RUNNING THE SOFTWARE	10
12. ADDRESS MAP	11
12.1 OVERHEAD CPLD REGISTER MAP.....	11
12.2 CONTROL AND STATUS REGISTERS	12
13. ADDITIONAL INFORMATION/RESOURCES.....	16
13.1 DS33M33 INFORMATION.....	16
13.2 DS33M33DK INFORMATION.....	16
13.3 TECHNICAL SUPPORT	16
14. COMPONENT LIST.....	16
15. SCHEMATICS	21

List of Figures

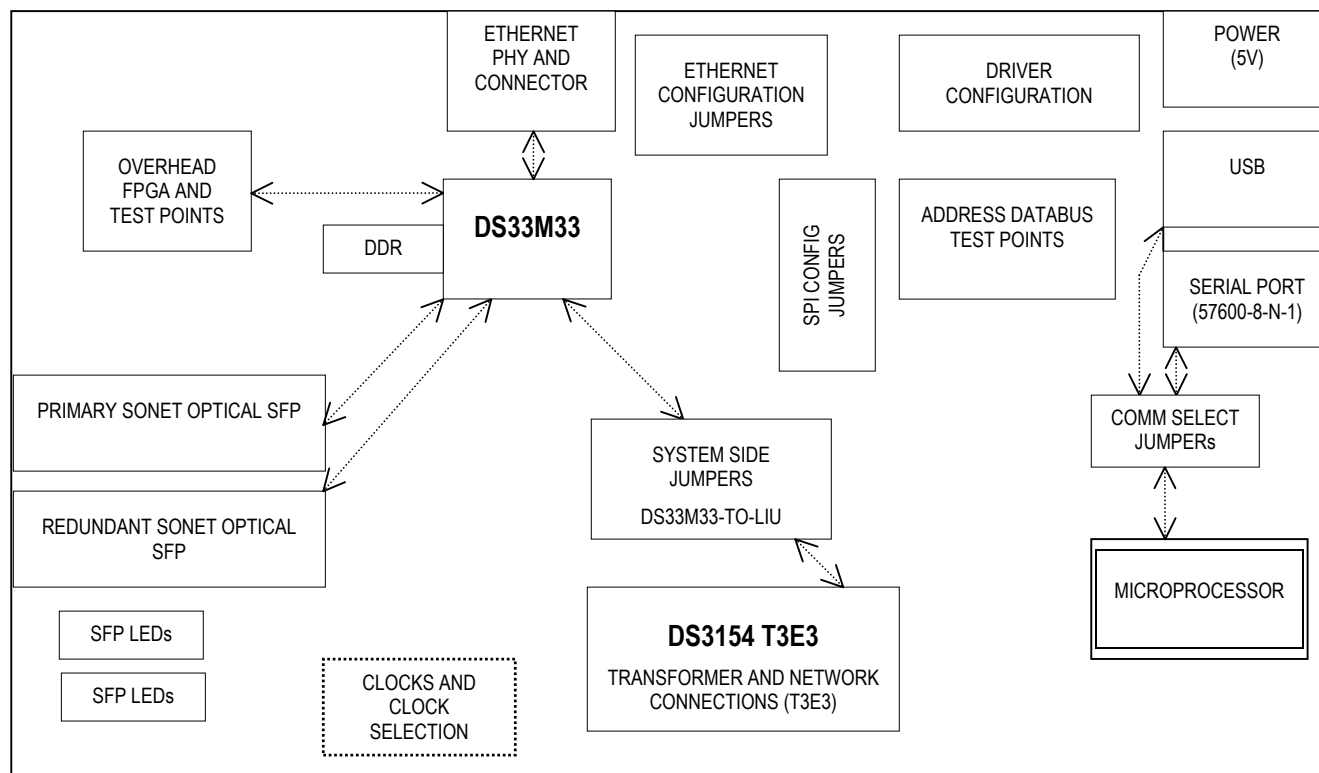
Figure 1-1. DS33M33DK Board Floorplan.....	3
Figure 15-1. DS33M33 PCB Layout and Schematic Hierarchy Block Page Listing.....	21

List of Tables

Table 3-1. Definition and Configuration Files	4
Table 5-1. Jumpers and Connectors	6
Table 12-1. Address Map	11
Table 12-2. Register Map for Overhead CPLD (Reference Designator U01)	11

1. Board Floorplan

Figure 1-1. DS33M33DK Board Floorplan



2. PCB Errata

There are no errata for the DS33M33DK02A0.

3. File Locations

This demo kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website www.maxim-ic.com/DS33M33DK. All locations are given relative to the directory in the CD/zip file called "DS33M33_def_ini_". [Table 3-1](#) shows the DS33M33, DS3154, and FPGA register definition files and configuration files.

Table 3-1. Definition and Configuration Files

FILE NAME	FILE USAGE
.\parallel_mode_DS33M_GlobalSonet.def	Top level definition file to select in ChipView's register mode. This file will autoload the remaining definition files for the DS33M33 when parallel mode is used. (Note the wan files still need to be loaded (either DS)).
.\parallel_mode\DS3154DC.def .\parallel_mode\ds33M_BufferMan.def .\parallel_mode\ds33M_EncapDecap.def .\parallel_mode\ds33M_GlobalEth.def .\parallel_mode\ds33M_group.def .\parallel_mode\ds33M_LanSubscriber.def .\parallel_mode\DS33M_port1.def .\parallel_mode\DS33M_port2.def .\parallel_mode\DS33M_port3.def .\parallel_mode\DS33M_serial_1234.def .\parallel_mode\DS33M_TEST.def .\parallel_mode\ds33M_Vcat.def .\parallel_mode\Overhead_FPGA.def	DS33M33 dependent files. These are called by _DS33M_GlobalSonet.def file, which is listed above.
.\parallel_mode\m33_eos_vcg0_port2_port3_mii.mfg	File for manually configuring the DS33M33 for EoS VC3 with two ports assigned to VCG1.
.\parallel_mode\m33_eos_vc3_mii100.mfg	File for manually configuring the DS33M33 for EoS VC3 mode.
.\parallel_mode\m33_eopos_ds3.mfg	File for manually configuring the DS33M33 for EoPoS DS3 mode.
.\parallel_mode\enc_dec_lb.mfg	Encap/decap loopback/
.\parallel_mode\m30_rx_tx.mfg	M30 mode Rx and Tx configuration. This file configures the MAC for GMII mode and requires a Gigabit Ethernet link.
.\parallel_mode\norm_ds3154_dlb.mfg .\parallel_mode\m33_pos_au3_liu.mfg	Two files for configuring the LIU in M33 mMode and configuring the DS33M33 in PoS AU3 mode.
.\spi_mode.zip	Configuration mode files for SPI™ 3-wire bus mode. The default mode for this demo kit is parallel mode. To avoid accidental use the SPI mode files have been provided in a zip format.
.\ParitalConfig_DS33M_100mBit.mfg .\ParitalConfig_DS33M_GigaBit.mfg	Files to change Ethernet speed in the MAC and Global Ethernet section.

4. Basic Operation

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

4.1 Powering Up the Demo Kit

- Connect PCB power jack to the wall adapter.
- Connect RS232 serial cable, or USB cable between the host PC and demo kit.
- Verify that the jumpers are configured as described in [Table 5-1](#).

4.1.1 General

- Upon power-up the power LEDs (DS30, DS31, DS32 green) will be lit. Note that with DS33M3301A0 board revision, the LED DS31 will be red when power conditions are correct.
- PHY LINK LED should be lit if an Ethernet cable is connected.

Following are several basic system initializations.

4.2 Basic DS33M33 Initialization

This section covers two basic methods for configuring the DS33M33.

1. Device Driver-Based Configuration: (Note: The DS33M3302A0 board revision does not come loaded with device drivers). If the pins J20.1+J20.2 are Jumpered the device driver will auto configure the DS33M33 upon power-up. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. To load the GUI interface for the device drivers, go to the ChipView register mode **Tools** menu and select **Tools→Plugins→DS33M30/M33 Device Driver Demo**.
2. Register-Based Configuration: EoS VC3 with two ports assigned to VCG1.
 - a. Remove jumper J20.1+J20.2 to disable device drivers, and reset the board.
 - b. Launch ChipView.exe and select **Register View**.
 - c. When prompted for a definition file, pick the file named **_DS33M33_GlobalMicroport.def**. Several additional definition files will load.
 - d. Go to the **File** menu and select **File→Memory Config File→Load .MFG file**. When prompted, select the file named **m33_eos_vcg0_port2_port3_mii.mfg**.

4.2.1 Additional Configuration for DS33M33

- Using either a patch or crossover cable, connect the Ethernet connector to an ordinary PC or network test equipment. This should cause the link LED to turn on.
- Place a loopback connector at the SONET network side; the optical LOS LEDs should go out.
- At this point any packets sent to the DS33M33 are echoed back. Incoming packets (i.e., ping) should cause the Activity LED to blink.
- Note that ChipView.exe display settings can be changed using the **Options→Settings** menu.

4.3 Monitor and Capture Ethernet Traffic

- Although ping is mentioned, it is **not** the recommended frame source for testing. The ping command goes through the computer's TCP/IP stack, and sometimes is not sent out the PC's network connector (i.e., if the PC's ARP cache is out of date). Additionally, ping requires two PCs, as a Windows PC with only one adapter cannot ping itself (i.e., a local ping gets sent to local host instead of out the connector). With that said, ping is still a valuable test once the prototyping stage is complete.
- Generation and capture of arbitrary (raw) packets can be accomplished using CommView. A time-limited demo is available at www.tamos.com/products/commview.
- Wireshark (formerly Ethereal) is a free packet capture utility. Download is available at www.wireshark.org.
- Adding additional Ethernet ports to a PC is rather simple when a USB-to-Ethernet adapter is used. This allows for end-to-end testing using a single PC. When using two adapters, the PC has a different IP address for each adapter. Test equipment allows selection of either adapter. Operating system-based

network traffic is sent out the default adapter, which usually is the adapter that has recently had connection to a live network.

5. Jumpers and Connectors

Jumpers and connectors are listed in [Table 5-1](#). They are listed in order of appearance on the PCB from left to right, top to bottom (as viewed with SONET connectors port on the left side of the board).

Table 5-1. Jumpers and Connectors

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J05	Overhead Test Points	J05.5+J05.6 Jumpered	2	Jumpers to connect overhead CPLD to DS33M33. Connector is marked to show that the odd numbered pins belong to the CPLD.
J02	Spare Connector	Not used	23	Spare pins connected to overhead CPLD.
J08	Overhead Test Points	—	2	Jumpers to connect overhead CPLD to DS33M33. Connector is marked to show that the odd numbered pins belong to the CPLD.
JB01 (bottom of PCB)	JTAG	—	24	CPLD JTAG header.
JP05 + JP02	Bias PHY Speed1 + Speed0	Jumper P2+1 (low) P2+1 (low)	26	If auto negotiation is enabled, this setting advertises capability for 10/100/1000 speeds. If auto negotiation is disabled, then this setting forces 10Mb mode.
		Jumper P2+3 (high) P2+3 (high)	26	If auto negotiation is enabled this setting advertises capability for 10/100 speeds. If auto negotiation is disabled, this setting is not legal.
		Jumper P2+3(high) P2+1 (low)	26	If auto negotiation is enabled, this setting advertises capability for 1000 speeds. If auto negotiation is disabled, this setting forces 1000Mb mode.
Note: In Gigabit mode the DS33M33 Mac must be configured with indirect Mac register MACCR bit 15 set.				
JP03	Bias PHY ANEN	Jumper P2+3 (high)	26	Jumper P2+3 to enable auto negotiation.
JP04	Bias PHY Duplex	Jumper P2+3 (high)	26	Jumper P2+3 to enable full duplex; jumper P1.2 to force half duplex.
JP06	Bias PHY ManMDIX	Jumper P2+1 (high)	26	Default MDIX setting P2+3 PHY is set to straight mode; P2+1 PHY is in crossover mode.
JP07	Bias PHY NonIEEE	Jumper P2+3 (high)	26	Jumper P2+3 to enable IEEE compliant operation.
JP08	Bias PHY MultiEn	Jumper P2+1 (high)	26	PHY advertisement setting. P2+3 selects multiple node priority (switch or hub); P1+2 selects single node priority (NIC).
JP09	Bias PHY MdxEn	Jumper P2+1 (high)	26	P2+3 disables pair swap mode, P2+1 enables pair swap mode

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
JP10	Bias PHY MacClkEn	Jumper P2+3 (low)	26	P2+3 PHY clock to mac output is disabled, P1+2 PHY clock to mac output is enabled. Mac clock only needs to be enabled in Gigabit mode.
DS14	LED activity	—	26	Flashes for PHY Tx-Rx activity.
DS15 DS16 DS17	LED link speed	1 of the 3 should be lit (when linked)	26	LED to indicate link speed—1000, 100, or 10Mbps. Only one of the three LEDs should be lit. See JP05 + JP02 description for setting in GMII vs. MII mode.
DS18	LED duplex	—	25	LED is on in full-duplex mode.
JB03 JB02	PHY Test Points	—	19	PHY test points. The connector pinout is compatible with existing PHY cards, but cannot be used with U04 on the board.
J16	JTAG	Jumper J16.1+J16.3	8	DS33M33 JTAG.
J20	Runtime options	NA	1	Currently the device drivers do not fit in flash, and are not loaded to the DK.
J31	JTAG	—	31	FPGA JTAG.
JP25 JP26	Comm Port	Jumper P1+2 P1+2	15	Jumper pins 1+2 to select the RS232 transceiver. Jumper pins 2+3 to select the USB to serial converter.
SW01	Reset	—	11	System reset button.
J21	Test Points	—	8	Databus test points, pins D0–D15
J24	Test Points	—	8	Address bus test points pins A0–A13.
J23	Test Points	—	8	Test points for DS33M33 CS, WR RD, and INT.
JP22 JP21 JP20	SPI Bias SWAP CPHA CPOL	Jumper P1+2	8	Jumper pins 2+1 to connect to processor parallel databus. Leave jumper off to pull pin low, jumper pins 2+3 to pull pin high.
JP14 JP13 JP12 JP11	SPI connection CS MISO MOSI SCK	Jumper P1+2	8	Jumper Pins 2+1 to connect to parallel databus. Jumper pins 2+3 to connect to SPI port.
J30	Pin Bias IFSEL_SIZE IFSEL_STYLE SPISEL HIZ DCESEL RMISEL ALE	Jumper IFSEL_STYLE HIZ_N (parallel mode)	8	Jumper to pull high, leave jumper off to pull low.
J19	Clock select	Jumper P2+4	6	Clock selection for PHY and Ethernet side of DS33M33.
JP01	Clock select	Jumper P1+2	6	Clad clock selection, jumper P1+2 to drive with 19.44MHz. Jumper P2+3 to drive with 77.76MHz clock.

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J09 J10	SerDes analog test points	—	3, 4	Test points to view analog +/- differential SerDes signals. To loopback DS33M33 Tx→Rx remove the SFP and jumper P3+5 and P2+6.
J03 J04	SFP test points	Jumper P9+10	3	Test points for SFP module.
DS02 DS03	SFP MOD0	—	3	Lit when a SFP module is installed.
DS08 DS09	SFP TXDISABLE	—	3	Lit when Tx is enabled.
DS05 DS04	SFP LOS	—	3	Lit when fiber optic cable is removed.
J06 J07	SFP LOS / M33 LOS	Jumper P2+3	3, 4	Jumper P2+3 to connect SFP LOS to DS33M33 LOS. Jumper P2+4 to pull DS33M33 high. Jumper P2+6 to pull DS33M33 low.
U03	SFP	Installed	3, 4	Primary SFP module.
U02	SFP	Not Installed	3, 4	Redundant SFP module.
J33	Software Debug	—	15	ONcE EBDI.
J32	JTAG	—	20	LIU JTAG.
J13 J15 J18	RCLK RNEG RPOS	Jumpered	9	LIU-to-DS33M33 connections.
J13 J15 J18	TCLK TNEG TPOS	Jumpered	9	LIU-to-DS33M33 connections.
JP16 JP23 JP24	LIU Port Clocks	Not used	9	Jumper 1+2 to drive TCLKn with OscSel. Jumper 2+3 to drive TCLKn with RCLKn.
J22 J25 J26 J27 JB05 JB06 J28 J29	RX3 TX3 RX1 TX1 RX4 (bottom of PCB) TX4 (bottom of PCB) RX2 TX2	—	8	Rx Tx jumpers.
JP17	LIU_T3MCLK	Jumper P2+3	20	Jumper P2+3 to drive with T3 Osc. Jumper P1+2 to drive with T3_MCLK_IO.
JP18	LIU_ALT_MCLK	Jumper P2+3	20	Jumper P2+3 to drive with Osc Sel. Jumper P1+2 to drive with Alternate MCLK.
JP19	LIU_E3MCLK	Jumper P2+3	20	Jumper P2+3 to drive with E3 Osc. Jumper P1+2 to drive with E3_MCLK_IO.
JP15	Osc Select	Jumper P2+3	20	Jumper P2+3 to drive with T3 Osc. Jumper P1+2 to drive with E3 Osc.

6. *Line-Side Connections*

The DS33M33DK has two optical ports: one Ethernet port and three T3E3 ports.

7. *System Connectors*

System-side signals can be accessed from test point headers. The headers are clearly labeled with signal information.

8. *Microcontroller*

The microcontroller has factory-installed firmware in on-chip nonvolatile memory. This firmware translates memory access requests from the RS-232 serial port into register accesses on the DS33M33 and the FPGAs.

9. *Power-Supply Connectors*

Connect a 5.0V wall adapter to the PCB power jack. LED DS1 provides indications that a 5.0V supply is connected properly. The board power supplies (3.3V, 2.5V, and 1.8V) are regulated to supply proper voltages to various circuits on the board.

10. *Connecting to a Computer*

Both USB and serial modes are supported.

To connect through a RS-232 serial port, set jumpers JP25 and JP26 jumpers to pins 1+2, identified in the silkscreen as UART,PROC. Connect a standard DB-9 serial cable between the serial port on the DS33M33DK and an available serial port on the host computer. The host computer must be a Windows-based PC. Be sure the cable is a standard straight-through cable rather than a null-modem cable. Null-modem cables prevent proper operation.

To connect through USB, set jumpers JP25 and JP26 jumpers to pins 3+2, identified in the silkscreen as USB,PROC. Connect a USB cable between the DS33M33DK USB connector and the PC. The host computer must be a Windows-based PC, which should automatically recognize the device as a virtual com port and assign the device drivers. If drivers are not automatically assigned, direct the **New Hardware** wizard to the driver files on the CD in the folder marked **USBdrivers_CP210x**.

11. Installing and Running the Software

ChipView is a general-purpose program that supports a number of Maxim demo kits. To install the ChipView software, run Chipview.msi from the disk included in the DS33M33DK box or from the zip file downloadable on our website at www.maxim-ic.com/DS33M33DK.

After installation, run the ChipView program with the DS33M33DK board powered up and connected to the PC. If the default installation options were used, one easy way to run ChipView is to click the **Start** button on the Windows toolbar and select **Programs→ChipView→ChipView**. In the opening screen, click the **Register View** button. Select the correct serial port in the **Port Selection** dialog box, then click **OK**.

Next, the **Definition File Assignment** window appears. This window has subwindows to select definition files for up to four separate boards on other Maxim evaluation platforms. In the active subwindow, select the **_DS33M_GlobalSonet.def** definition file from the list shown, or browse to find it in another directory. Press the **Continue** button.

After selecting the definition file, the main part of the ChipView window displays the DS33M33's register map. To select a register, click on it in the register map. When a register is selected, the full name of the register and its bit map are displayed at the bottom of the ChipView window. Bits that are logic 0 are displayed in white, while bits that are logic 1 are displayed in green.

The ChipView software supports the following actions:

- **Toggle a bit.** Select the register in the register map and then click the bit in the bit map.
- **Write a register.** Select the register, click the **Write** button, and enter the value to be written.
- **Write all registers.** Click the **Write All** button and enter the value to be written.
- **Read a register.** Select the register in the register map and click the **Read** button.
- **Read all registers.** Click the **Read All** button.

12. Address Map

Address space begins at 0x81000000. All offsets given in the following tables are relative to 0x81000000. Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named **Overhead_FPGA.def**.

Table 12-1. Address Map

OFFSET	DEVICE	DESCRIPTION
0X6000	FPGA	Overhead CPLD and Clock/Signal Routing
0X4000	DS3154	DS3154 Line Interface Unit
0X0000	DS33M33	DS33M33 Registers

12.1 Overhead CPLD Register Map

Table 12-2. Register Map for Overhead CPLD (Reference Designator U01)

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0001	ATOH_CFG	Control	ATOH Configuration
0X0002	ATOHEN_CFG	Control	ATOHEN Configuration
0X0003	GPIOAwr	Control	GPIO A Output Enable + Write Value
0X0004	GPIOBwr	Control	GPIO B Output Enable + Write Value
0X0005	DTOH_STAT	Read-Only	DTOH Status
0X0006	DTOH_SEL	Control	DTOH Configuration
0X0007	GPIOrd_STAT	Read-Only	GPIO Read Values
0X0008	RDOH_STAT	Read-Only	RDOH Status
0x000A	RDOH_SEL	Control	RDOH Select
0x000D	TAOH_CFG	Control	TAOH Configuration
0x000F	TAOHen_CFG	Control	TAOHen Configuration

12.2 Control and Status Registers

Register Name: **ATOH_CFG**

Register Description: **ATOH Configuration**

Register Offset: **0x0001**

Bit #	7	6	5	4	3	2	1	0
Name								
Default	0	0	0	0	0	0	0	0

This register sets the overhead transport data byte value, which is positioned by the following register, **ATOHEN_CFG**.

Register Name: **ATOHEN_CFG**

Register Description: **ATOHEN Configuration**

Register Offset: **0x0002**

Bit #	7	6	5	4	3	2	1	0
Name								
Default	0	0	0	0	0	0	0	0

Byte enable for overhead transport byte, the data value in **ATOH_CFG** is positioned in the overhead as specified by **ATOHEN_CFG**. Examples follow:

ATOHEN_CFG	ATOH_CFG	RESULT
0	NA	Data is not written onto the overhead when ATOHEN_CFG = 0.
0x01	0x54	Data value 0x54 is written onto the first byte of the transport overhead.
0x81	0x54	Data value 0x54 is written onto the last byte of the transport overhead.
0x##	0xNN	Data value 0xNN is written to the 0x## byte of the transport overhead.

Register Name: **GPIOAwr**Register Description: **GPIO A Output Enable + Write Value**Register Offset: **0x0003**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	GPIOa3 Output En	GPIOa3 Value	GPIOa2 Output En	GPIOa2 Value	GPIOa1 Output En	GPIOa1 Value
Default	0	0	0	0	0	0	0	0

Bits 5 and 4: DS33M33 GPIOA_3 Three-State and Level

0x = FPGA three-states GPIOA_3 pin

00 = FPGA drives GPIOA_3 pin with 0.0V

01 = FPGA drives GPIOA_3 pin with 3.3V

Bits 3 and 2: DS33M33 GPIOA_2 Three-State and Level

0x = FPGA three-states GPIOA_2 pin

00 = FPGA drives GPIOA_2 pin with 0.0V

01 = FPGA drives GPIOA_2 pin with 3.3V

Bits 1 and 0: DS33M33 GPIOA_1 Three-State and Level

0x = FPGA three-states GPIOA_1 pin

00 = FPGA drives GPIOA_1 pin with 0.0V

01 = FPGA drives GPIOA_1 pin with 3.3V

Register Name: **GPIOBwr**Register Description: **GPIO B Output Enable + Write Value**Register Offset: **0x0004**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	GPIOb3 Output En	GPIOb3 Value	GPIOb2 Output En	GPIOb2 Value	GPIOb1 Output En	GPIOb1 Value
Default	0	0	0	0	0	0	0	0

Bits 5 and 4: DS33M33 GPIOB_3 Three-State and Level control

0x = FPGA three-states GPIOB_3 pin

00 = FPGA drives GPIOB_3 pin with 0.0V

01 = FPGA drives GPIOB_3 pin with 3.3V

Bits 3 and 2: DS33M33 GPIOB_2 Three-State and Level control

0x = FPGA three-states GPIOB_2 pin

00 = FPGA drives GPIOB_2 pin with 0.0V

01 = FPGA drives GPIOB_2 pin with 3.3V

Bits 1 and 0: DS33M33 GPIOB_1 Three-State and Level control

0x = FPGA three-states GPIOB_1 pin

00 = FPGA drives GPIOB_1 pin with 0.0V

01 = FPGA drives GPIOB_1 pin with 3.3V

Register Name: **DTOH_STAT**
 Register Description: **DTOH Status**
 Register Offset: **0x0005**

Bit #	7	6	5	4	3	2	1	0
Name	STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0
Default	0	0	0	0	0	0	0	0

Read value of 1 of 81 bytes selected by DTOH_SEL.

Register Name: **DTOH_SEL**
 Register Description: **DTOH Configuration**
 Register Offset: **0x0006**

Bit #	7	6	5	4	3	2	1	0
Name	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
Default	0	0	0	0	0	0	0	0

Byte select for overhead transport byte, the overhead byte specified by DTOH_CFG is written to DTOH_STAT.

Examples:

DTOH_SEL	DTOH_STAT	RESULT
0	First byte	The first byte of the transport overhead is written to DTOH_STAT.
0x80	Last byte	The last byte of the transport overhead is written to DTOH_STAT.

Register Name: **GPIOd_STAT**
 Register Description: **GPIO Read Values**
 Register Offset: **0x0007**

Bit #	7	6	5	4	3	2	1	0
Name	—	GPIOA3	GPIOA2	GPIOA1	—	GPIOB3	GPIOB2	GPIOB1
Default	0	0	0	0	0	0	0	0

Bit 6: DS33M33 GPIOA3 Pin Value

Reflects the value of DS33M33 GPIOA3 pin.

Bit 5: DS33M33 GPIOA2 Pin Value

Reflects the value of DS33M33 GPIOA2 pin.

Bit 4: DS33M33 GPIOA1 Pin Value

Reflects the value of DS33M33 GPIOA1 pin.

Bit 2: DS33M33 GPIOB3 Pin Value

Reflects the value of DS33M33 GPIOB3 pin.

Bit 1: DS33M33 GPIOB2 Pin Value

Reflects the value of DS33M33 GPIOB2 pin.

Bit 0: DS33M33 GPIOB1 Pin Value

Reflects the value of DS33M33 GPIOB1 pin.

Register Name: **RDOH_STAT**
 Register Description: **RDOH Status**
 Register Offset: **0x0008**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Read value from the member and byte selected by RDOH_SEL[7:4] and RDOH_SEL[3:0]

Register Name: **RDOH_SEL**
 Register Description: **RDOH Select**
 Register Offset: **0x000A**

Bit #	7	6	5	4	3	2	1	0
Name	IF3	IF2	IF1	IF0	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Overhead interface Member Select. Writing IF[3:0] to a value of 0 disables. Writing 1 to 10 selects among the 10 members used in RDOH_STAT.

Bits 3 to 0: Byte Select. Writing B[3:0] to a value of 0-to-N selects the Nth byte in the member selected.

Register Name: **TAOH_CFG**
 Register Description: **TAOH Configuration**
 Register Offset: **0x000D**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Value to be written to the member and byte selected by TAOHen_CFG[7:4] and TAOHen_CFG [3:0]

Register Name: **TAOHen_CFG**
 Register Description: **TAOH Enable Configuration**
 Register Offset: **0x000F**

Bit #	7	6	5	4	3	2	1	0
Name	IF3	IF2	IF1	IF0	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Overhead interface Member Select. Writing IF[3:0] to a value of 0 disables. Writing 1 to 10 selects among the 10 members used in TAOH_STAT.

Bits 3 to 0: Byte Select. Writing B[3:0] to a value of 0-to-N selects the Nth byte in the member selected.

13. Additional Information/Resources

13.1 DS33M33 Information

For more information about the DS33M33, refer to the DS33M33 data sheet at www.maxim-ic.com/DS33M33.

13.2 DS33M33DK Information

For more information about the DS33M33DK, refer to the DS33M33DK Quick View page at www.maxim-ic.com/DS33M33DK.

13.3 Technical Support

For additional technical support, submit your questions at www.maxim-ic.com/support.

14. Component List

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C08, CB34, CB36, CB37, CB38, CB39, CB40, CB41, CB42, CB58, CB64, CB66, CB67, CB68, CB72, CB79, CB92, CB101, CB104, CB112, CB170	21	L_0603 CERAM .01uF 50V 10% X7R	AVX	06035C103KAT
See next row (begins with C02)	61	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
C02, C04, C05, C07, C10, C15, C18, CB05, CB06, CB09, CB10, CB11, CB12, CB16, CB21, CB22, CB23, CB25, CB28, CB33, CB43, CB44, CB45, CB47, CB53, CB54, CB63, CB65, CB69, CB77, CB83, CB85, CB88, CB89, CB94, CB95, CB97, CB98, CB113, CB115, CB116, CB118, CB122, CB126, CB128, CB134, CB135, CB137, CB138, CB140, CB142, CB143, CB144, CB146, CB148, CB156, CB160, CB168, CB177, CB186, CB187				
DB01	1	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS06, DS07, DS10, DS11, DS12, DS13, DS31	8	LED, RED/GREEN, SMD	LITEON	160-1172-1-ND
GND_TP01, GND_TP02, GND_TP03, GND_TP04, GND_TP11, GND_TPB01, GND_TPB02, GND_TPB03, GND_TPB06	9	STANDARD GROUND CLIP	KEYSTONE	4954
DS14, DS15, DS16, DS17	4	LED, GREEN/GREEN, SMD	LUMEX	67-1362-1-ND
J34	1	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
UB02, UB04, UB06	3	SPI SERIAL EEPROM 2M 8 PIN SOIC 2.7V to 3.6V	Atmel	AT25F2048N-10SU-2.7
RPB24, RPB26	2	RESISTOR, 4 PACK, 50 OHM 2PCT QUAD 0603	KOA	CN1J4TTD500G
U10	1	IC, SINGLE-CHIP USB TO UART BRIDGE, 28 PIN QFN	SIL	CP2101
J32	1	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPULATE	DNP	DNP
U04	1	GIG PHYTER V, 10/100/1000 ETHERNET PHYSICAL LAYER, 128 PIN QFP	National Semiconductor	DP83865DVH
U07	1	QUAD DS3/E3/STS1 LIU 144P BGA	Maxim	DS3154
U05	1	IC, ETHERNET OVER SDH/SONET (EoS), -40C TO 85C, 256-PIN CSBGA	Maxim	DS33M33N
XB01	1	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
See next row (begins with C01)	79	0603 CERAM 4.7uF 6.3V MULTILAYER	Digi-Key	ECJ-1VB0J475M
C01, C03, C06, C09, C11, C12, C13, C14, C16, C23, CB03, CB04, CB07, CB14, CB15, CB17, CB18, CB19, CB20, CB24, CB26, CB27, CB29, CB30, CB31, CB32, CB46, CB49, CB55, CB60, CB62, CB70, CB73, CB74, CB75, CB76, CB78, CB82, CB84, CB86, CB90, CB91, CB93, CB96, CB100, CB102, CB103, CB106, CB107, CB109, CB110, CB114, CB117, CB119, CB120, CB121, CB123, CB127, CB129, CB131, CB132, CB133, CB136, CB139, CB141, CB147, CB150, CB153, CB154, CB162, CB163, CB165, CB167, CB173, CB175, CB181, CB182, CB183, CB190				
See next row (begins with CB50)	20	0603 CERAM .1uF 16V 10%	Panasonic	ECJ-1VB1C104K

CB50, CB56, CB57, CB61, CB71, CB80, CB81, CB87, CB99, CB105, CB108, CB149, CB151, CB152, CB155, CB161, CB166, CB172, CB179, CB180				
See next row (begins with C17)	21	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
C17, C19, C20, C21, C22, C24, CB188, CB01, CB02, CB08, CB13, CB35, CB48, CB51, CB52, CB59, CB111, CB124, CB125, CB130, CB169				
CB164, CB184	2	L_1206 CERAM 1uF 16V 10%	Panasonic	ECJ-3YB1C105K
CB178	1	1206 CERAM 4.7uF 25V 10% X5R	Panasonic	ECJ-3YB1E475K
CB158, CB159, CB185, CB189	4	L_D CASE TANT 68uF 16V 20%	Panasonic	ECS-T1CD686R
RB09, RB10	2	RES 0603 100 Ohm 1/16W 1%	Panasonic	ERJ-3EKF1000V
RB12, RB13	2	RES 0603 1.00K Ohm 1/16W 1%	Panasonic	ERJ-3EKF1001V
RB17, RB19, RB20, RB21, RB22, RB23, RB24, RB25	8	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
RB16	1	RES 0603 9.76K Ohm 1/16W 1%	Panasonic	ERJ-3EKF9761V
R02, R04, R05, RB04, RB27	5	RES 0603 0.0 Ohm 1/16W 5%	Panasonic	ERJ-3GEY0R00V
RB01, RB02, RB29, RB05	4	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
R03	1	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R01, RB06, RB11	3	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
RB08	1	RES 0603 2.2K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ222V
RB14, RB15	2	RES 0603 30 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ300V
RB07, RB26, RB28, RB30	4	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
RB03, RB18	2	RES 0805 10K Ohm 1/10W 1%	Panasonic	ERJ-6ENF1002V
SW01	1	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
RPB18	1	RESISTOR, 4 PACK, 100 OHM 5PCT QUAD 0603	Panasonic	EXB-V8V101JX
RPB01, RPB02, RPB05, RPB14, RPB20, RPB30, RPB36, RPB48, RPB52	9	RESISTOR, 4 PACK, 1K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V102JX
RPB03, RPB08, RPB10, RPB11, RPB12, RPB13, RPB29, RPB32, RPB33, RPB40, RPB41, RPB43, RPB45, RPB47, RPB49, RPB50, RPB51, RPB54, RPB55, RPB56, RPB57, RPB58, RPB60, RPB61, RPB62, RPB63, RPB64	27	RESISTOR, 4 PACK, 10K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V103JX
RPB19, RPB21, RPB28	3	RESISTOR, 4 PACK, 2.2K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V222JX
RP02, RP03, RP04, RP05, RP06, RP07, RP08, RP09, RP10, RP11, RP12, RP13, RPB15, RPB16, RPB17, RPB23, RPB25, RPB27, RPB31, RPB34, RPB35, RPB37, RPB44	23	RESISTOR, 4 PACK, 30 OHM 5PCT QUAD 0603	Panasonic	EXB-V8V300JX
RP01, RPB04, RPB06, RPB07, RPB09, RPB22, RPB38, RPB39, RPB42, RPB46, RPB53, RPB59	12	RESISTOR, 4 PACK, 330 OHM 5PCT QUAD 0603	Panasonic	EXB-V8V331JX
L01, L02, LB01, LB02, LB03, LB04	6	1uH $\pm$ 10% 0805 Multilayer Ceramic 400 mA	TDK	GLF2012T1R0M

J01, J30	2	HEADER, 14 PIN, DUAL ROW, VERT	Samtec	HDR-TSW-107-14-T-D
J11	1	CONNECTOR, SINGLE LEVEL, GIGABIT RJ-45, 10 PIN	Halo Electronics	HFJ11-1G02E
U08	1	IC, FPGA, 1.2V, 20X20 TQFP, 144 PIN	LAT	LFE2-6E-5TN144C
U01	1	IC, FPGA, 1.2V, 20X20 TQFP, 144 PIN	LAT	LFEC3E-3T144C
DS04, DS05, DS28, DS19, DS20, DS21, DS22, DS23, DS24, DS25, DS26, DS27	12	L_LED, RED, SMD	Panasonic	LN1251C
DS02, DS03, DS08, DS09, DS29, DS18, DS30, DS32	8	L_LED, GREEN, SMD	Panasonic	LN1351C
UB09	1	IC, LINEAR REG 1.5W, 1.8V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-18
UB08	1	IC, LINEAR REG 1.5W, 2.5V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-25
UB10, UB11, UB13	3	IC, LINEAR REG 1.5W, 3.3V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-33
UB01, UB03	2	IC, LDO REGULATOR WITH RESET, 1.20V OUTPUT 300 MA, 6 PIN SOT23	Maxim	MAX1963Ezt120-T
UB07	1	MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143	Maxim	MAX811TEUS-T
U09	1	MMC2107 PROCESSOR	Motorola	MMC2107
J03, J04, J23	3	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Digi-Key	S2012-05-ND
J33	1	100 MIL 2*7 POS JUMPER	NA	NA
J35	1	TYPE B SINGLE RT ANGLE, BLACK	Digi-Key	WM17108-ND
JB08	1	100 MIL 2 POS JUMPER	NA	NA
See next row (begins with JP01)	27	100 MIL 3 POS JUMPER	NA	NA
JP01, JP02, JP03, JP04, JP05, JP06, JP07, JP08, JP09, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22, JP23, JP24, JP25, JP26, JPB01				
TPB01, TPB02, TPB03	3	TEST POINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U06	1	DOUBLE DATA RATE (DDR) SDRAM 2-2-2 TIMING 256MBITX16 TSSOP	MICRON	MT46V16M16TG-75E
U11, U12	2	CYPRESS SRAM 4Mbit*8	CYPRESS	CY62148DV30L-70SXI
UB14	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	MAX3233E
JB02	1	TEST POINTS FOR SMD 50 PIN, 2 ROW VERTICAL	NA	NA_NOTPOPULATED
UB05, UB12	2	HIGH SPEED INVERTER	FAIRCHILD	NC7SZ86
J24	1	NON POPULATED HEADER, 14 PIN, DUAL ROW, VERT	Samtec	NOPOP-HDR-TSW-107-14-T-D
JB05, JB06	2	DO NOT POPULATE L_2 PIN HEADER, .100 CENTERS, VERTICAL	Samtec	NOPOP-TSW-102-07-T-S
J09, J10	2	TERMINAL STRIP, 6 PIN, DUAL ROW, VERT NOT POPULATED	Samtec	NOPOP-TSW-103-07-T-D
J21	1	NOPOP TERMINAL STRIP, 16 PIN, DUAL ROW, VERT	Samtec	NOPOP-TSW-108-07-T-D
YB04	1	OSCILLATOR, CRYSTAL CLOCK, 5.0V - 34.368 MHZ	SaRonix	NTH089AA-34.368
YB05	1	SOCKETED OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ	SaRonix	NTH089AA3-25.000+SOCKET
YB03	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3-44.736

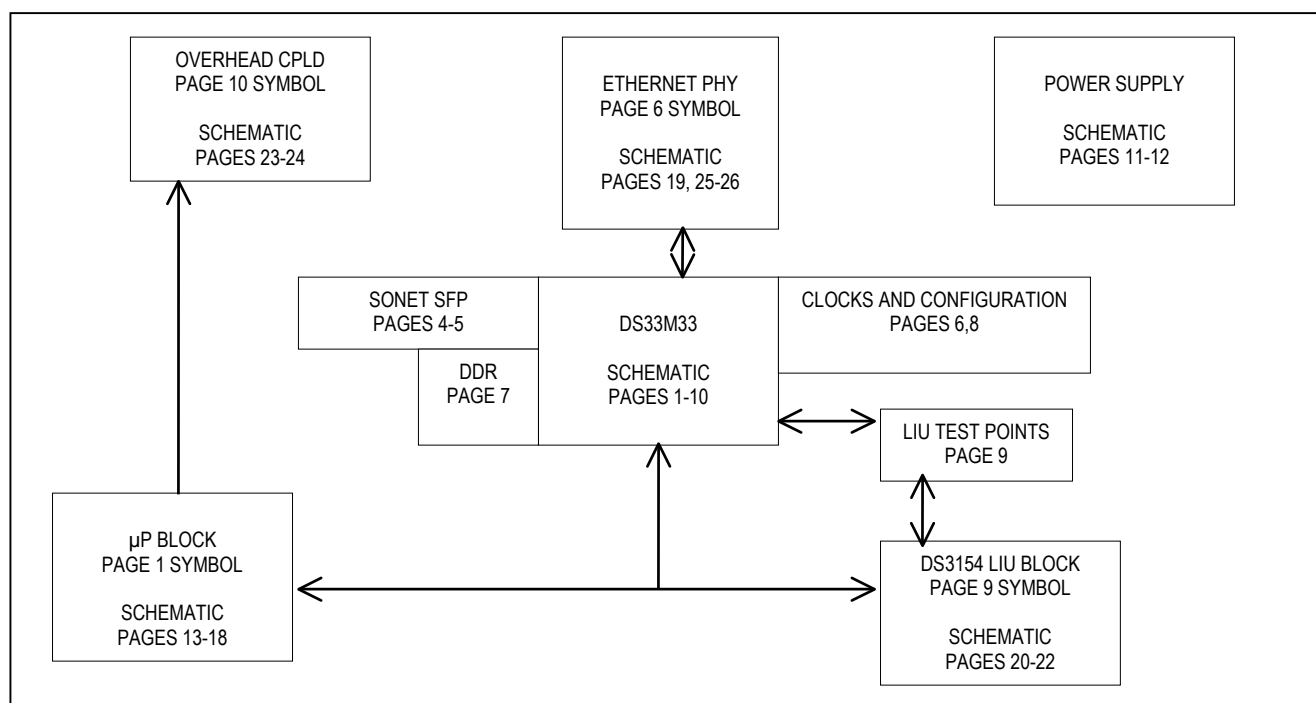
JB09	1	CONN 2.1MM/5.5MM PWRJACK RT ANGLE PCB, closed frame, high current 24VDC@5A also requires 5V ACDC adapter INPUT 100-240VAC 50-60HZ 0.6A OUTPUT DC 5V 2.6A. PN DMS050260-P5P-SZ. MODEL 3Z-161WP05	CUI, INC	PJ-002AH
JB03	1	PLUG, SMD, 50 PIN, 2 ROW VERTICAL	Samtec	SFM-125-L2-S-D-LC
U02, U03	2	SFP host / receptacle	PARTS_KIT	SFP_HOST-TYCO
HB01, HB02, HB03, HB04, HB05	5	Rubber bumper 0.5 inch	NA	SJ5518-0
YB01	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 19.44 MHZ	SaRonix	SOCKET+NTH089A 3-19.44
YB02	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 77.76 MHZ	SaRonix	SOCKET+NTH089A 3-77.7600
T01	1	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
CB145, CB157, CB171, CB174, CB176	5	D CASE TANT 470uF 6.3V 20%	KEM	T491D477M006AS
J22, J25, J26, J27, J28, J29	6	L_2 PIN HEADER, .100 CENTERS, VERTICAL	Samtec	TSW-102-07-T-S
J06, J07, J12, J13, J14, J15, J17, J18, J19, J20, JB04, JB07	12	TERMINAL STRIP, 6 PIN, DUAL ROW, VERT	Samtec	TSW-103-07-T-D
J16, J31, JB01	3	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Samtec	TSW-105-07-T-D
J02, J05, J08	3	TERMINAL STRIP, 16 PIN, DUAL ROW, VERT	Samtec	TSW-108-07-T-D

15. Schematics

The DS33M33DK schematics are featured in the following pages. The schematic contains five hierarchical blocks: Microcontroller, DS3154, Ethernet PHY, Ethernet Test Points, and Overhead CPLD.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here blocks are wired together as if they were ordinary components. [Figure 15-1](#) shows the system diagram in terms of hierarchical blocks with schematic page numbers given for each functional block.

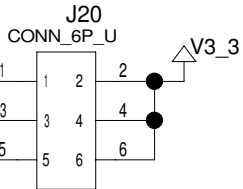
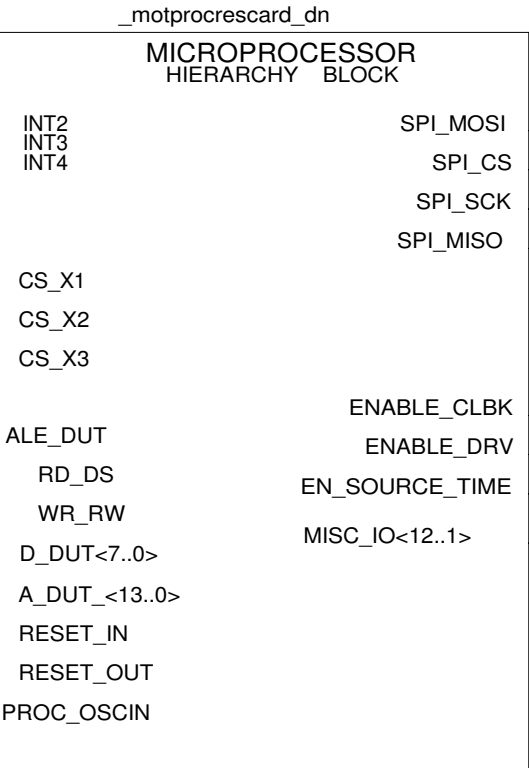
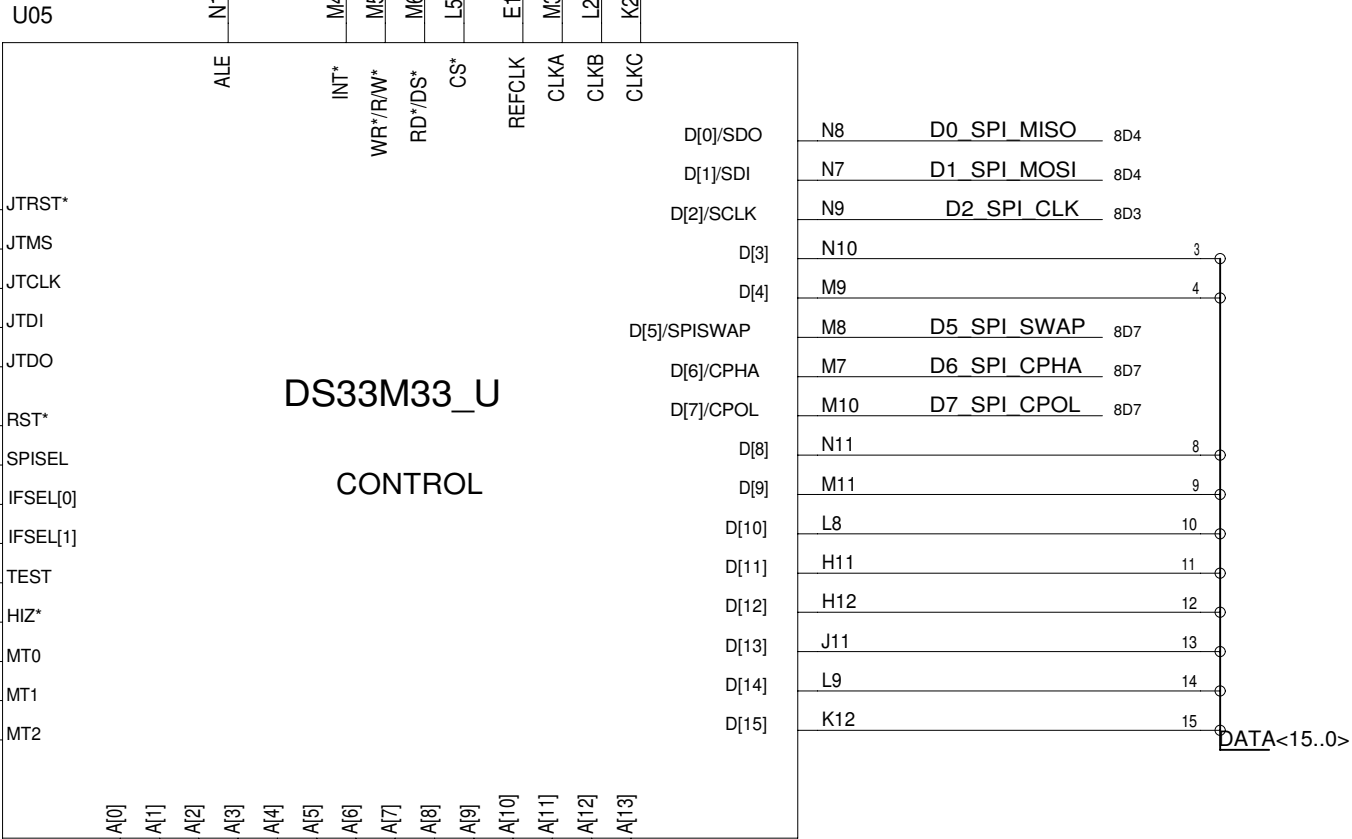
Figure 15-1. DS33M33 PCB Layout and Schematic Hierarchy Block Page Listing



DS33M33DK CONTENTS / INDEX

MICROPORT.	P.1,13-18
OVERHEAD.	P.2,10,23-24
T3E3 LIU I/F.	P.2,9,20-22
SERDES.	P.3-4
ETHERNET.	P.5-6,19,25-26
DDR MEMORY.	P.7
OSCILLATORS.	P.6
BIAS+CONFIG.	P.8
POWER.	P.11-12

8A6	M3X_JTRST	N4	JTRST*
8A7	M3X_JTMS	P1	JTMS
8A7	M3X_JTCLK	N2	JTCLK
8A8	M3X_JTDI	P2	JTDI
8A7	M3X_JTDO	N3	JTDO
9B1	RESET_SYS	C1	RST*
8A2	M3X_SPISEL	N6	SPISEL
8A2	M3X_IFSEL_STYLE	P7	IFSEL[0]
8A2	M3X_IFSEL_SIZE	N5	IFSEL[1]
8A8	M3X_TEST_EN	F5	TEST
8B2	M3X_HIZ_N	B1	HIZ*
8B8	M3X_MT0	B2	MT0
8B8	M3X_MT1	A1	MT1
8B8	M3X_MT2	M2	MT2



BEGINNING OF DS33M33DK

TITLE: DS33M33DK01A0	DATE:
MICROPORT. P.1,13-18	10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 1/12(BLOCK) 1/26(TOTAL)

D

D

C

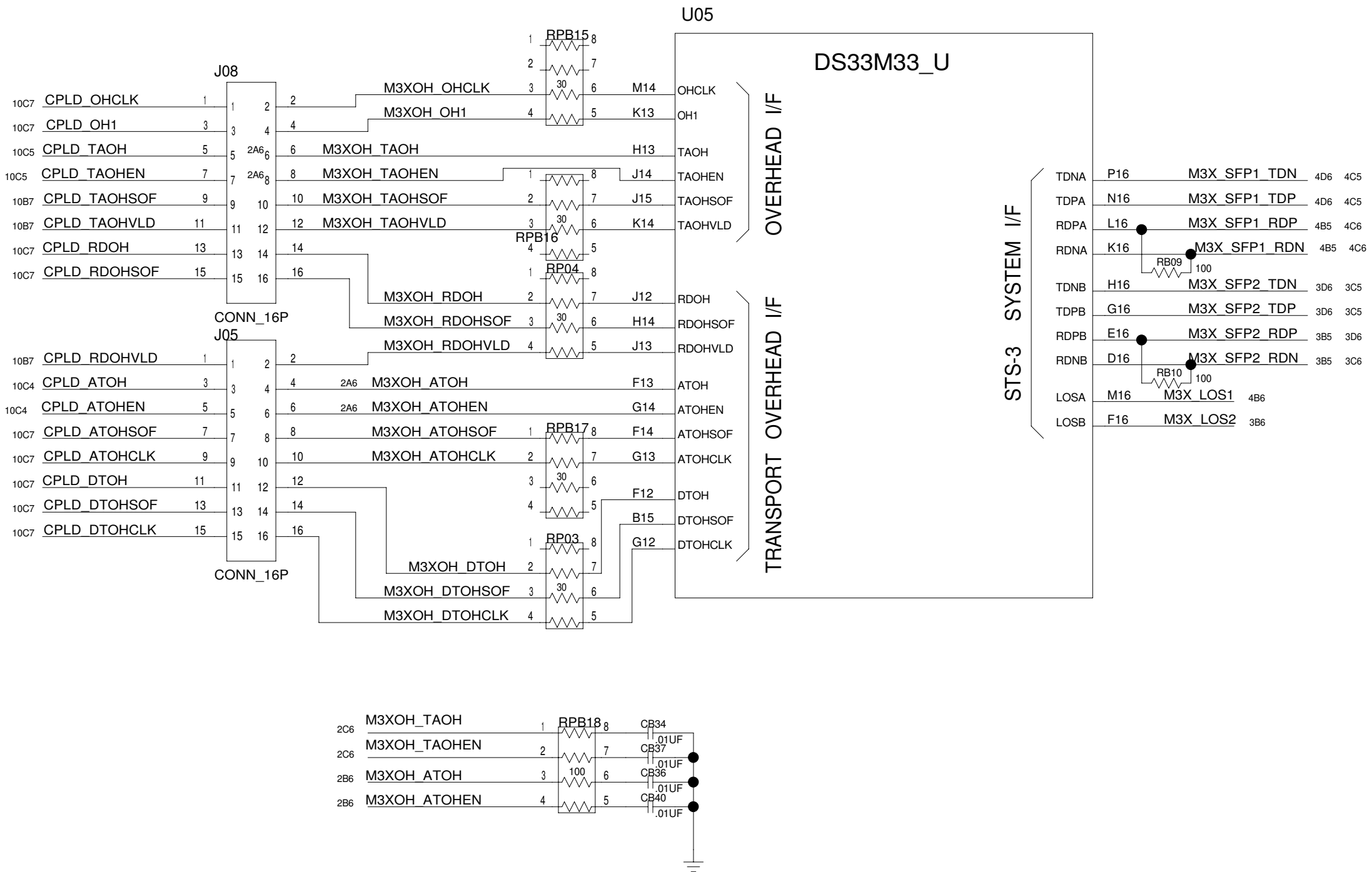
C

B

B

A

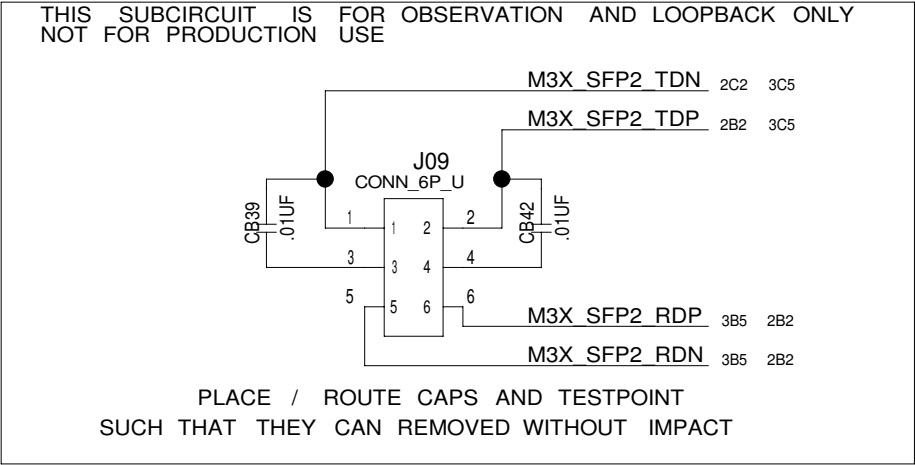
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TITLE: DS33M33DK01A0		DATE:
OVERHEAD. T3E3 LIU I/F.		P.2,10,23-24 P.2,9,20-22
ENGINEER: STEVE SCULLY		PAGE: 2/12(BLOCK) 2/26(TOTAL)

D

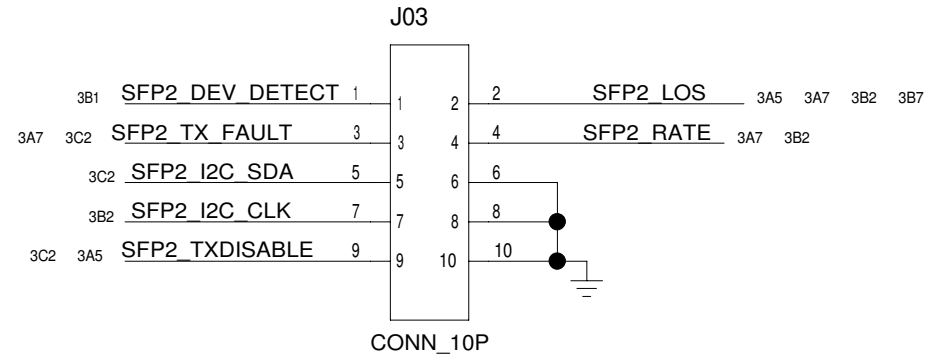
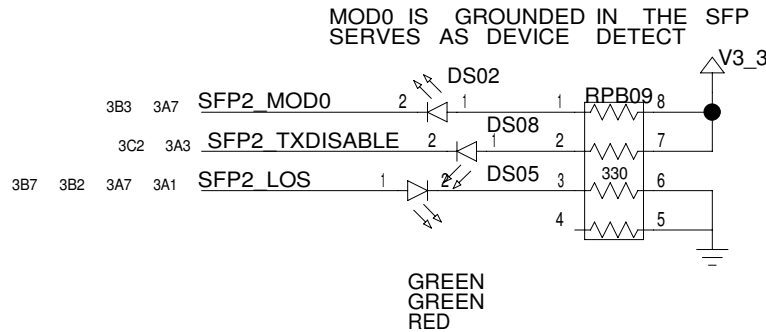
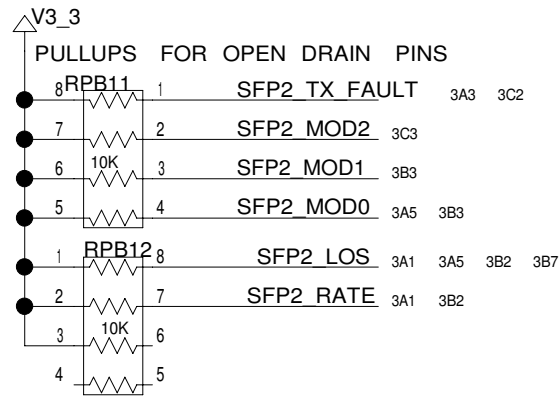
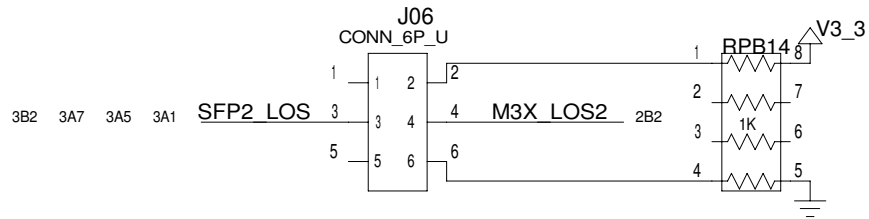
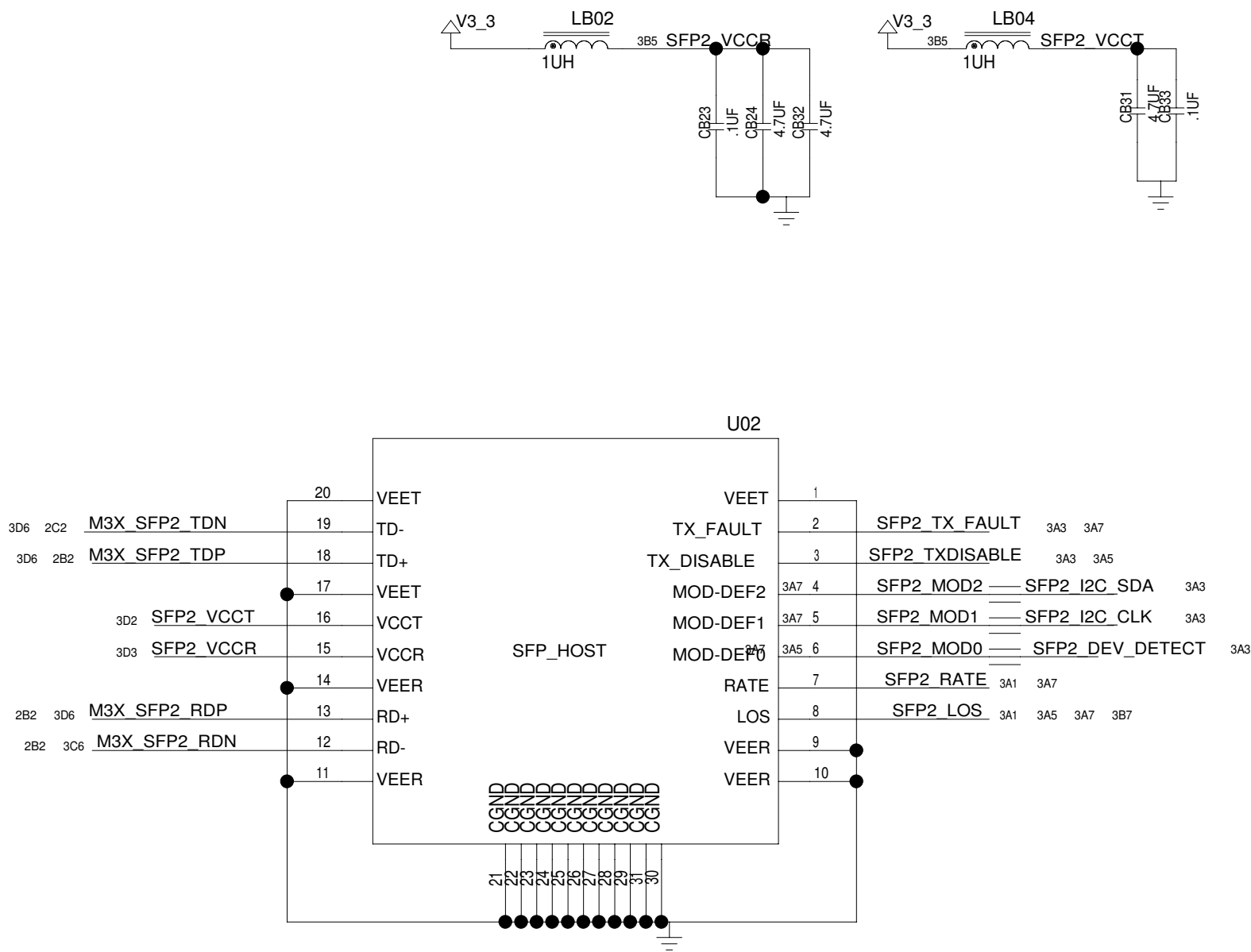
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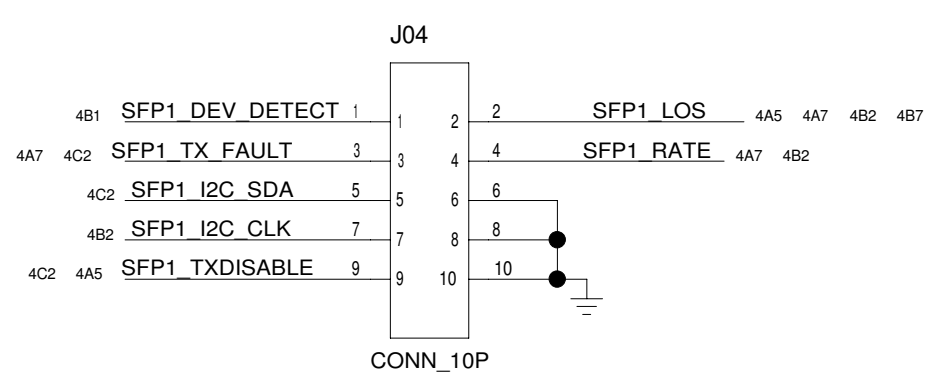
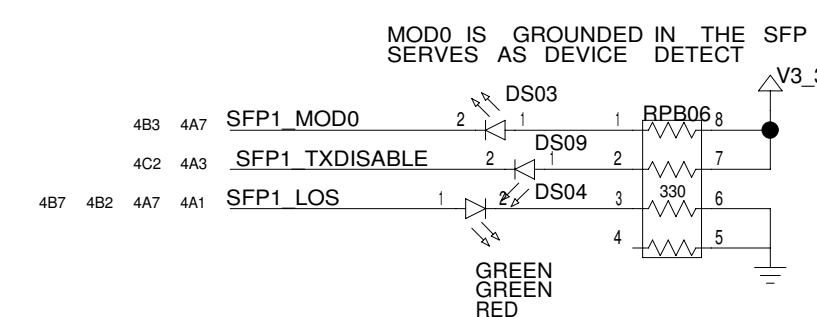
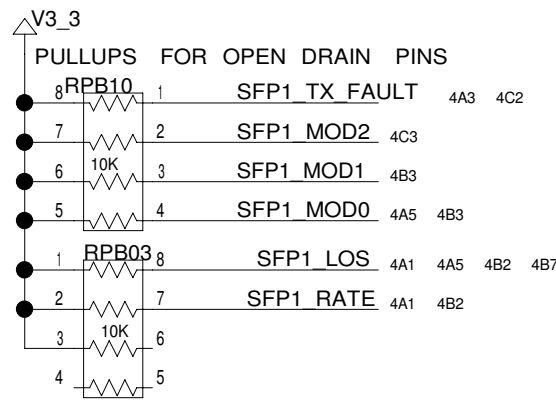
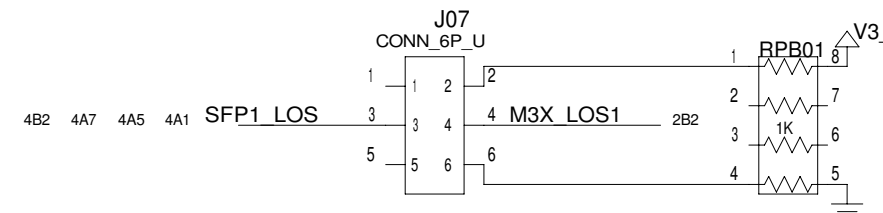
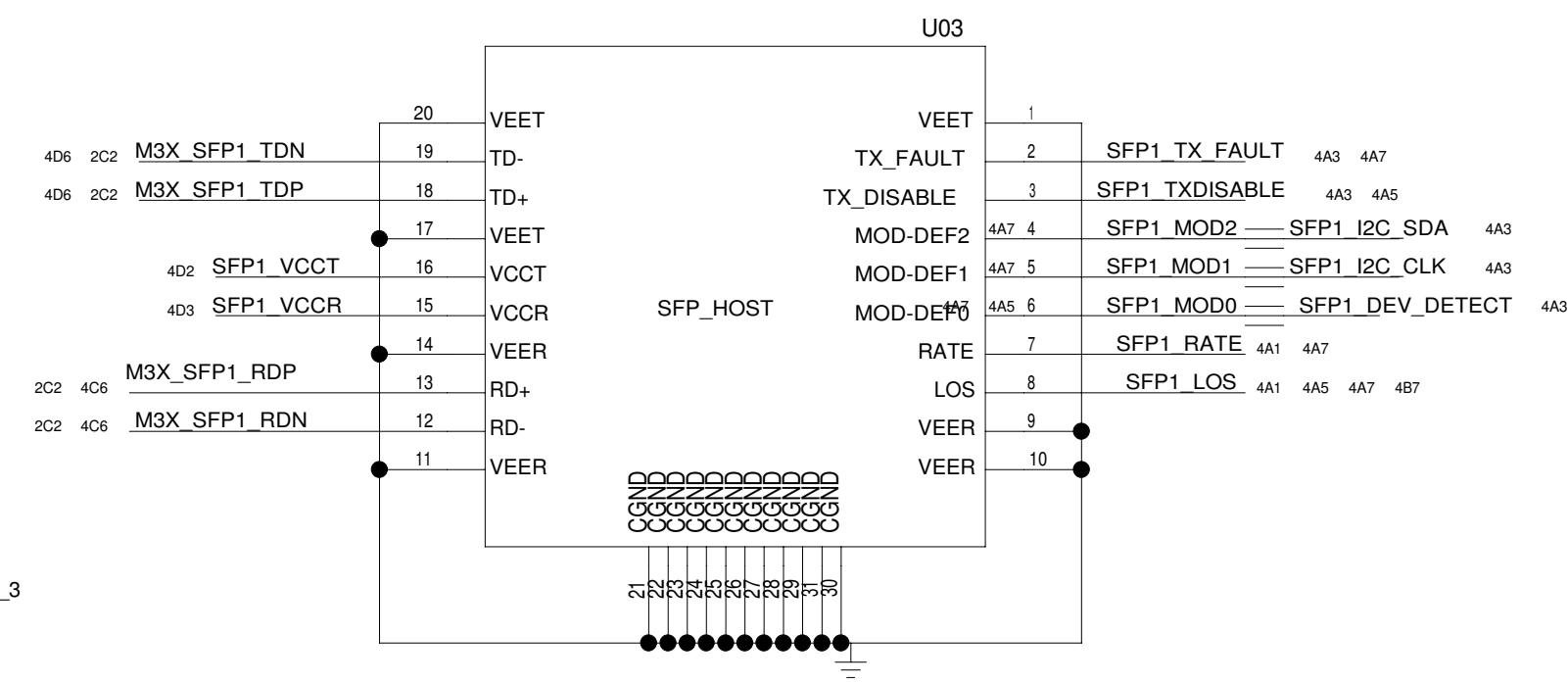
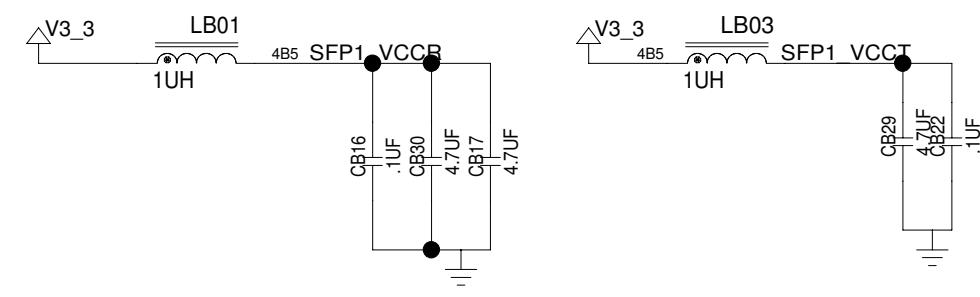
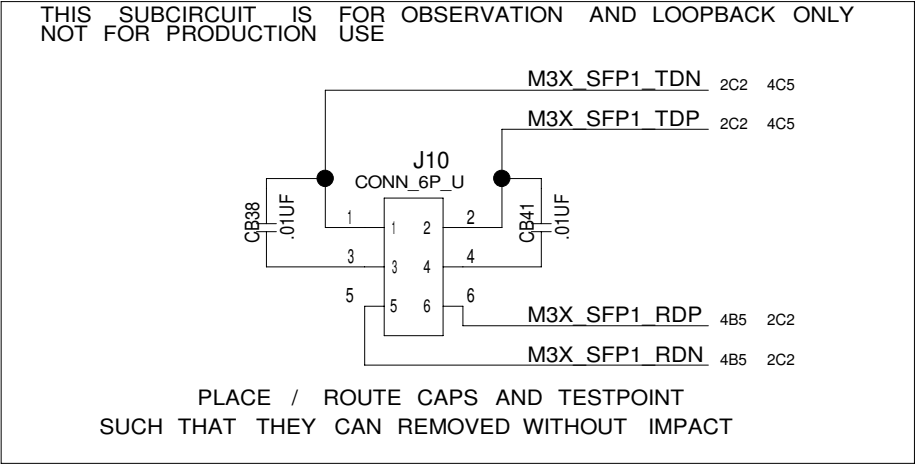
B

A



TITLE: DS33M33DK01A0		DATE:	
SERDES.		P.3-4	
ENGINEER: STEVE SCULLY		PAGE: 3/12(BLOCK) 3/26(TOTAL)	

8 7 6 5 4 3 2 1



TITLE: DS33M33DK01A0		DATE:	
SERDES.		P.3-4	
ENGINEER: STEVE SCULLY		PAGE: 4/12(BLOCK) 4/26(TOTAL)	

8 7 6 5 4 3 2 1



D

C

B

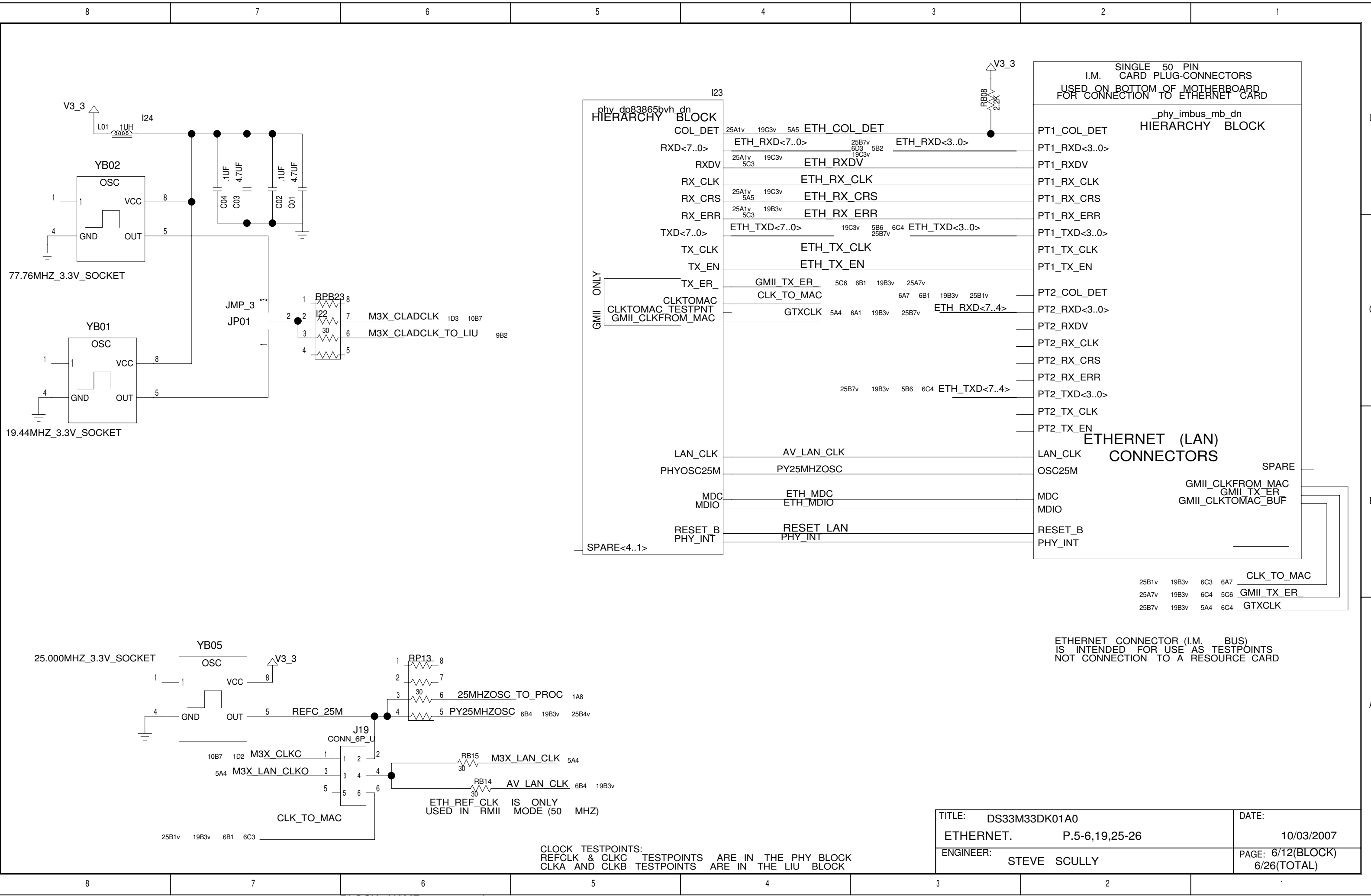
A

D

C

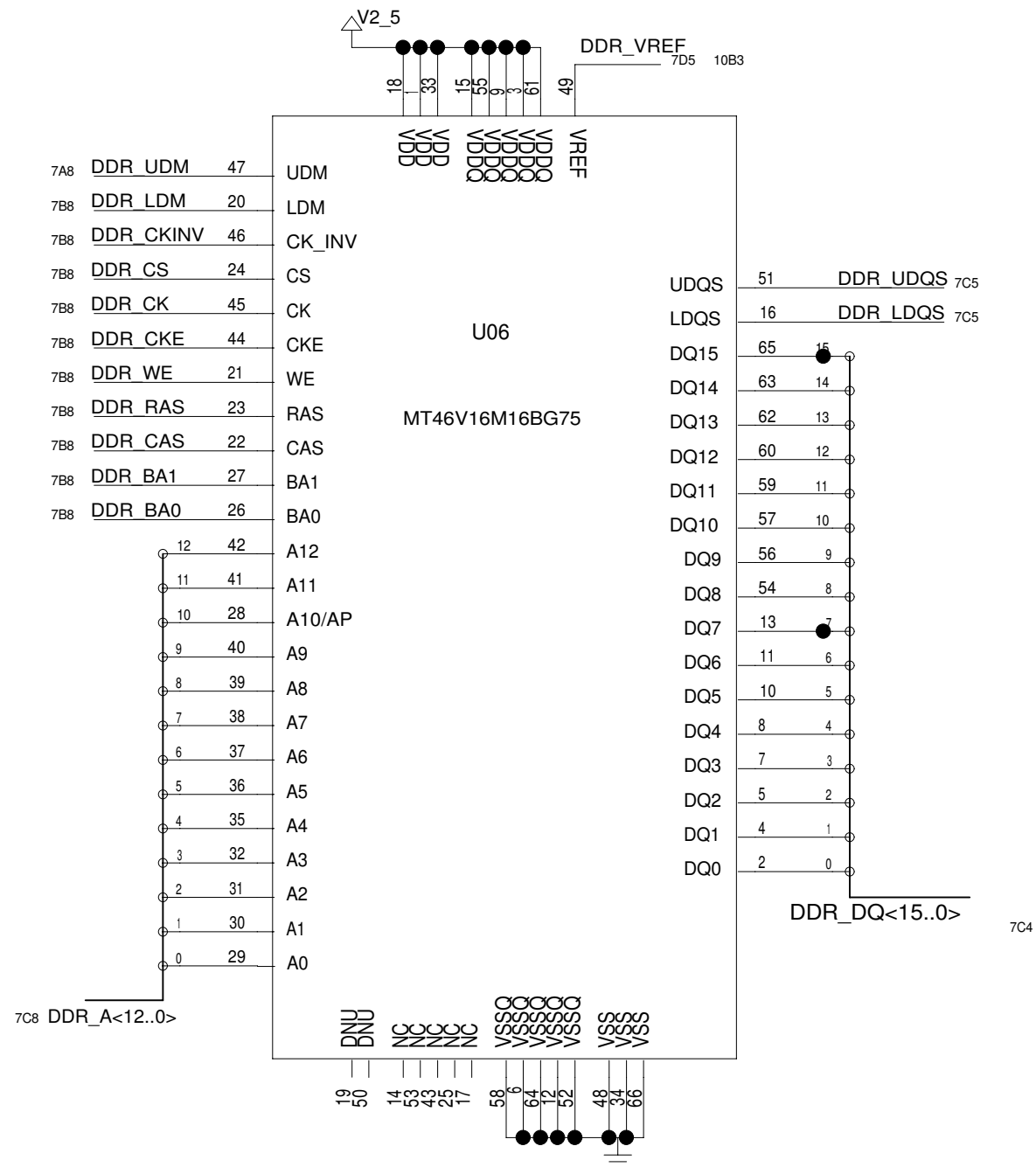
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A



CLOCK TESTPOINTS:
REFCLK & CLKC TESTPOINTS ARE IN THE PHY BLOCK
CLKA AND CLKB TESTPOINTS ARE IN THE LIU BLOCK

TITLE: DS33M33DK01A0	DATE: 10/03/2007
ETHERNET. P.5-6,19,25-26	PAGE: 6/12(BLOCK)
ENGINEER: STEVE SCULLY	6/26(TOTAL)



TITLE: DS33M33DK01A0 DDR MEMORY. P.7	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 7/12(BLOCK) 7/26(TOTAL)

D

D

C

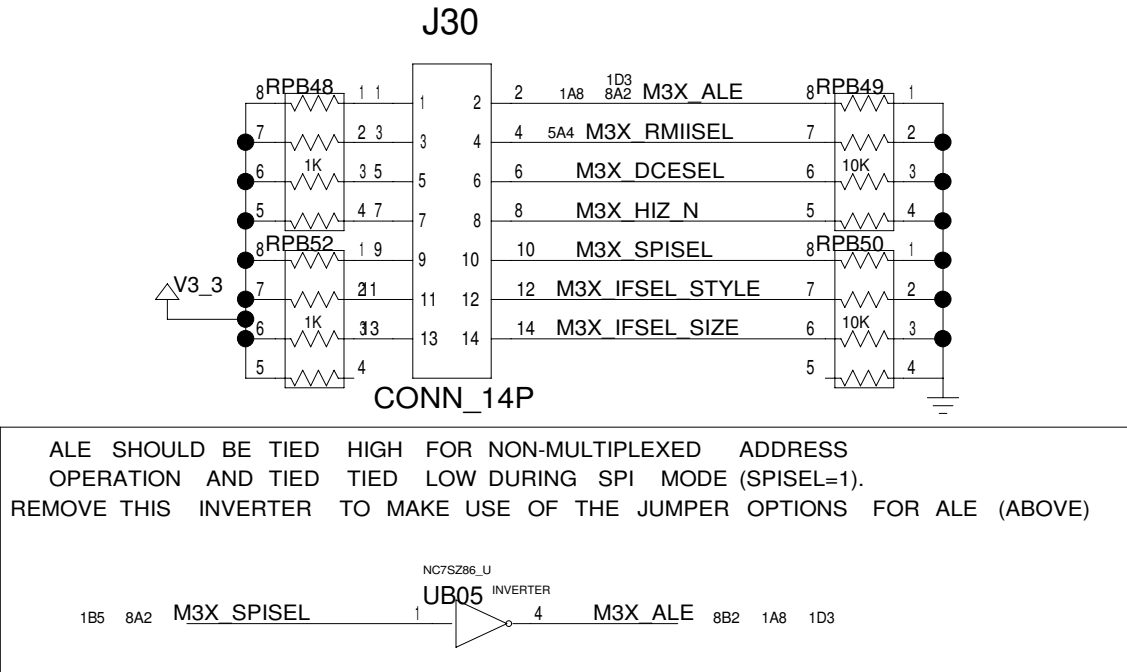
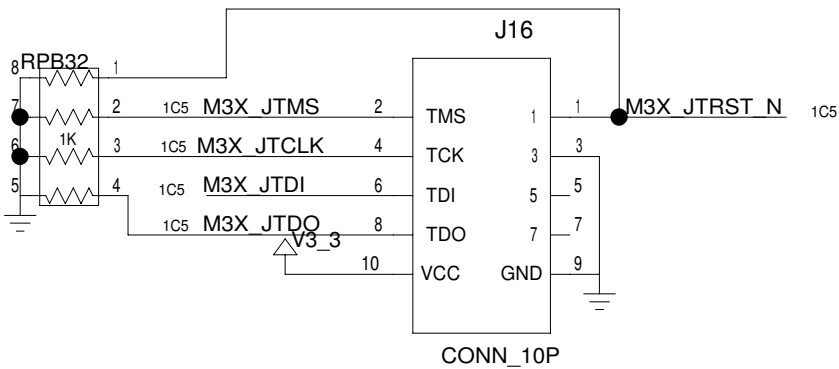
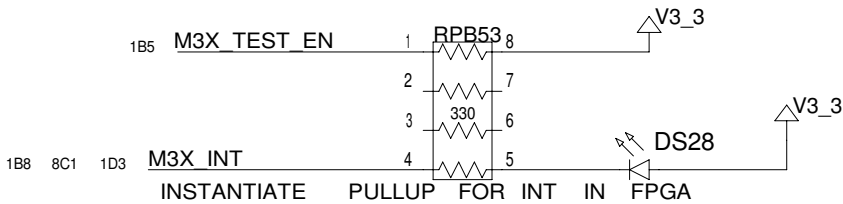
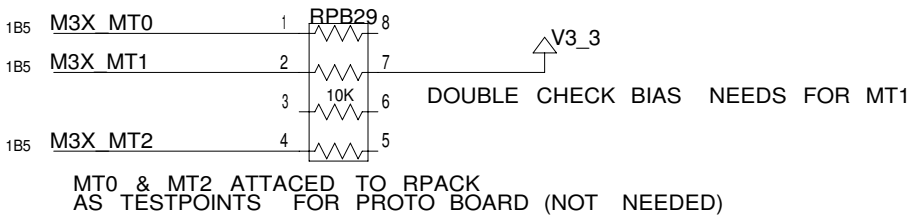
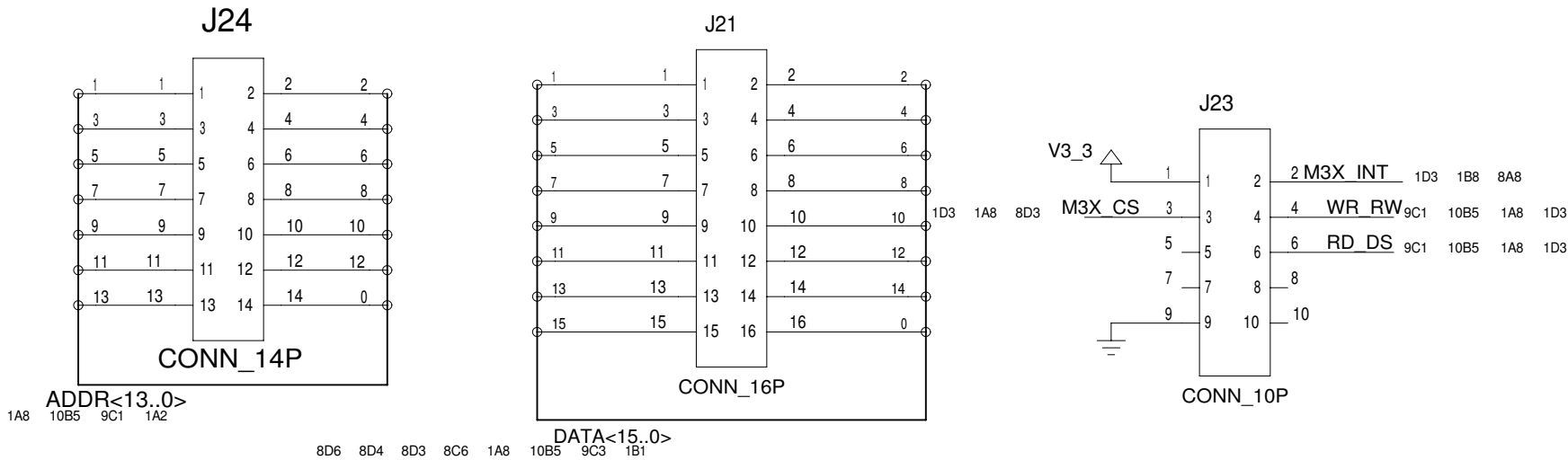
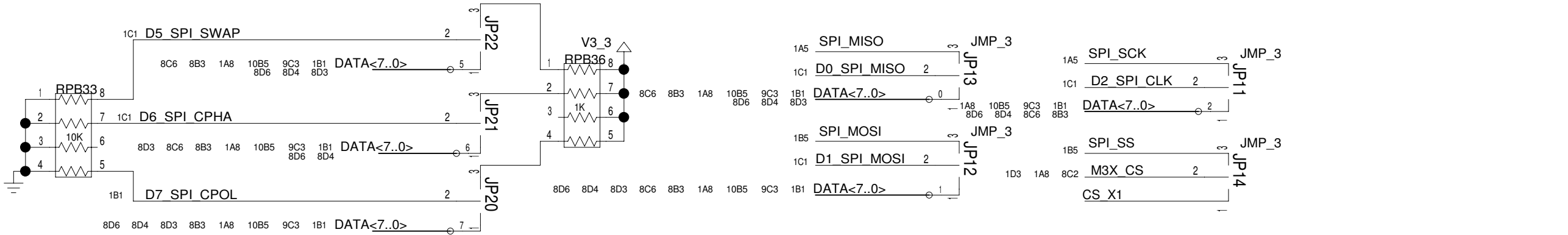
C

B

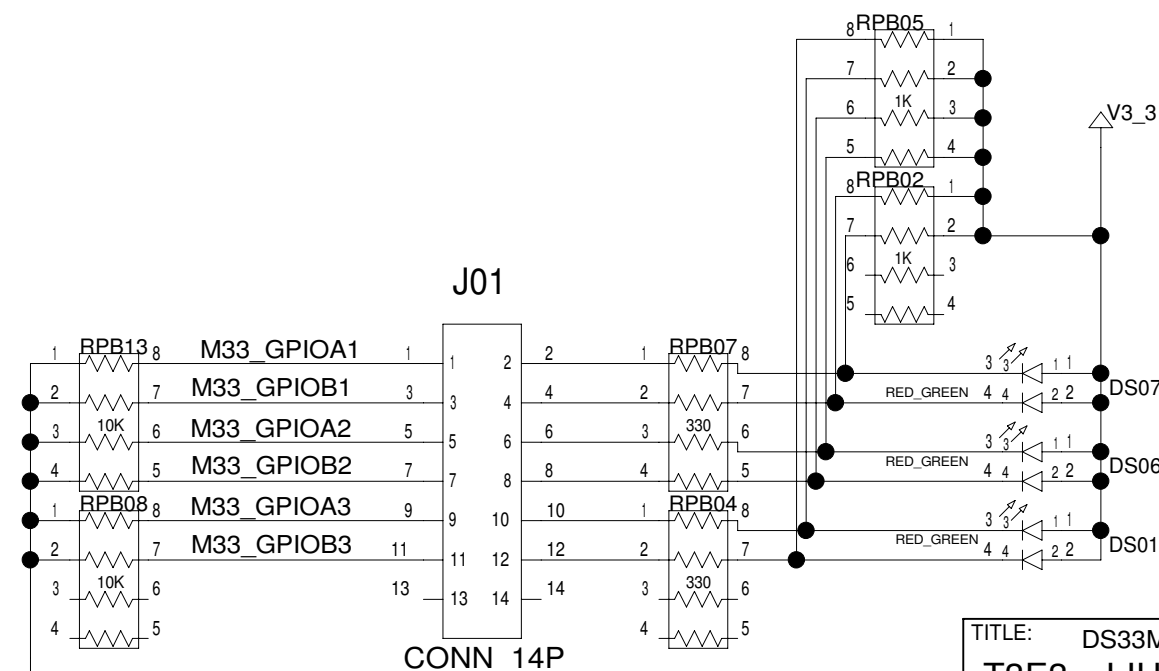
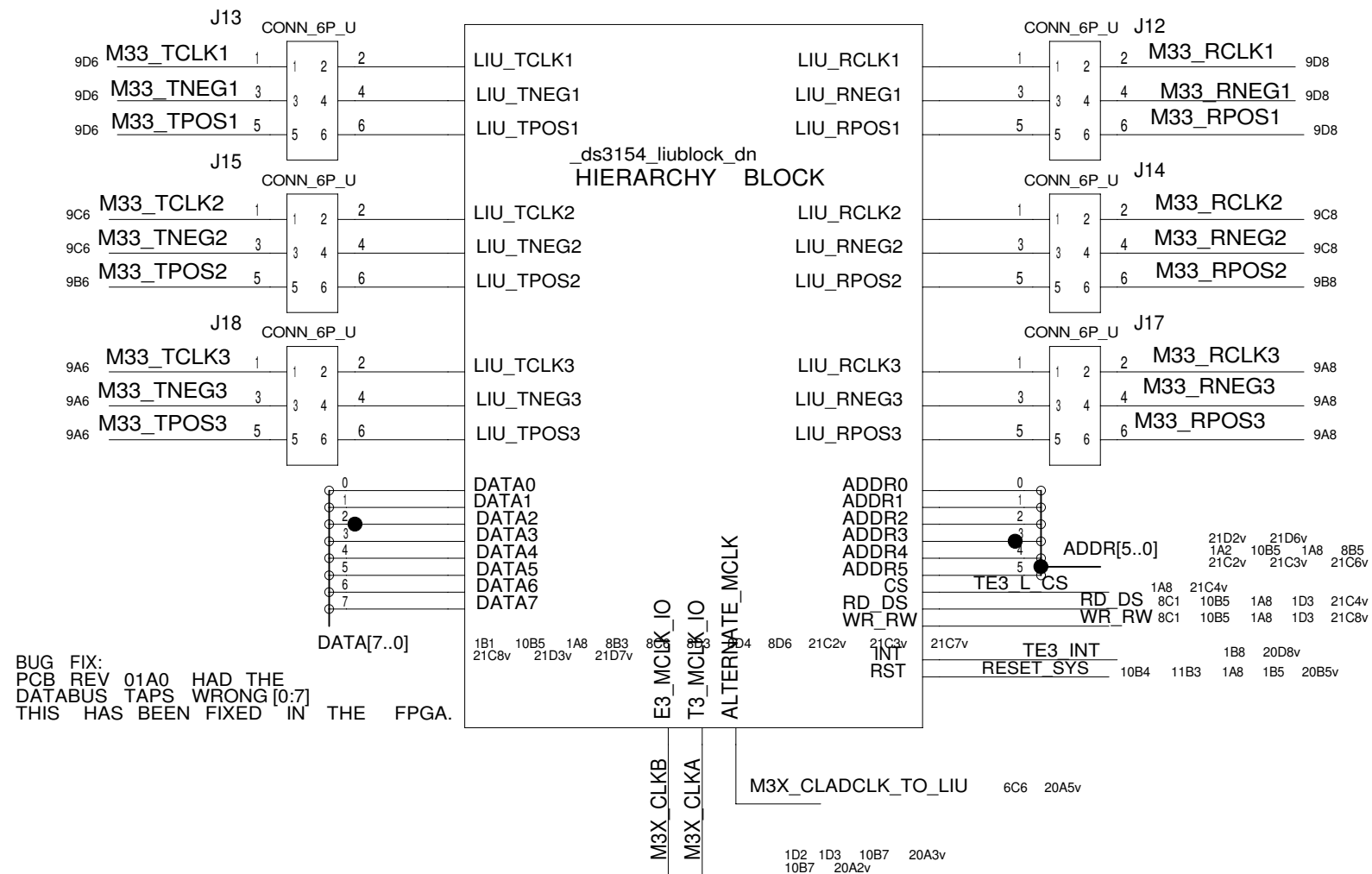
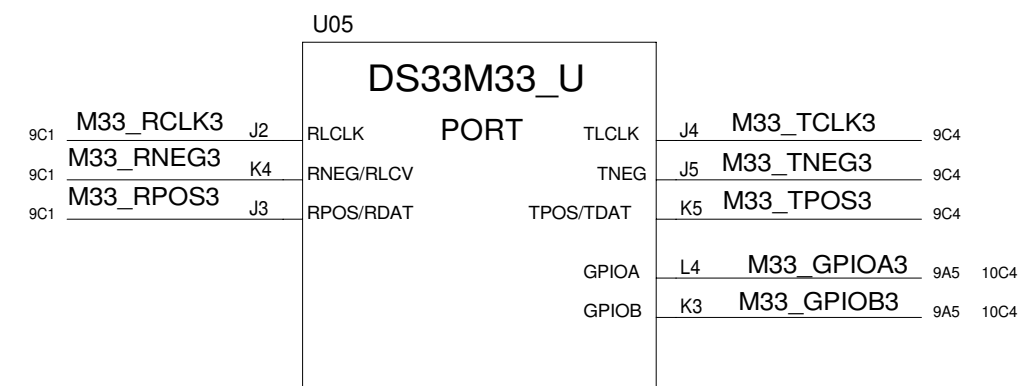
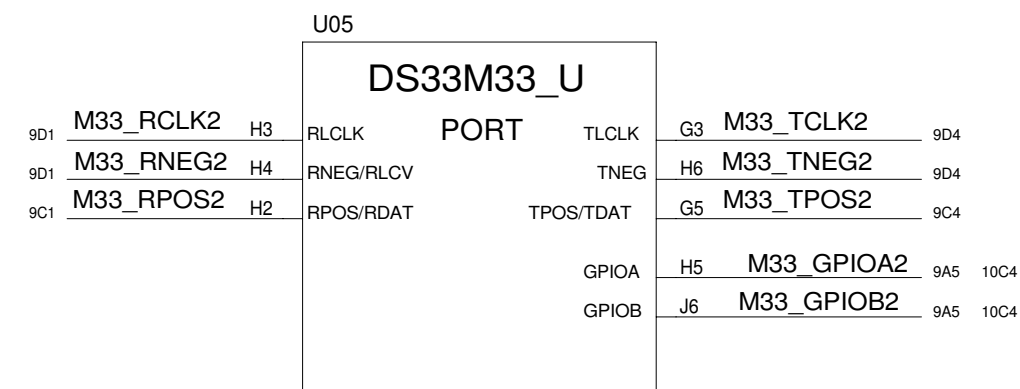
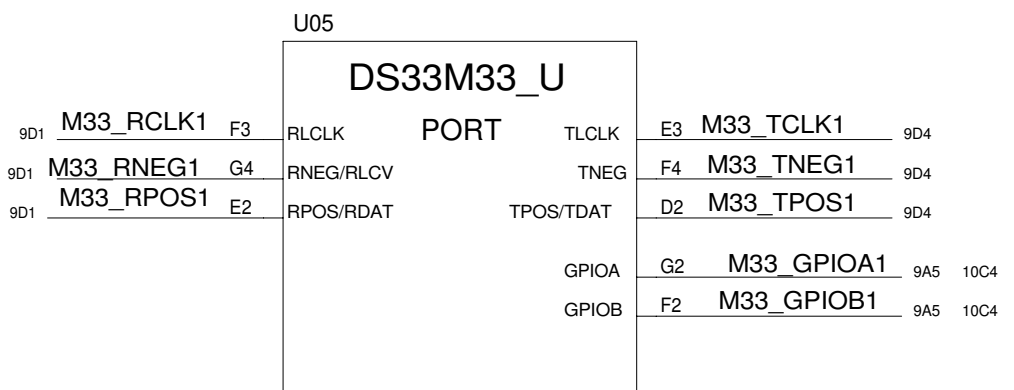
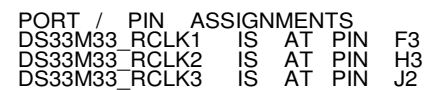
B

A

A



TITLE: DS33M33DK01A0 BIAS+CONFIG. P.8	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 8/12(BLOCK) 8/26(TOTAL)



TITLE: DS33M30M31M33EE01A0 T3E3 LIU I/F. P.2,9,20-22	DATE: 04/15/2007
ENGINEER: STEVE SCULLY	PAGE: 9/12(BLOCK) 9/26(TOTAL)

8

7

6

5

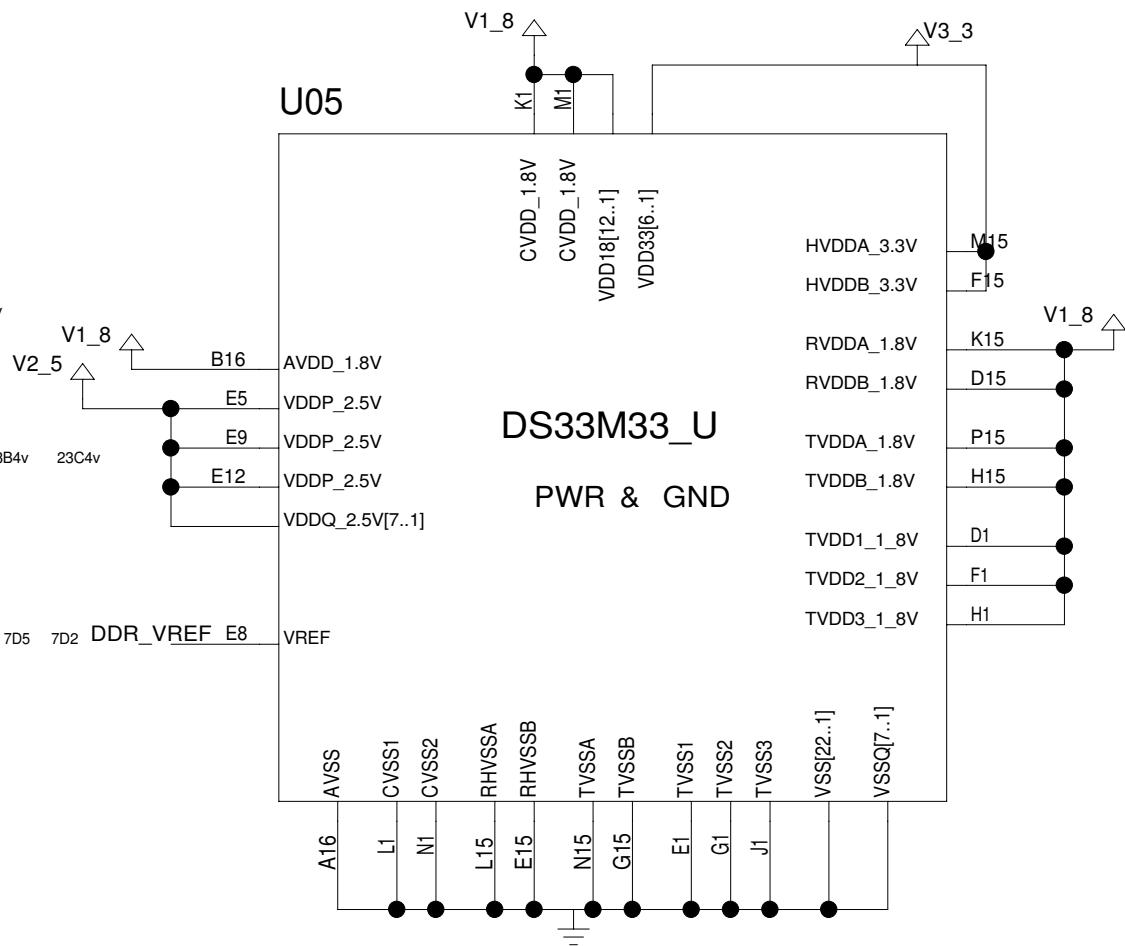
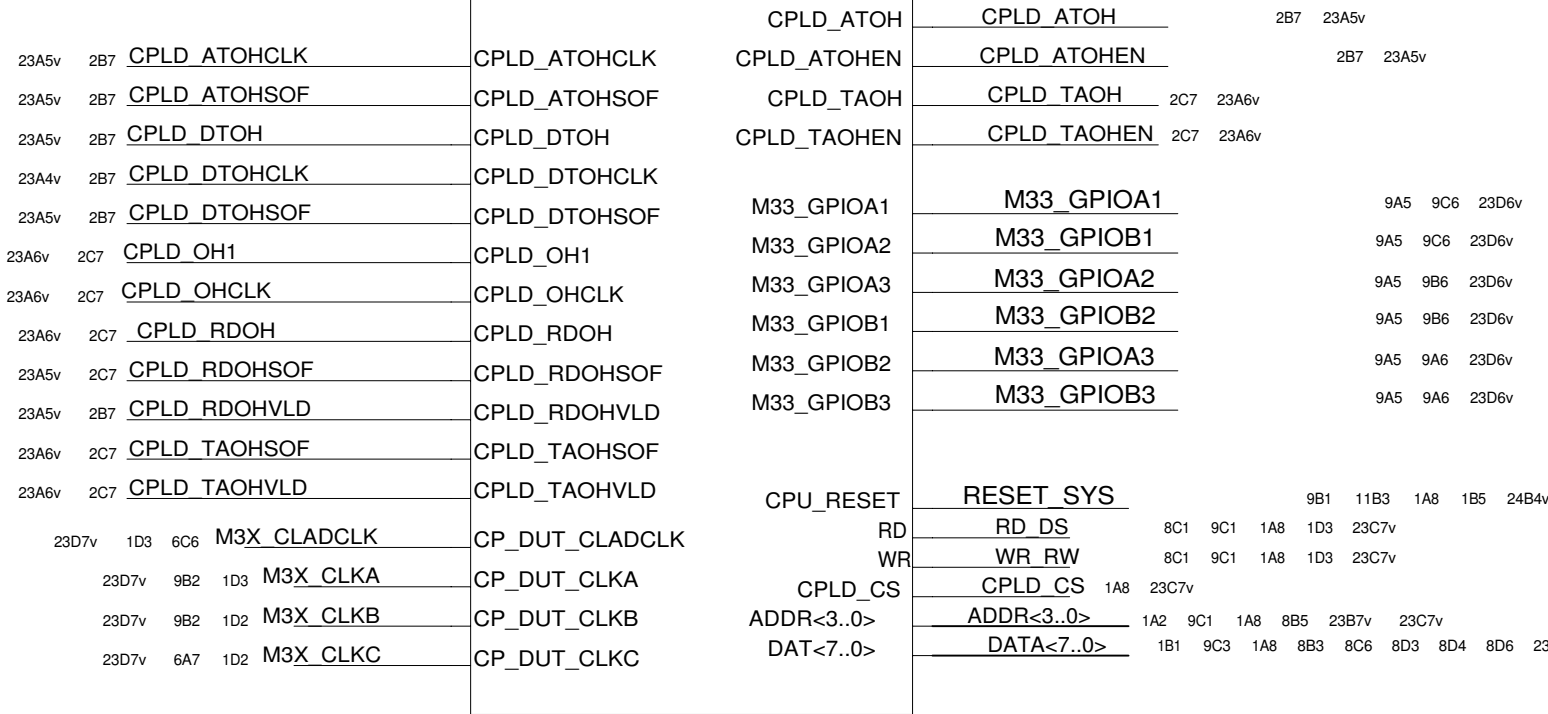
4

3

2

1

overheadcpld_dn
HIERARCHY BLOCK



TITLE: DS33M33DK01A0	DATE:
OVERHEAD. P.2,10,23-24	10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 10/12(BLOCK)
	10/26(TOTAL)

8

7

6

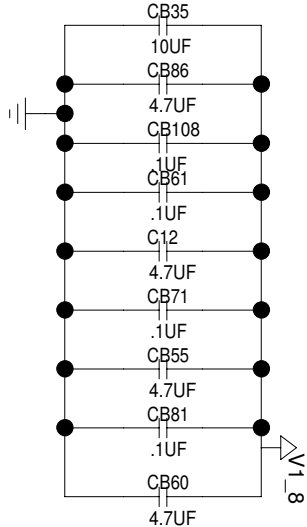
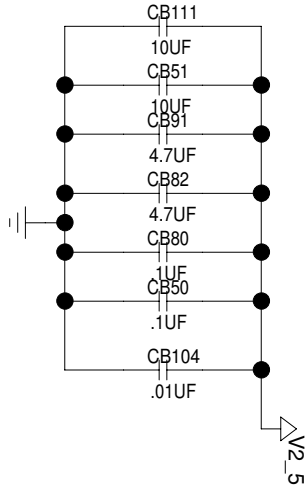
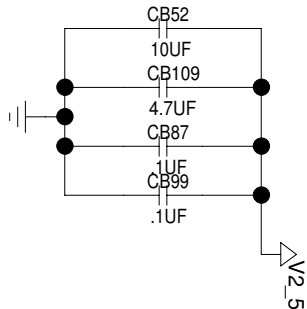
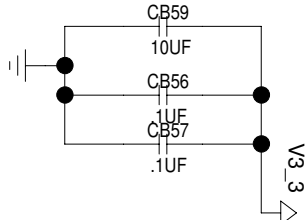
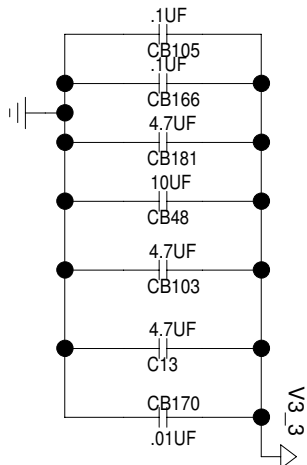
5

4

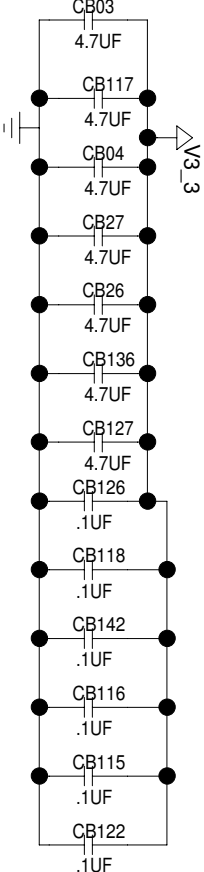
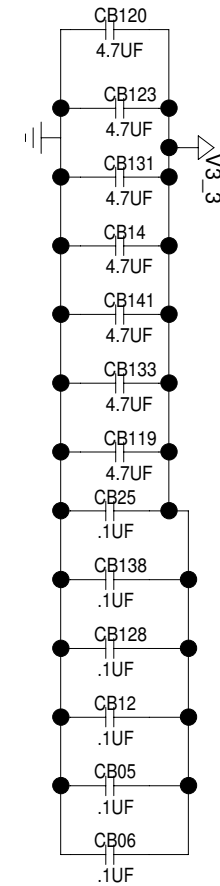
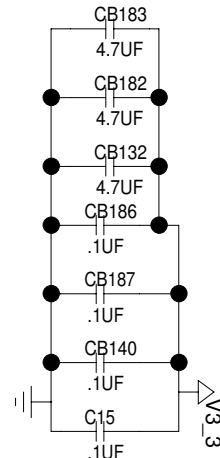
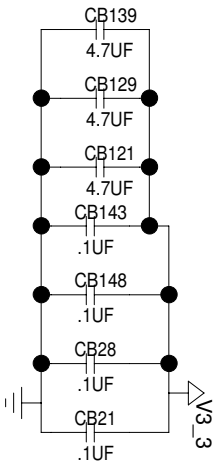
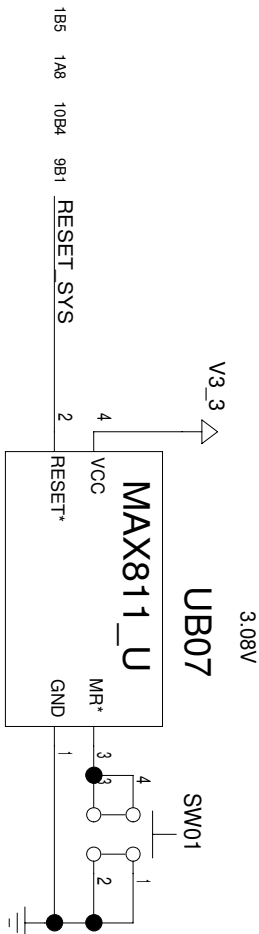
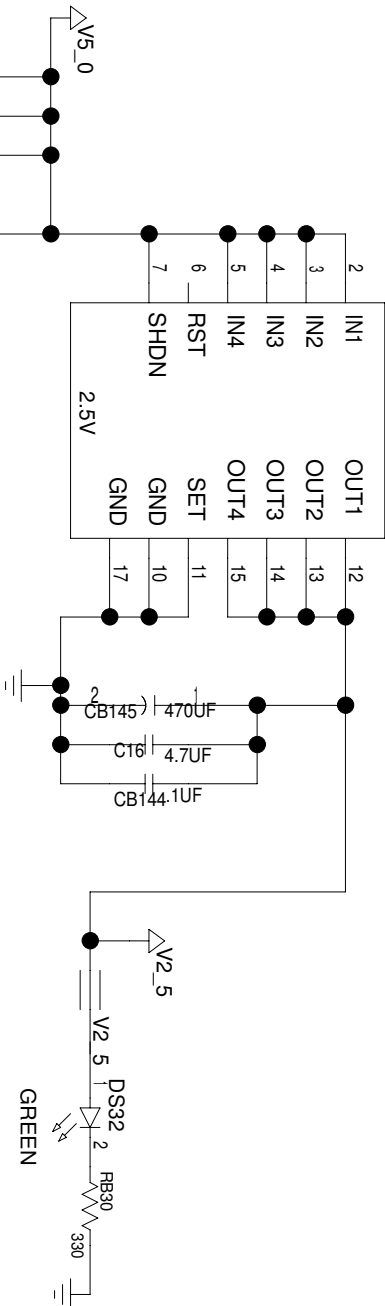
3

2

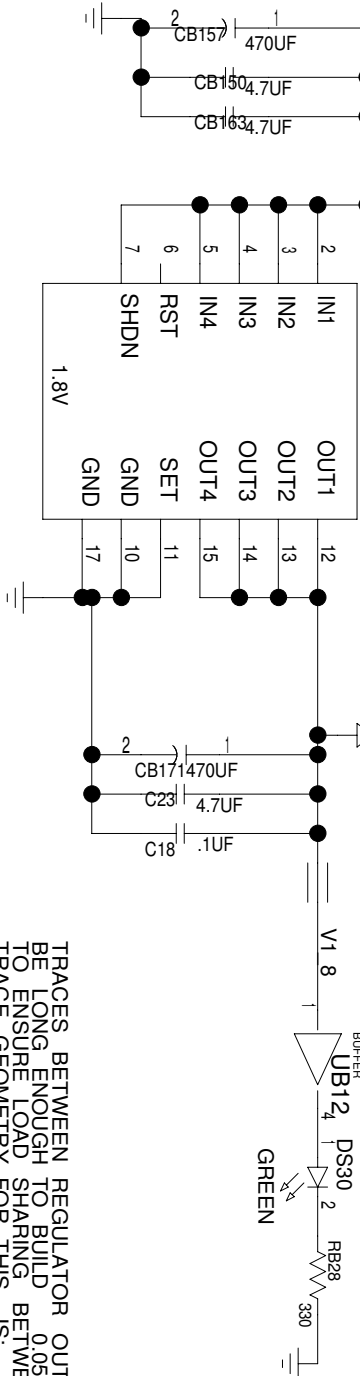
1



UB08
MAX1793_U



UB09
MAX1793_U



TRACES BETWEEN REGULATOR OUTPUT AND V2_5 SHOULD BE LONG ENOUGH TO BUILD 0.05 OHM OF RESISTANCE TO ENSURE LOAD SHARING BETWEEN THE 2.5V 1% REGULATORS TRACE GEOMETRY FOR THIS IS: 1 INCH LONG, 10 MIL WIDE, 1 OZ COPPER

TITLE: DS33M33DK01A0		DATE: 10/03/2007
POWER. P.11-12		
ENGINEER: STEVE SCULLY	PAGE: 11/12(BLOCK) 11/26(TOTAL)	

D

D

C

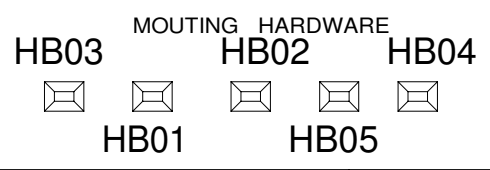
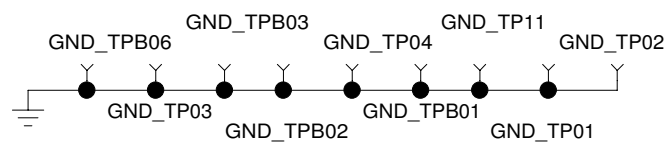
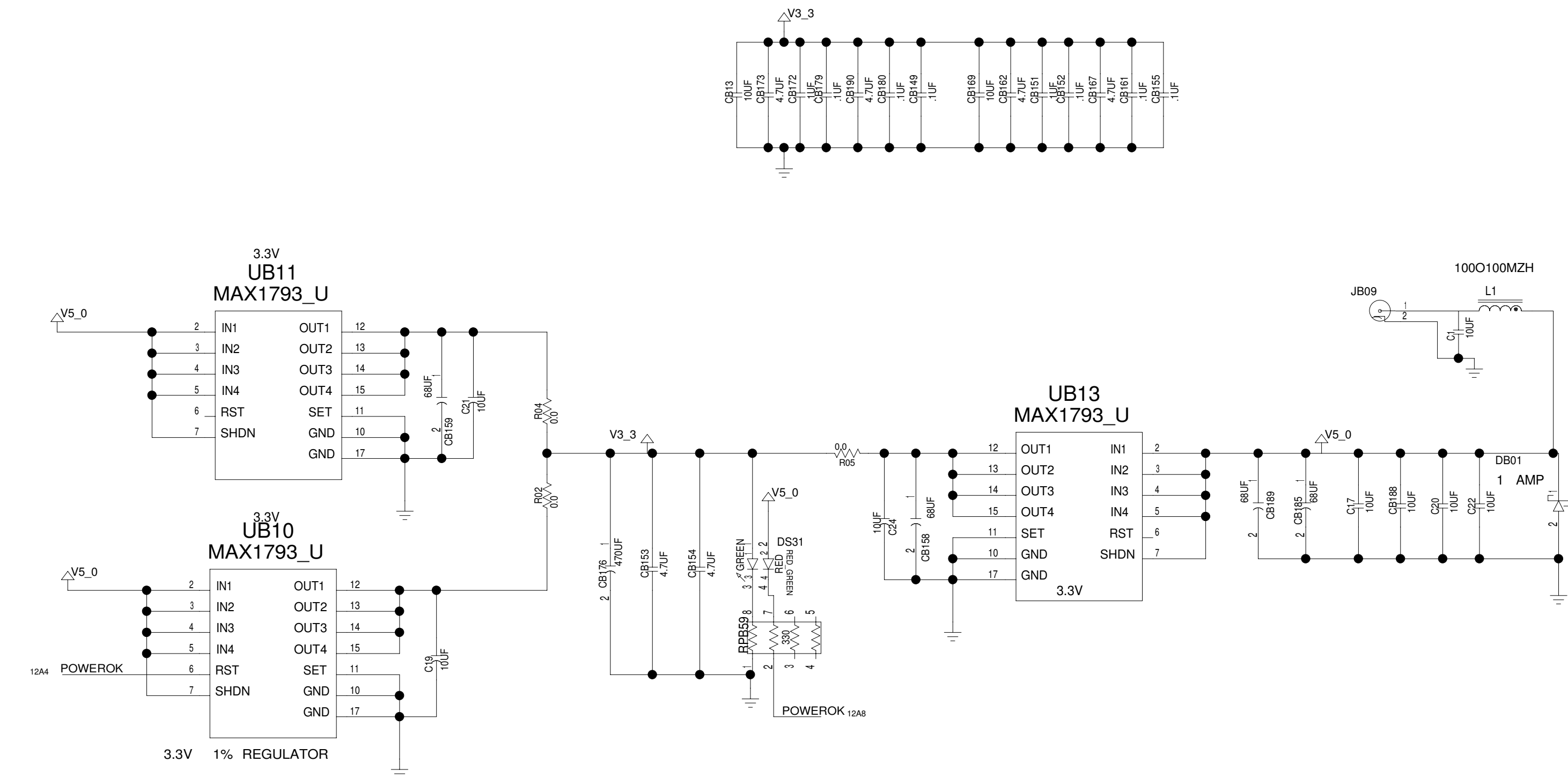
C

B

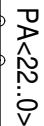
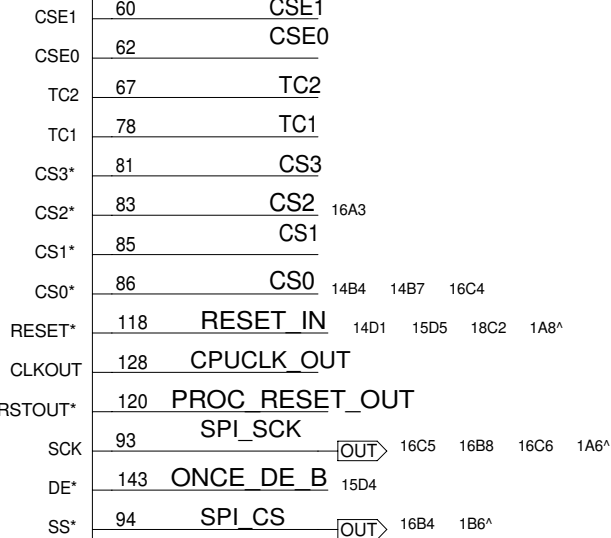
B

A

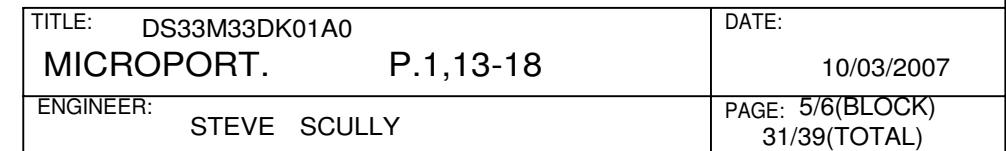
A

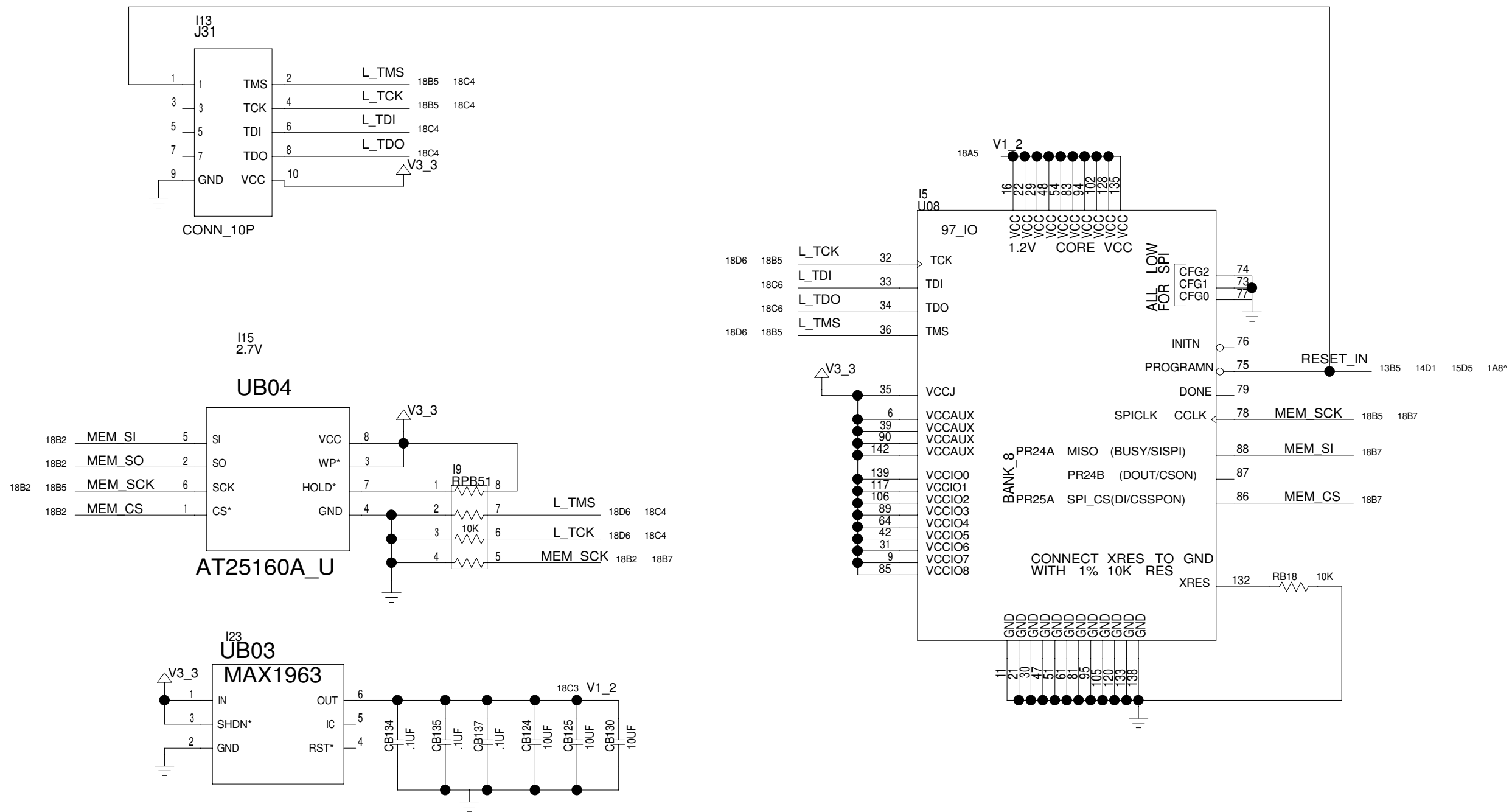


TITLE: DS33M33DK01A0 POWER. P.11-12		DATE: 10/03/2007
ENGINEER: STEVE SCULLY		PAGE: 12/12(BLOCK) 12/26(TOTAL)



TITLE: DS33M33DK01A0 MICROPORT. P.1,13-18	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 1/6(BLOCK) 13/26(TOTAL)

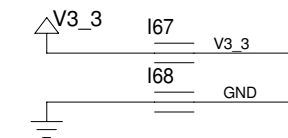




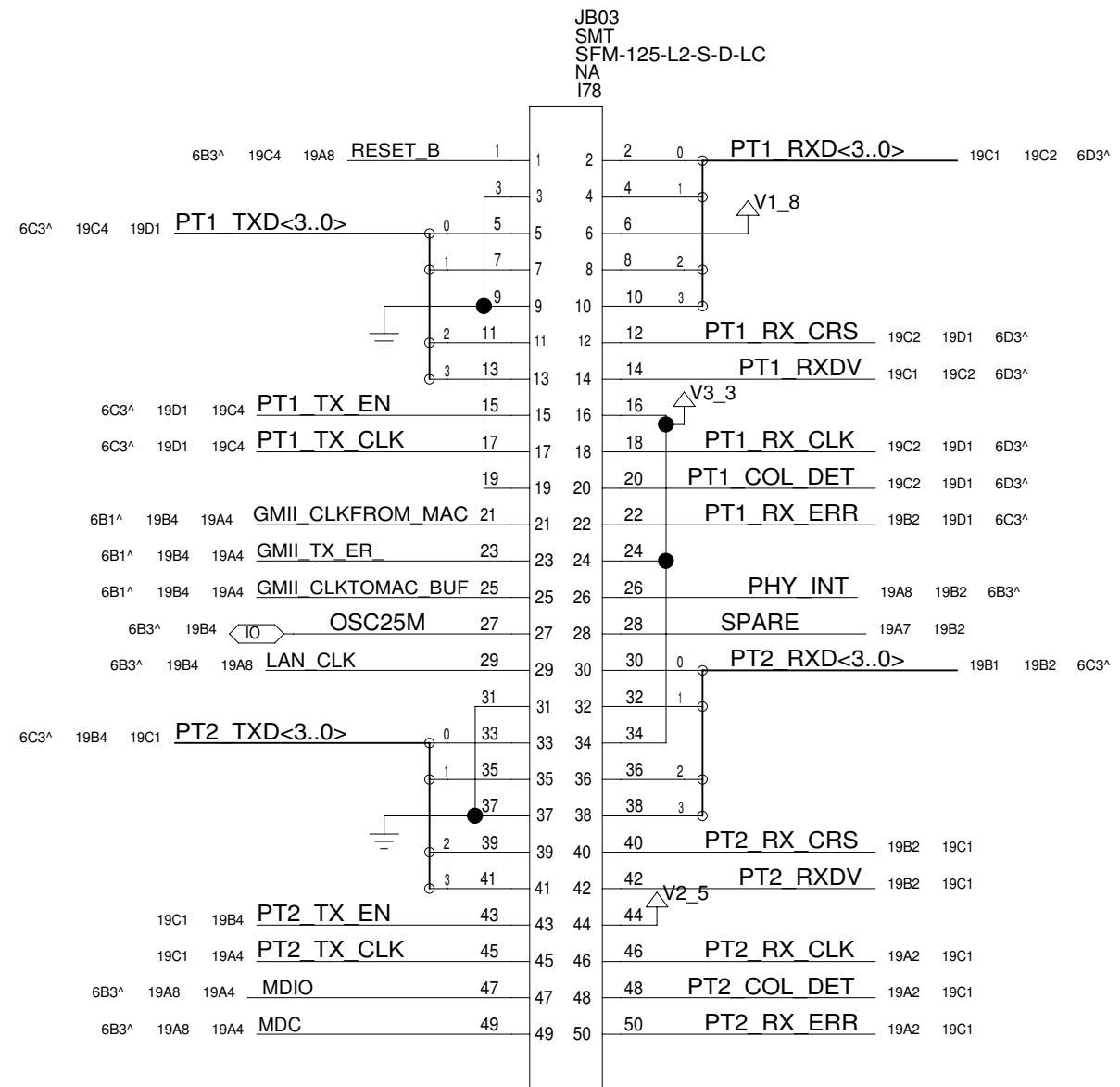
TITLE: DS33M33DK01A0
MICROPORT. P.1,13-18
ENGINEER: STEVE SCULLY

DATE: 10/03/2007
PAGE: 3/5(BLOCK)
31/39(TOTAL)

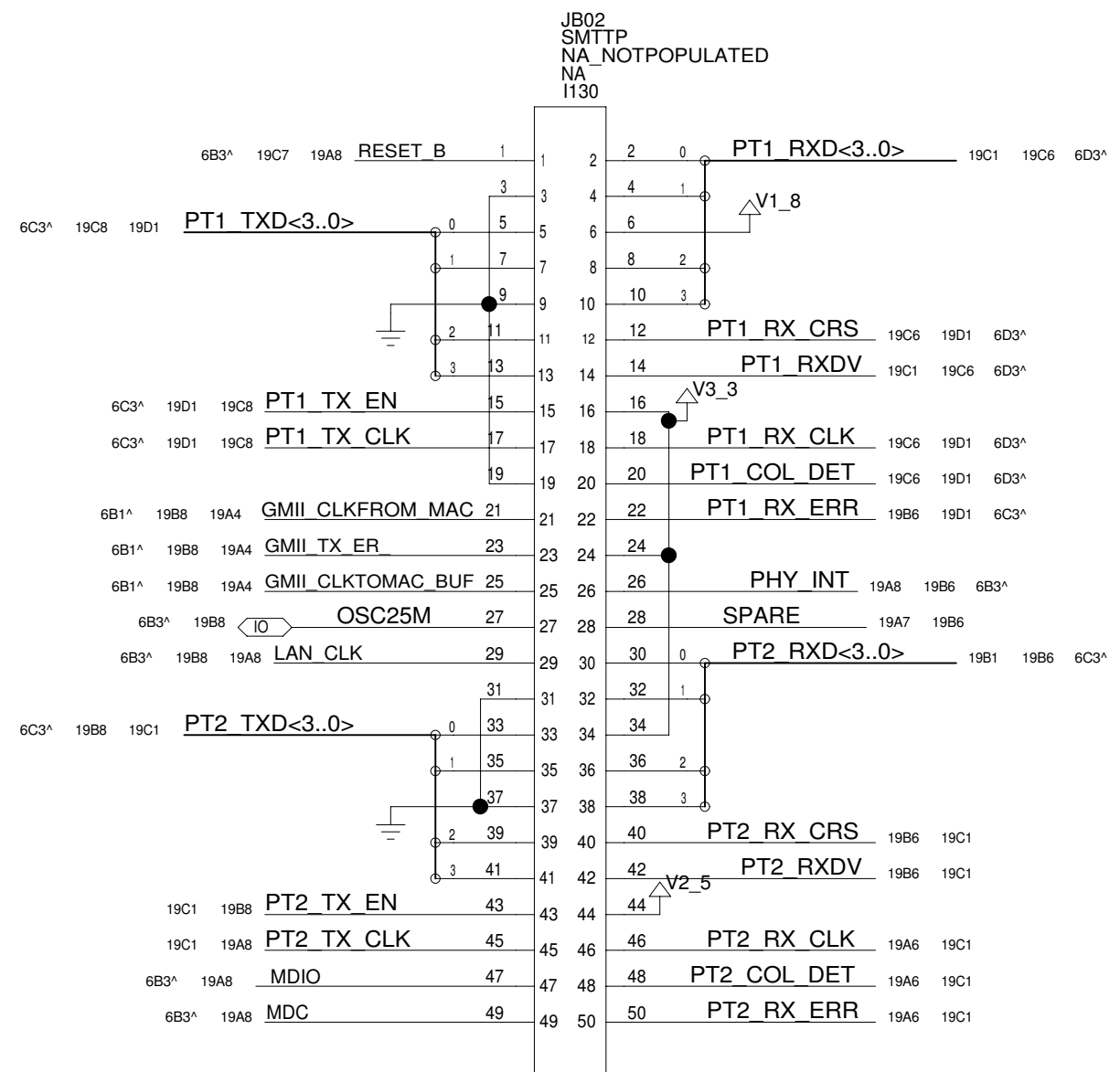
D



C



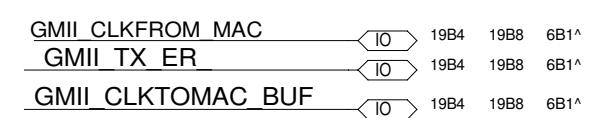
B



A

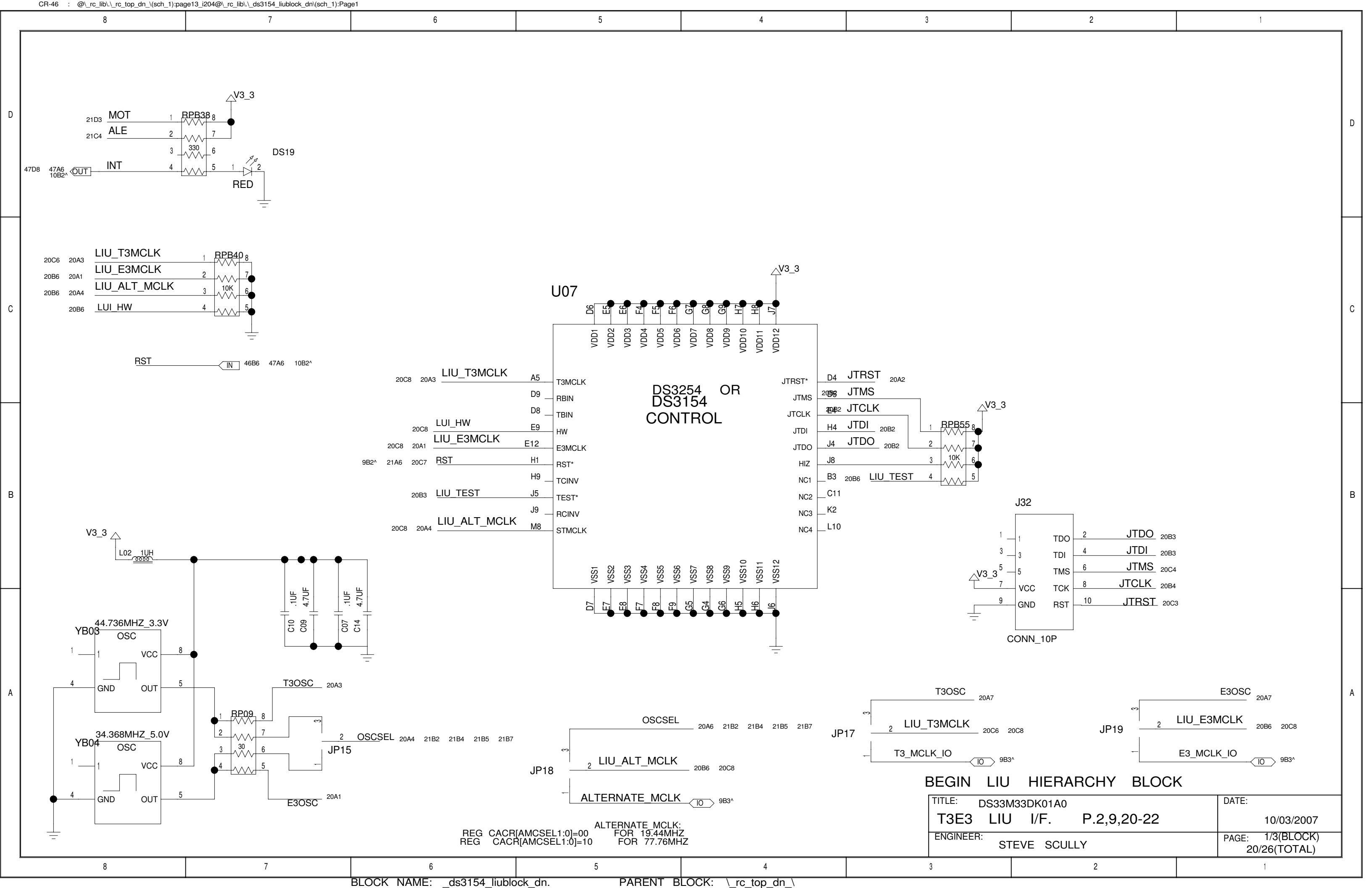


CONNECTORS FOR LAN MOTHERBOARD TO RESOURCE CARD



BEGIN/END PHY CONNECTOR HIERARCHY BLOCK

TITLE: DS33M33DK01A0	DATE: 10/03/2007
ETHERNET. P.5-6,19,25-26	PAGE: 1/1(BLOCK)
ENGINEER: STEVE SCULLY	19/26(TOTAL)



REG CACR[AMCSEL1:0]=00 ALTERNATE MCLK:
REG CACR[AMCSEL1:0]=10 FOR 19.44MHZ
FOR 77.76MHZ

BEGIN LIU HIERARCHY BLOCK

TITLE: DS33M33DK01A0	DATE: 10/03/2007
T3E3 LIU I/F. P.2,9,20-22	PAGE: 1/3(BLOCK)
ENGINEER: STEVE SCULLY	20/26(TOTAL)

D

C

B

A

PORT LOCATIONS
RLOS1 IS AT PIN A1
RLOS2 IS AT PIN M12
RLOS3 IS AT PIN A12

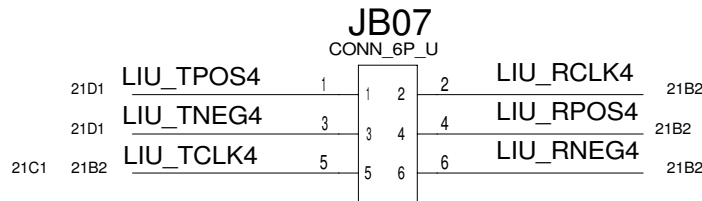
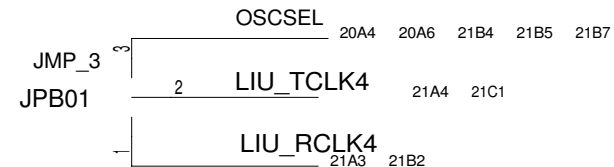
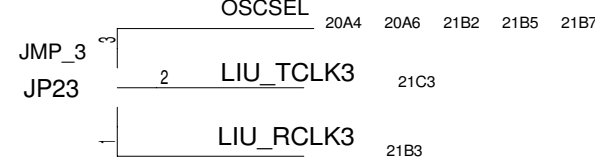
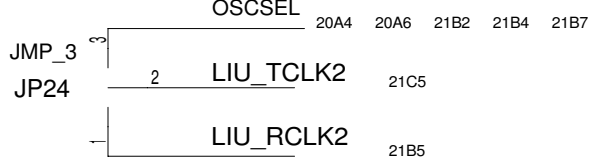
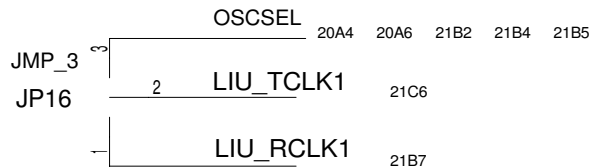
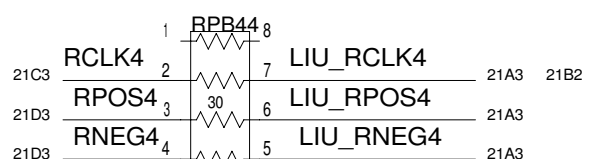
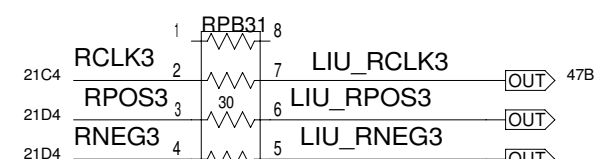
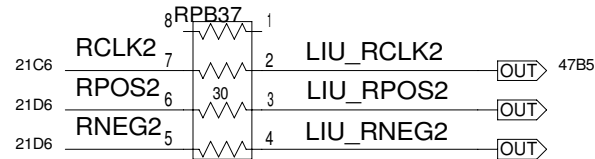
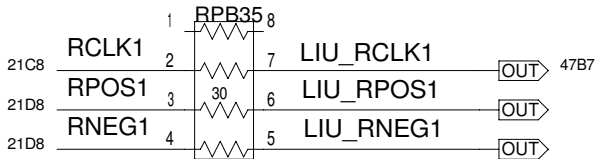
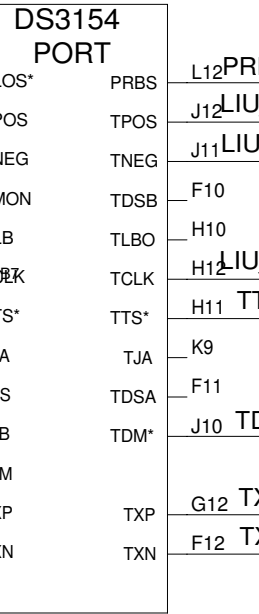
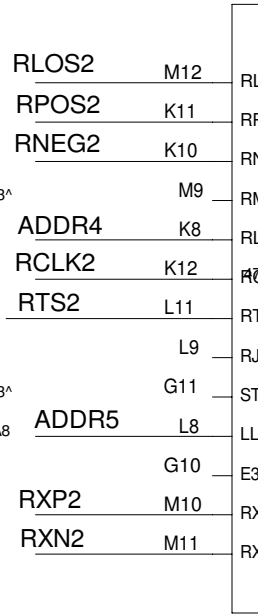
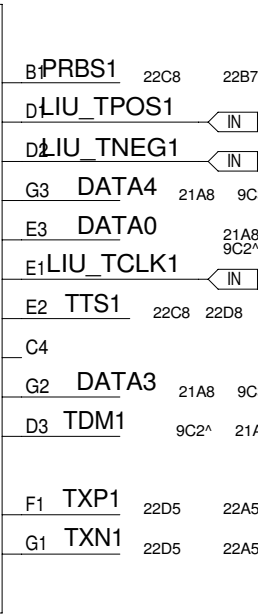
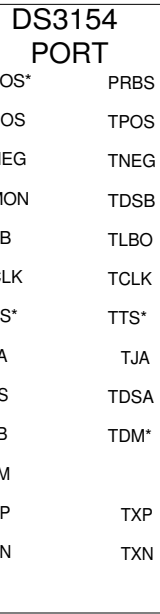
PORT 4 OF DS3254 IS NOT USED WITH DS33M33
IT IS A SPARE PORT IN THIS DESIGN
DS3253 IS RECOMMENDED FOR DS33M33

U07 DS3254 OR

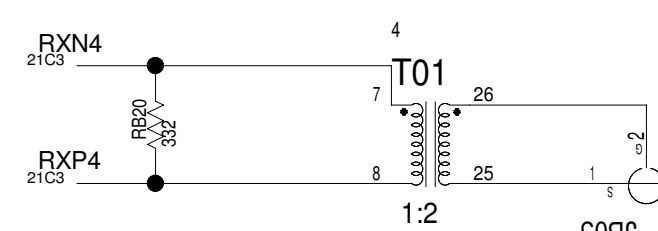
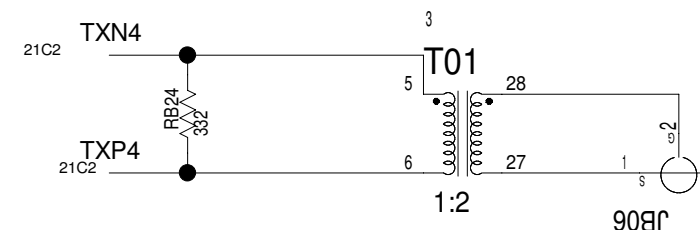
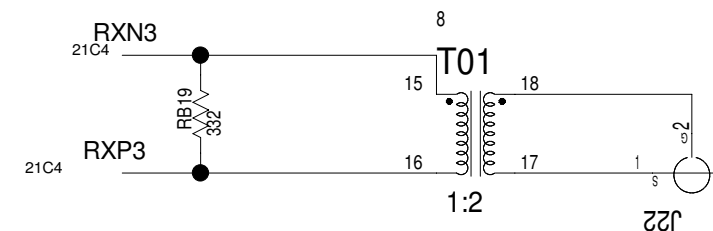
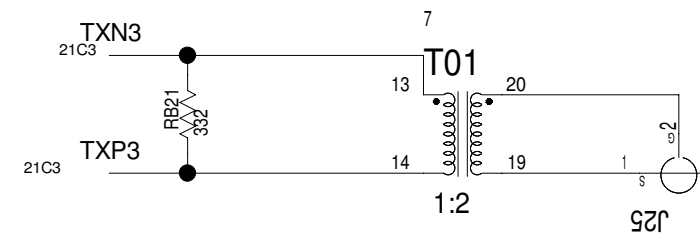
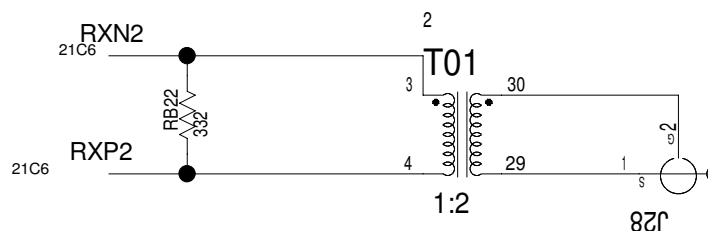
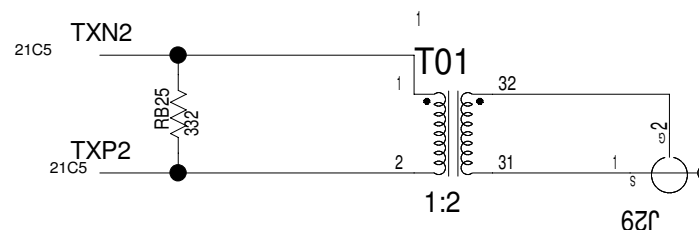
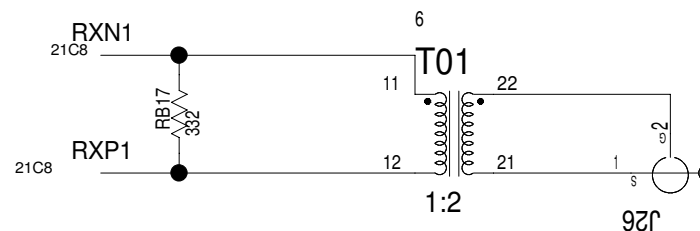
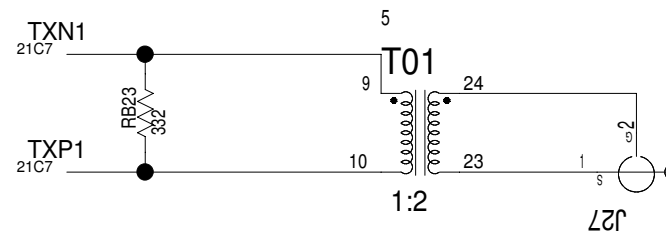
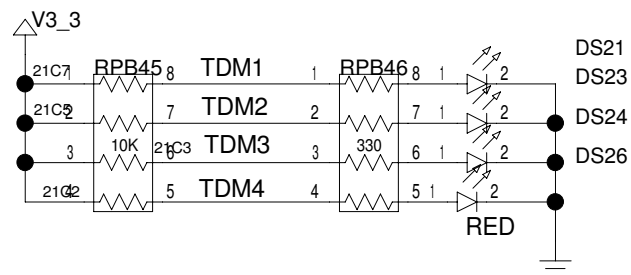
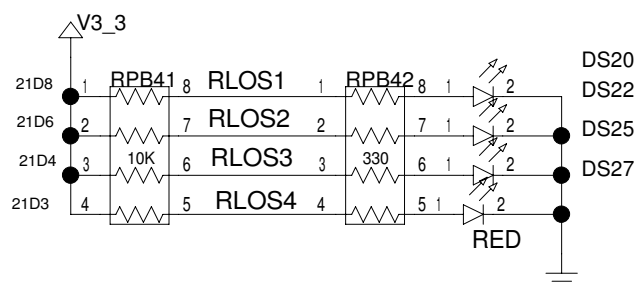
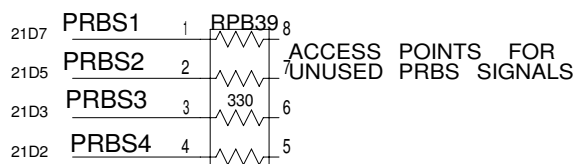
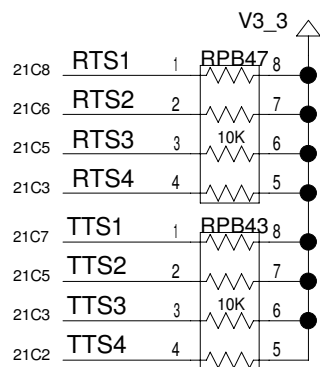
U07 DS3254 OR

U07 DS3254 OR

U07 DS3254 OR

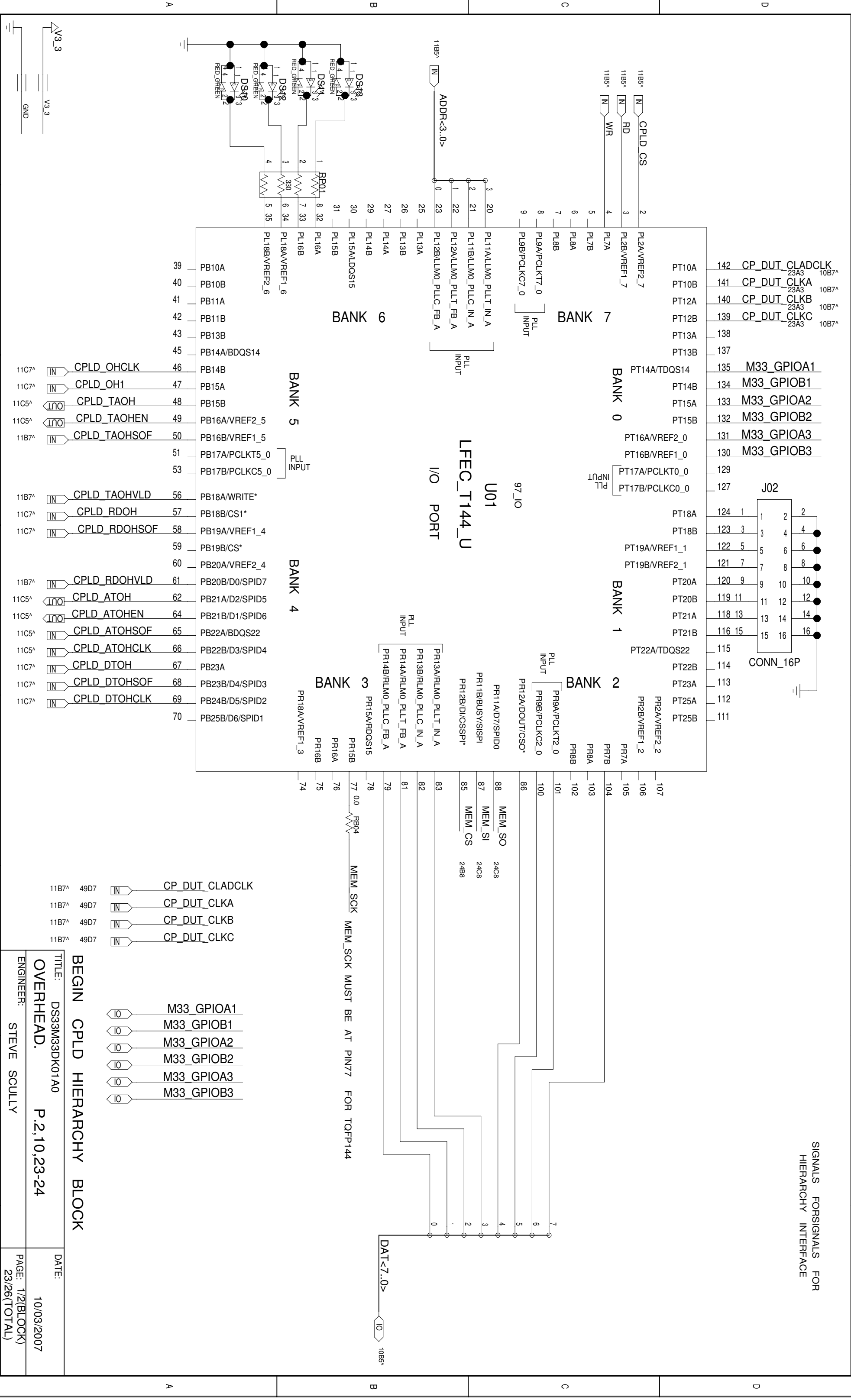


TITLE: DS33M33DK01A0		DATE: 10/03/2007	
T3E3 LIU I/F. P.2,9,20-22		PAGE: 2/3(BLOCK)	
ENGINEER: STEVE SCULLY		21/26(TOTAL)	



END LIU HIERARCHY BLOCK

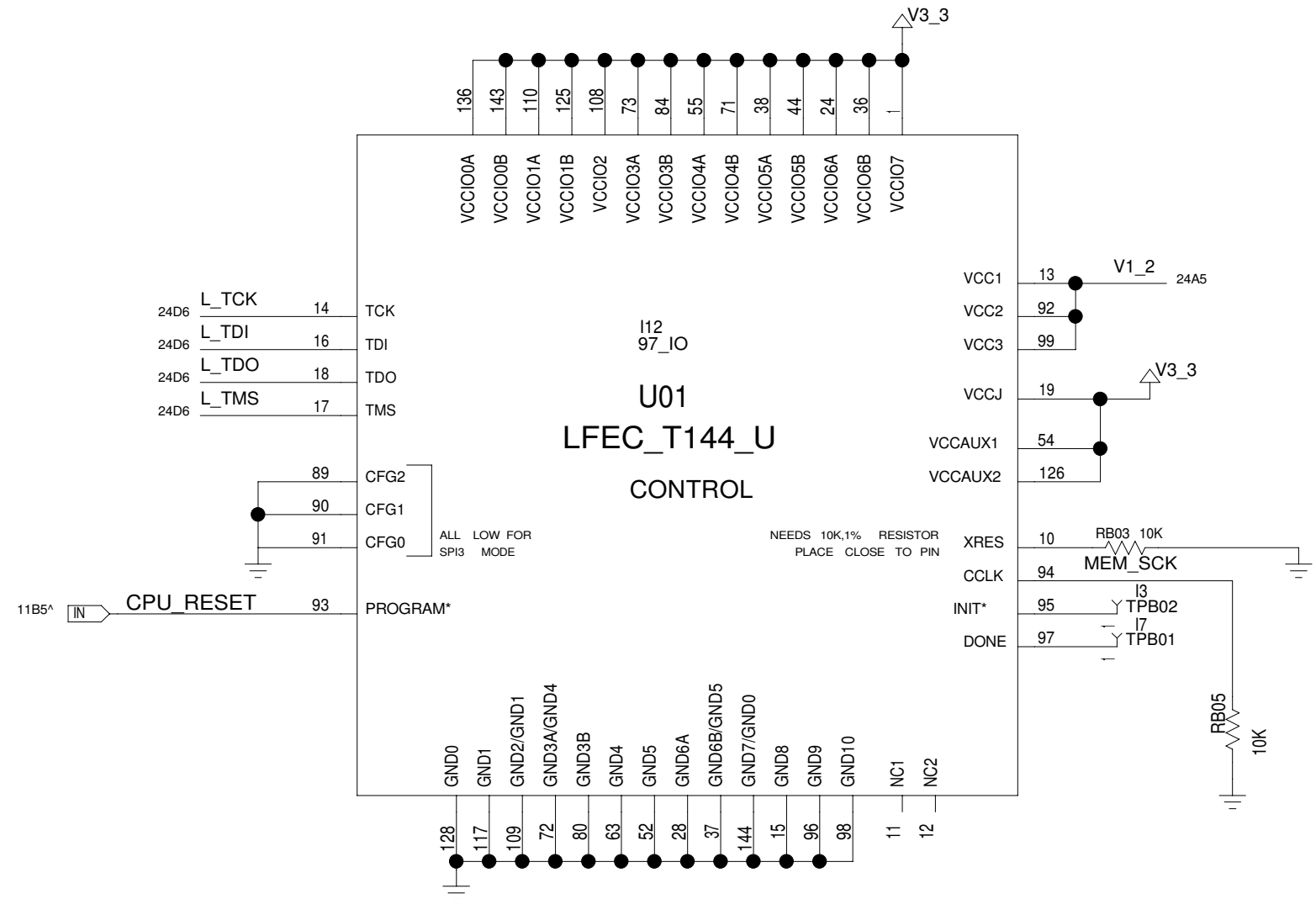
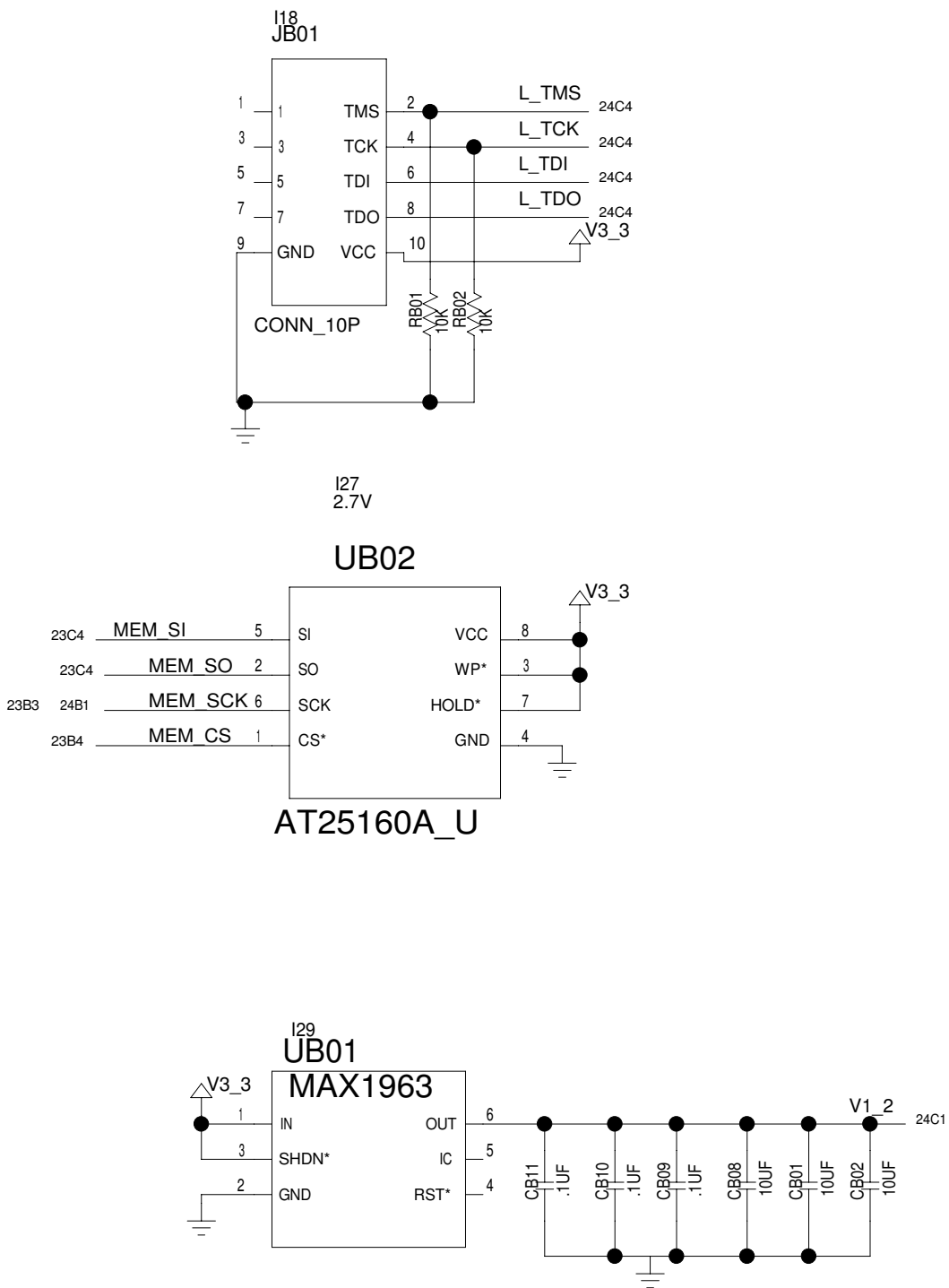
TITLE: DS33M30M31M33EE01A0 T3E3 LIU I/F. P.2,9,20-22	DATE: 04/15/2007
ENGINEER: STEVE SCULLY	PAGE: 8/11(BLOCK) 8/34(TOTAL)



SIGNALS FOR
HIERARCHY INTERFACE

BEGIN CPLD HIERARCHY BLOCK

TITLE:	DS33M33DK01A0	DATE:	10/03/2007
OVERHEAD.	P.2,10,23-24	PAGE:	1/2(BLOCK)
ENGINEER:	STEVE SCULLY		23/26(TOTAL)



END CPLD HIERARCHY BLOCK

TITLE: DS33M33DK01A0 OVERHEAD.	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 24/26(TOTAL)
P.2,10,23-24	



TITLE: DS33M33DK01A0	DATE:
ETHERNET. P.5-6,19,25-26	10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 25/26(TOTAL)

D

C

B

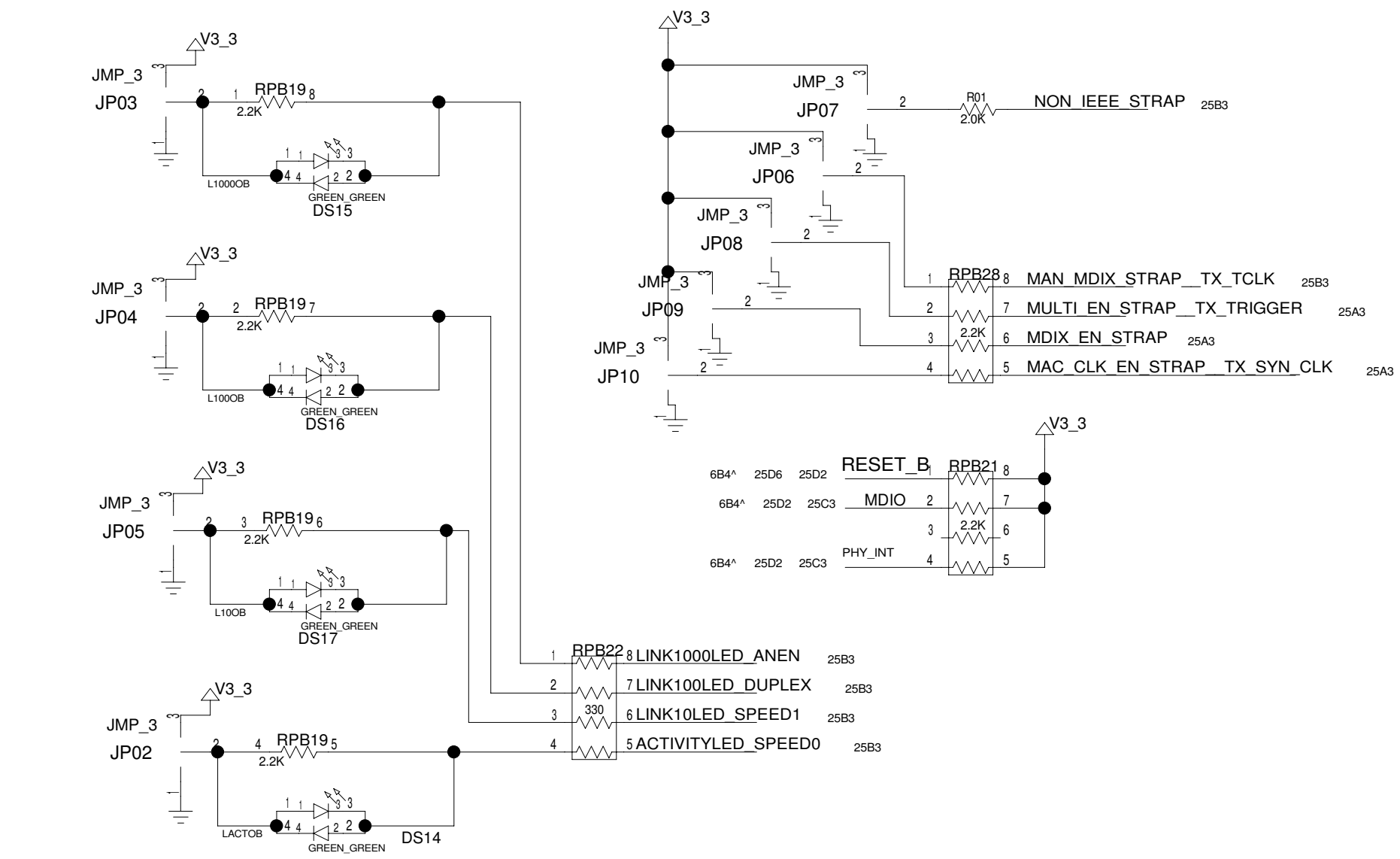
A

D

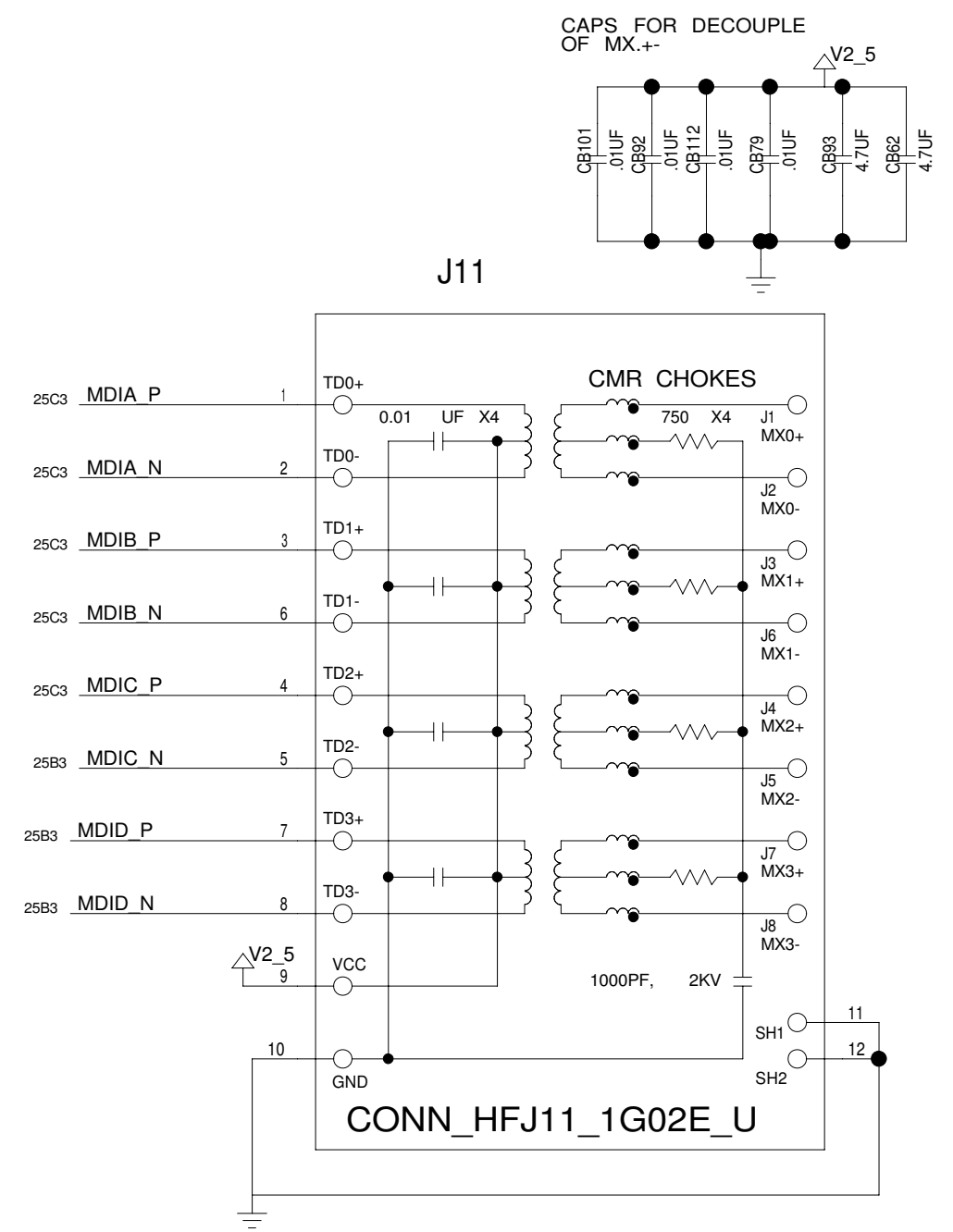
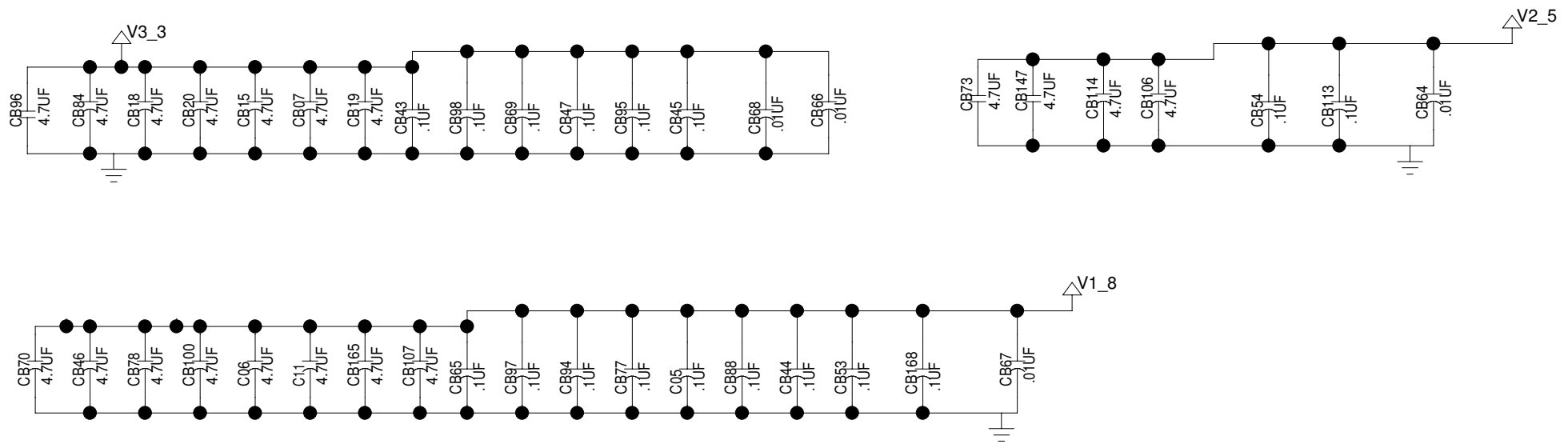
C

B

A



CHECK THAT 2.2K RES USE THE SAME RPACK STRAP OPTIONS HERE DO NOT FOLLOW DATASHEET



END PHY HIERARCHY BLOCK

TITLE: DS33M33DK01A0	DATE: 10/03/2007
ETHERNET. P.5-6,19,25-26	PAGE: 2/2(BLOCK)
ENGINEER: STEVE SCULLY	26/26(TOTAL)