SCOPE: CMOS, MICROPROCESSOR-COMPATIBLE, 8-BIT A/D CONVERTER

Device Type	Generic Number
01	MX7574S(x)/883B
02	MX7574T(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter		Mil-Std-1835	Case Outline	Package Code
MAXIM	SMD			
Q	V	GDIP1-T18 or CDIP2-T18	18 LEAD CERDIP	J18
E	2	CQCC1-N20	20 LCC	L20

Absolute Maximum Ratings:

V_{DD} to AGND ..... 0V to 7V
V_{DD} to DGND ..... 0V to 7V
AGND to DGND ..... -0.3V, +0.3V
Clock Input Voltage to DGND ..... -0.3V to V_{DD}
Digital Input Voltage to DGND ..... -0.3V to V_{DD}
Digital Output Voltage to DGND ..... -0.3V to V_{DD}
AIN to AGND ..... -20V to +20V
Digital Input Voltage to DGND ..... -0.3V, (V_{DD}+0.3V)
Digital Output Voltage to DGND ..... -0.3V, (V_{DD}+0.3V)
VREF ..... -20V, +20V
VBOFS ..... -20V, +20V
VAIN ..... -20V, +20V

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
18 pin CERDIP(derate 10.5mW/°C above +70°C) 842mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
18 pin CERDIP..... 45°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
18 pin CERDIP..... 95°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Supply Voltage Range (V_{DD}) .....+5V
Reference Voltage (VREF) ..... -10V
Ground ..... AGND=DGND=0V
Clock Resistance 150k
Clock Capacitance (C_{CLK}) 100pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Resolution NOTE 5	RES			All	8		Bits
Relative Accuracy	RA	External clock frequency 500kHz.	1,2,3	01 02		±0.75 ±0.50	LSB
Differential Nonlinearity	DNL	External clock frequency 500kHz.	1,2,3	01 02		±0.875 ±0.75	LSB
Gain Error	AE	Gain Error is measured after calibrating out offset error. External clock frequency 500kHz.	1 2,3	01		±5.0 ±6.5	LSB
			1 2,3	02		±3.0 ±4.5	
Offset Error	VOS	External clock frequency 500kHz.	1 2,3	01		±60 ±80	LSB
			1 2,3	02		±30 ±50	
Resistance mismatch between BOFS and AIN	RM		1,2,3	All		±1.5	%
Input Resistance	RIN	At VREF AT BOFS At AIN	1,2,3	All	5 10 10	15 30 30	kΩ
Digital Input High Level Voltage	V_{IH}	$\overline{RD}$, $\overline{CS}$ NOTE 3	1,2,3	All	2.4		V
Digital Input Low Level Voltage	V_{IL}	$\overline{RD}$, $\overline{CS}$ NOTE 3	1,2,3	All		0.8	V
Digital Input Current	I_{IN}	V_{IN}=0V or V_{DD}	1 2,3	All		±1.0 ±10	µA
Digital Input Capacitance	CID	NOTE 2	1,2,3	All		5.0	pF
Clock Input High	V_{IH}	NOTE 3	1,2,3	All	3.0		V
Clock Input Low	V_{IL}	NOTE 3	1,2,3	All		0.4	V
Clock Input High Current	I_{IH}		1,2,3	All		±2.0	mA
Clock Input Low Current	I_{IL}		1 2,3	All		±1.0 ±10	µA
Digital Output High Voltage	V_{OH}	I_{SOURCE}=40µA	1,2,3	All	4.0		V
Digital Output Low Level Voltage	V_{OL}	I_{SINK}=1.6mA	1,2,3	All		0.4	V
Floating State Leakage Current (DB7-DB0)	I_{LKG}	V_{OUT}=0V or V_{DD}	1 2,3	All		±1.0 ±10	µA
Floating State Output Capacitance (DB7-DB0)	C_{OUT}	NOTE 2	1,2,3	All		7.0	pF

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Supply Current	I_{CC}	BUSY and RD= HIGH, AIN=0V	1,2,3	All		5.0	mA
CS Pulse Width	t_{CS}	NOTE 4	9,10,11	All	150		ns
RD to CS Setup Time	t_{WSCS}	NOTE 5		All	0		ns
CS to BUSY Propagation Delay	t_{CBPD}	BUSY Load=20pF NOTE 5		All		180	ns
		BUSY Load=100pF NOTE 5				200	
BUSY to RD Setup Time	t_{BSR}	NOTE 4	9,10,11	All	0		ns
BUSY to CS Setup Time	t_{BSCS}	NOTE 4	9,10,11	All	0		ns
Data Valid Access Time	t_{RAD}	Load=20pF NOTE 4 Load=100pF NOTE 5		All		200 400	ns
Data Valid Hold Time	t_{RHD}	NOTE 4	9,10,11	All	80	180	ns
CS to RD Hold Time	t_{RHS}	NOTE 4	9,10,11	All		500	ns
Reset Time Requirement	t_{RESET}	NOTE 4	9,10,11	All	3		µs
RD to BUSY	t_{WBPD}	NOTE 4 BUSY Load=20pF	9,10,11	All		2	µs
Conversion Time	$t_{CONVERT}$	Ext CLK 500kHz NOTE 5		All		15	

NOTE 1: V_{DD}=+5.0V, VREF=-10V. Unipolar Configuration, R_{CLK}=180kΩ. C_{CLK}=100pF.
NOTE 2: Guaranteed at 25°C if not tested to the limits specified in Table 1.
NOTE 3: Guaranteed by functional pattern testing in external clock RAM, ROM, and SLOW modes.
NOTE 4: Static RAM interface mode.
NOTE 5: Guaranteed at 25°C, +125°C, -55°C, if not tested to the limits specified in Table 1.

ORDERING INFORMATION:

	Package	Pkg. Code	MAXIM PART #	SMD Number
01	18 pin CERDIP	J18	MX7574SQ/883B	5962-8961604VA
01	20 pin LCC	L20	MX7574SE/883B	5962-89616042C
02	18 pin CERDIP	J18	MX7574TQ/883B	5962-8961603VA
02	20 pin LCC	L20	MX7574TE/883B	5962-89616032C

TERMINAL CONNECTIONS:

	J18	L20
Pin		
1	V_{DD}	NC
2	VREF	V_{DD}
3	BOFS	VREF
4	AIN	BOFS
5	AGND	AIN
6	D7(MSB)	AGND
7	D6	D7(MSB)
8	D5	D6
9	D4	D5
10	D3	D4
11	D2	NC
12	D1	D3
13	D0(LSB)	D2
14	$\overline{BUSY}$	D1
15	$\overline{RD}$	D0(LSB)
16	$\overline{CS}$	$\overline{BUSY}$
17	CLK	$\overline{RD}$
18	DGND	$\overline{CS}$
19		CLK
20		DGND

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4**, 9, 10, 11***
Group A Test Requirements Method 5005	1, 2, 3, 4** , 9, 10, 11***
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroups 4, capacitance tests shall be tested at initial qualification and upon redesign.
*** Subgroups 10 and 11 if not tested, are guaranteed to the limits in Table 1.