

**SCOPE: CMOS, 8-BIT, 8-CHANNEL DATA ACQUISITION SYSTEM**

<u>Device Type</u>	<u>Generic Number</u>
01	MAX170DM(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
JA	GDIP1-T8 or CDIP2-T8	8 LEAD CERDIP	J08

**Absolute Maximum Ratings**

V <sub>DD</sub> to AGND .....	-0.3V to +7V
V <sub>SS</sub> to DGND.....	+0.3V to -17V
AIN to AGND .....	±15V
Clock Input Voltage to DGND .....	-0.3V to V <sub>DD</sub>
Digital Input Voltage to GND .....	-0.3V to (V <sub>DD</sub> +0.3V)
Digital Output Voltage to GND .....	-0.3V to (V <sub>DD</sub> +0.3V)
Lead Temperature (soldering, 10 seconds) .....	+300°C
Storage Temperature .....	-65°C to +160°C
Continuous Power Dissipation .....	T <sub>A</sub> =+70°C
8 pin CERDIP(derate 8.0mW/°C above +70°C) .....	640mW
Junction Temperature T <sub>J</sub> .....	+150°C
Thermal Resistance, Junction to Case, $\Theta_{JC}$	
8 pin CERDIP.....	55°C/W
Thermal Resistance, Junction to Ambient, $\Theta_{JA}$ :	
8 pin CERDIP.....	125°C/W

**Recommended Operating Conditions**

Ambient Operating Range (T <sub>A</sub> ) .....	-55°C to +125°C
Supply Voltage (V <sub>DD</sub> ).....	+4.75V to +5.25V
Supply Voltage (V <sub>SS</sub> ).....	-11.4V to -15.75V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TABLE 1. ELECTRICAL TESTS:**

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T <sub>A</sub> ≤ +125°C V <sub>DD</sub> =+5V±5%, V <sub>SS</sub> =-11.4V to -15.75V, f <sub>CLK</sub> =2.5MHz Unless otherwise specified						
<b>ACCURACY</b>								
Resolution	RES				All	12		Bits
Integral Nonlinearity	INL			1,2,3	All		±1.0	LSB
Differential Nonlinearity	DNL	Guaranteed Monotonic over Temperature		1,2,3	All		±1.0	LSB
Offset Error	V <sub>OS</sub>	NOTE 1		1,2,3	All		±5.0	LSB
Full-Scale Error	AE	NOTE 2		1	All		±5.0	LSB
Full-Scale Tempco		NOTES 3,4		1,2,3	All		±45	ppm/°C
Conversion Time	t <sub>CONV</sub>	14 Clock cycles		9,10,11	All		5.6	µs
<b>ANALOG INPUTS</b>								
Input Voltage Range				1,2,3	All	0	+5	V
Input Current		A <sub>IN</sub> =0V to +5V		1,2,3	All		3.5	mA
<b>INTERNAL REFERENCE</b>								
V <sub>REF</sub> Output Voltage				1	All	-5.2	-5.3	V
Output Current Sink Capability		NOTE 5		1,2,3	All		5.0	mA
<b>LOGIC INPUTS</b>								
Logic High Threshold	V <sub>IH</sub>			1,2,3	All	+2.4		V
Logic Low Threshold	V <sub>IL</sub>			1,2,3	All		+0.8	V
Input Current	I <sub>IN</sub>	A <sub>IN</sub> =0V to V <sub>DD</sub> , Clock _____ A <sub>IN</sub> =0V to V <sub>DD</sub> , CONVST/EOC		1,2,3	All		±10 ±200	µA
Input Capacitance	C <sub>IN</sub>	NOTE 6		4	All		10	pF
<b>LOGIC OUTPUTS</b>								
Output High Voltage	V <sub>OH</sub>	Data I <sub>SOURCE</sub> =200µA		1,2,3	All	4.0		V
Output Low Voltage	V <sub>OL</sub>	Data I <sub>SINK</sub> =1.6mA Data I <sub>SINK</sub> =6.0mA		1,2,3	All		0.4 1.5	V
<b>POWER REQUIREMENTS</b>								
Positive Supply Current	I <sub>DD</sub>	CONVST/EOC=V <sub>DD</sub> , A <sub>IN</sub> =0V		1,2,3	All		8	mA
Negative Supply Current	I <sub>SS</sub>	CONVST/EOC=V <sub>DD</sub> , A <sub>IN</sub> =0V		1,2,3	All		-11	mA
<b>TIMING</b>								
Clock Pulse Width	t <sub>CH</sub>	Clock High		9	All	40		ns
	t <sub>CL</sub>	Clock Low				60		
CONVST/EOC Pulse Width	t <sub>SH</sub>	High		9	All	40		ns
	t <sub>SL</sub>	Low				60		
CONVST/EOC to Clock Skew	t <sub>SC0</sub>	Leading clock		9	All		50	ns
	t <sub>SC1</sub>	Leading clock +1				275		
Clock to Data Delay	t <sub>PD</sub>			9	All	25	155	ns

NOTE 1: Typical change over temperature is  $\pm 1$ LSB.

NOTE 2:  $FS=+5.000V$ . Ideal last code transition =  $FS-3/2$  LSB. Adjusted for offset error.

NOTE 3: Full scale  $Tempco=\Delta FS/\Delta T$ , where  $\Delta FS$  is full scale change from  $25^{\circ}C$  to  $+125^{\circ}C$  or  $-55^{\circ}C$ .

NOTE 4: Includes internal reference drift.

NOTE 5: Output current should not change during conversion.

NOTE 6: Guaranteed by design, not subject to test.

NOTE 7: Timing Specifications are sample tested at  $25^{\circ}C$  to ensure compliance. Guaranteed but not tested over temperature. All input control signals are specified with  $tR=tF=5ns$  (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Package	ORDERING INFORMATION:
8 pin CERDIP	MAX170DMJA/883B

#### TERMINAL CONNECTIONS:

	8 PIN CERDIP	
1	$V_{DD}$	Positive Supply, +5V
2	$A_{IN}$	Analog Input, 0V to +5V Unipolar
3	$V_{REF}$	Reference Voltage Output, -5.25V
4	GND	Ground
5	DATA	Serial Data Output
6	CLOCK	Clock Input, TTL/+5V CMOS compatible.
7	$\overline{\text{CONVST/EOC}}$	Conversion start input for three wire mode. End-of-conversion output for two wire mode.
8	$V_{SS}$	Negative Supply, -12V or -15V.

## QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
  1. Test condition A, B, C, D.
  2. TA = +125°C, minimum.
  3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

**TABLE 2. ELECTRICAL TEST REQUIREMENTS**

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10**, 11**
Group A Test Requirements Method 5005	1, 2, 3, 9, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

\* PDA applies to Subgroup 1 only.

\*\* Guaranteed but not tested.