

SCOPE: 500ksps, 12-bit ADCs with Track/Hold and Reference

<u>Device Type</u>	<u>Generic Number</u>
01	MAX122(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
YG	CDIP4-T24	24 LEAD SIDEBRAZE	Y24

Absolute Maximum Ratings

V_{DD} to GND	-0.3V to 6V
VSS to DGND	-0.3V to -17V
AIN to AGND	$\pm 15V$
AGND to DGND	$\pm 0.3V$
Digital Inputs/Outputs to DGND	-0.3V to ($V_{DD} + 0.3V$)
Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature	-65°C to +160°C
Continuous Power Dissipation	$T_A = +70^\circ C$
24 pin narrow Sidebraxe (derate 14.3mW/°C above +70°C)	1143mW
Junction Temperature T_J	+150°C
Thermal Resistance, Junction to Case, Θ_{JC}	25°C/W
Thermal Resistance, Junction to Ambient, Θ_{JA} :	70°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A)	-55°C to +125°C
Positive Supply Voltage Range (V_{CC})	4.75V to 5.25V
Negative Supply Voltage Range (V_{EE})	-10.8V to -15.75V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤T _A ≤ +125°C V _{DD} =+4.75V to +5.25V, V _{SS} =-10.8 to -15.75V, f _{CLK} =5MHz Unless otherwise specified					
ACCURACY							
Resolution	RES		1,2,3	All	12		Bits
Differential Non-linearity Note 1	DNL	12-bit no missing codes over temperature range	1,2,3	All		±1.0	LSB
Integral Non-linearity Note 1	INL		1,2,3	All		±1.0	LSB
Bipolar Zero Error Note 1		Code 00..00 to 00..01 transition, near A _{IN} =0V	1,2,3	All		±3.0	LSB
Full-Scale Error Note 1,2		Including reference; adjusted for bipolar zero error	1	All		±8.0	LSB
Power Supply Rejection Ratio (Change in FS, <u>3</u>)	PSRR	V _{DD} only, 5V ±5% V _{SS} only, -12V ±10% V _{SS} only, -15V ±5%	1,2,3	All		±0.75 ±1.0 ±1.0	LSB
ANALOG INPUT							
Input Range			1,2,3	All	-5	+5	V
Input Current		A _{IN} =+5V (approximately 6kΩ to REF)	1,2,3	All		2.5	mA
Input Capacitance Note 4			4	All		10	pF
REFERENCE							
Output Voltage		No external load, A _{IN} =5V	1	All	-5.02	-4.98	V
External Load Regulation		0mA < I _{SINK} < 5mA, A _{IN} =0V	1,2,3	All		5.0	mV
Temperature Drift		Note 5	1,2,3	All		±30	ppm/°C
DYNAMIC PERFORMANCE							
Signal-to-Noise Plus Distortion	SINAD	f _s =333kHz, A _{IN} =±5Vp-p, 50kHz	1 2,3	All	70 69		dB
Total Harmonic Distortion	THD	First five harmonics	1 2,3	All		-78 -75	dB
Spurious-Free Dynamic Range	SFDR		1 2,3	All	78 75		dB
CONVERSION TIME							
Synchronous	t _{CONV}	13 t _{CLK}	1,2,3	All		2.60	μs
Clock Frequency	f _{CLK}		1,2,3	All	0.1	5.0	MHz
DIGITAL INPUTS							
		CLKIN, CONVST, RD, CS					
Input High Voltage	V _{IH}		1,2,3	All	2.4		V
Input Low Voltage	V _{IL}		1,2,3	All		0.8	V
Input Capacitance		NOTE 4	4	All		10	pF
Input Current		V _{IN} =0V or V _{DD}	1,2,3	All		±5	μA

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DIGITAL OUTPUT		D11-D0, INT/BUSY						
Output Low Voltage	V _{OL}	I _{SINK} =1.6mA		1,2,3	All		0.4	V
Output High Voltage	V _{OH}	I _{SOURCE} =1mA		1,2,3	All	V _{DD} -0.5		V
Leakage Current	I _{LKG}	V _{IN} =0V or V _{DD} , D11-D0		1,2,3	All		±5	µA
Output Capacitance		NOTE 4		4	All		10	pF
POWER REQUIREMENTS								
Positive Supply Voltage	V _{DD}	Guaranteed by supply rejection test		1,2,3	All	4.75	5.25	V
Negative Supply Voltage	V _{SS}	Guaranteed by supply rejection test		1,2,3	All	-10.80	-15.75	V
Positive Supply Current <u>6/</u>	I _{DD}	V _{DD} =5.25V, V _{SS} =-15.75V, A _{IN} =0V		1,2,3	All		15	mA
Negative Supply Current <u>6/</u>	I _{SS}	V _{DD} =5.25V, V _{SS} =-15.75V, A _{IN} =0V		1,2,3	All		20	mA
Power Dissipation <u>6/</u>		V _{DD} =5V, V _{SS} =-12V, A _{IN} =0V		1,2,3	All		315	mW
TIMING CHARACTERISTICS <u>7/</u>								
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time	t _{CS}			9,10,11	All	0		ns
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time	t _{CH}			9,10,11	All	0		ns
$\overline{\text{CONVST}}$ Pulse Width	t _{CW}			9,10,11	All	30		ns
$\overline{\text{RD}}$ Pulse Width	t _{rw}			9,10,11	All	t _{DA}		ns
Data-Access Time	t _{DA}	CL=100pF		9 10,11	All		75 120	ns
Bus-Relinquish Time	t _{DH}			9 10,11	All		50 80	ns
$\overline{\text{RD}}$ or $\overline{\text{CONVST}}$ to $\overline{\text{BUSY}}$	t _{B0}	CL=50pF		9 10,11	All		75 120	ns
CLKIN to $\overline{\text{BUSY}}$ or $\overline{\text{INT}}$	t _{B1}	CL=50pF		9 10,11	All		110 180	ns
CLKIN to $\overline{\text{BUSY}}$ Low	t _{B2}	In mode 5		9 10,11	All		90 150	ns
$\overline{\text{RD}}$ to $\overline{\text{INT}}$ High	t _{IH}	CL=50pF		9 10,11	All		50 90	ns
$\overline{\text{BUSY}}$ or $\overline{\text{INT}}$ to Data Valid	t _{BD}	CL($\overline{\text{INT}}$, $\overline{\text{BUSY}}$)=50pF CL(Data)=100pF		9 10,11	All		20 35	ns
Acquisition Time	t _{AQ}	NOTE 4		9 10,11	All	350 400		ns

NOTE 1: These tests are performed at V_{DD}=5V, V_{SS}=-15V. Operation over supply is guaranteed by supply rejection tests.

NOTE 2: Ideal full-scale transition is at +5V -3/2LSB=+4.9963V, adjusted for offset error.

NOTE 3: Supply rejection defined as change in full-scale transition voltage with the specified change in supply voltage=(FS at nominal supply)-(FS at nominal supply \pm tolerance), expressed in LSBs.

NOTE 4: For design guidance only, not tested.

NOTE 5: Temperature drift is defined as the change in output voltage from +25°C to T_{MIN} or T_{MAX}.
It is calculated as $TC=(\Delta REF/VREF)/(\Delta T)$

NOTE 6: $\overline{CS}=\overline{RD}=\overline{CONVST}=0V$, MODE=5V

NOTE 7: Control inputs specified with $t_r=t_f=5ns$ (10% to 90% of +5V) and timed from a 1.6V voltage level. Output delays are measured to +0.8V if going low, or +2.4V if going high. For bus-relinquish time, a change of 0.5V is measured. See Commercial datasheet, Figures 1 and 2 for load circuits.

Package	ORDERING INFORMATION:
24 pin Sidebrazed	MAX122BMYG/883B

TERMINAL CONNECTIONS:

	YG24
1	MODE
2	V _{SS}
3	V _{DD}
4	A _{IN}
5	VREF
6	AGND
7	D11
8	D10
9	D9
10	D8
11	D7
12	DGND
13	D6
14	D5
15	D4
16	D3
17	D2
18	D1
19	D0
20	\overline{CONVST}
21	CLKIN
22	$\overline{INT/BUSY}$
23	\overline{CS}
24	\overline{RD}

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.