SCOPE: IMPROVED 16-CHANNEL/DUAL 8-CHANNEL, HIGH PERFORMANCE CMOS ANALOG MULTIPLEXER

Device Type	Generic Number	Circuit Function
01	DG406A(x)/883B	16-Channel Analog Multiplexer
02	DG407A(x)/883B	Dual 8-Channel Analog Multiplexer

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
K	GDIP1-T28 or CDIP2-T28	28 LEAD CERDIP	J28
Z	CQCC1-N28	28-Pin Ceramic LCC	L28

Absolute Maximum Ratings

Voltage Referenced to V$^-$

- V$^+$ to V$^-$ .... -0.3V, 44V
- V$^+$ to GND .... -0.3V, 25V
- Digital Inputs, S, D 1/ .... (V$^-$) -2V to (V$^+$)+2V or 30mA whichever occurs first
- Continuous Current, Any terminal 30mA
- Peak Current, S or D (Pulsed at 1ms, 10% duty cycle max) 100mA

Lead Temperature (soldering, 10 seconds) .... +300°C

Storage Temperature .... -65°C to +160°C

Continuous Power Dissipation .... T_A=+70°C

28 lead CERDIP(derate 16.7mW/°C above +70°C) 1333mW

28 lead LCC (derate 10.2mW/°C above +70°C) 816mW

Junction Temperature T_J .... +150°C

Thermal Resistance, Junction to Case, ΘJC:

- Case Outline 28 lead CERDIP.................. 25°C/W
- Case Outline 28 lead LCC .... 15°C/W

Thermal Resistance, Junction to Ambient, ΘJA:

- Case Outline 28 lead CERDIP.................. 60°C/W
- Case Outline 28 lead LCC .... 98°C/W

Recommended Operating Conditions

- Ambient Operating Range (T_A) .... -55°C to +125°C
- Positive Supply Voltage (V$^+$) .... +15V
- Negative Supply Voltage (V$^-$) .... -15V
- V_{AL} (max) 0.8V
- V_{AH} (min) 2.4V

1/ Signals on Sx, Dx, A0, A1, A2, A3 or EN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS: DUAL SUPPLIES

TEST	Symbol	**CONDITIONS** -55 °C <=T_A<= +125°C V+=+15V, V-=-15V, GND=0V V_{AH}=+2.4V, V_{AL}=+0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	NOTE 3	1,2,3	All	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S =-1.0mA, V_D=±10V	1 2,3	All		100 125	Ω
$r_{DS(ON)}$ Matching between Channels	$\Delta r_{DS(ON)}$	V_D=±10V NOTE 4	1 2,3	All		8 10	Ω
On-resistance Flatness	r_{FLAT}	I_S=-1.0mA, V_D=±5V or 0V	1 2,3	All		9 12	Ω
Source-OFF Leakage Current	$I_{S(OFF)}$	V_S =±10V, VD=±10V, V_{EN}=0V	1 2,3	All	-0.5 -50	0.5 50	nA
Drain-OFF Leakage Current	$I_{D(OFF)}$	V_S =±10V, VD=±10V, V_{EN}=0V	1 2,3	01	-1.0 -200	1.0 200	nA
			1 2,3	02	-1.0 -100	1.0 100	
Drain-ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D =V_S=±10V, sequence each switch on	1 2,3	01	-1.0 -200	1.0 200	nA
			1 2,3	02	-1.0 -100	1.0 100	
INPUT							
Input Current/Voltage High	I_{AH}	V_{IN}= 2.4V, 15V	1,2,3	All	-1.0	1.0	µA
Input Current/Voltage Low	I_{AL}	V_{EN}=0V, 2.4V; V_A=0V	1,2,3	All	-1.0	1.0	µA
SUPPLY							
Power Supply Range			1,2,3	All	±4.5	±20	V
Positive Supply Current	I+	V_{EN}=V_A=0V or 4.5V	1 2,3	All		30 75	µA
		V_{EN}=2.4V, $V_{A(ALL)}$=0V or 2.4V	1 2,3	All		0.5 1.0	mA
Negative Supply Current	I-	V_{EN}=2.4V, $V_{A(ALL)}$=0V or 2.4V	1 2,3	All	-1 -10	1 10	µA
DYNAMIC							
Transition Time	t_{TRANS}	Figure 2	9 10,11	All		300 400	ns
Break-Before-Make interval	t_{OPEN}	Figure 4	9	All	10		ns

TABLE 1. ELECTRICAL TESTS: DUAL SUPPLIES

TEST	Symbol	**CONDITIONS** -55 °C <=T_A<= +125°C V+=+15V, V-=-15V, GND=0V V_{AH}=2.4V, V_{AL}=0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
DYNAMIC							
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3	9 10,11	All		200 400	ns
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3	9 10,11	All		150 300	ns
Charge Injection	Q	C_L=1.0nF, V_S=0V, R_S=0Ω, Figure 5, NOTE 3	9	All		15	pC

TABLE 1. ELECTRICAL TESTS: SINGLE SUPPLY

TEST	Symbol	**CONDITIONS** -55 °C <=T_A<= +125°C V+=+12V, V-=0V, GND=0V V_{AH}=+2.4V, V_{AL}=+0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	NOTE 3	1,2,3	All	0	12	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S =-1.0mA, V_D=3V or 10V	1	All		175	Ω
DYNAMIC							
Transition Time	t_{TRANS}	V_{S1}=8V, V_{S16}=0V, V_A=0V Figure 2	9	All		450	ns
Enable Turn-On Time	$t_{ON(EN)}$	V_{AL}=0V, V_{S1}=5V, Figure 3	9	All		600	ns
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3	9	All		300	ns
Charge Injection	Q	C_L=1.0nF, V_{S1}=0V, R_S=0Ω, Figure 5, NOTE 3	9	All		10	pC

NOTE 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this datasheet.

NOTE 3: Guaranteed by design.

NOTE 4: $\Delta r_{ON}=\Delta r_{ON}(max)-\Delta r_{ON}(min)$. On-resistance match between channels and flatness are guarantee only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

FIGURE 2: TRANSITION TIME TEST CIRCUIT: See Commercial Data Sheet
FIGURE 3: ENABLE SWITCHING TIME TEST CIRCUIT: See Commercial Data Sheet
FIGURE 4: BREAK-BEFORE-MAKE INTERVAL: See Commercial Data Sheet
FIGURE 5: CHARGE INJECTION: See Commercial Data Sheet

ORDERING INFORMATION:	
DG406AK/883B 28 CDIP	DG407AK/883B 28 CDIP
DG406AZ/883B 28 LCC	DG407AZ/883B 28 LCC

TRUTH TABLE **TERMINAL CONNECTION**

A3	**A2**	**A1**	**A0**	**EN**	**DG406A ON SWITCH**		**TERMINAL NUMBER**	**01 DG406A**	**02 DG407A**
X	X	X	X	0	None			J28, L28	J28 & L28
0	0	0	0	1	1		1	V+	V+
0	0	0	1	1	2		2	NC	DB
0	0	1	0	1	3		3	NC	NC
0	0	1	1	1	4		4	S16	S8B
0	1	0	0	1	5		5	S15	S7B
0	1	0	1	1	6		6	S14	S6B
0	1	1	0	1	7		7	S13	S5B
0	1	1	1	1	8		8	S12	S4B
1	0	0	0	1	9		9	S11	S3B
1	0	0	1	1	10		10	S10	S2B
1	0	1	0	1	11		11	S9	S1B
1	0	1	1	1	12		12	GND	GND
1	1	0	0	1	13		13	NC	NC
1	1	0	1	1	14		14	A3	NC
1	1	1	0	1	15		15	A2	A2
1	1	1	1	1	16		16	A1	A1
							17	A0	A0
					DG407A		18	EN	EN
	A2	**A1**	**A0**	**EN**	**On Switch**		19	S1	S1A
	X	X	X	0	None		20	S2	S2A
	0	0	0	1	1		21	S3	S3A
	0	0	1	1	2		22	S4	S4A
	0	1	0	1	3		23	S5	S5A
	0	1	1	1	4		24	S6	S6A
	1	0	0	1	5		25	S7	S7A
	1	0	1	1	6		26	S8	S8A
	1	1	0	1	7		27	V-	V-
	1	1	1	1	8		28	D	DA

Logic “0” $V_{AL} \leq 0.8V$
Logic “1” $V_{AH} \geq 2.4V$

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:

   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.