19-5039; Rev 5; 1/12

EVALUATION KIT AVAILABLE

2.2MHz, Dual, Step-Down DC-DC Converters, Dual LDOs, and RESET

MAX16922

General Description

The MAX16922 power-management integrated circuit (PMIC) is designed for medium power-level automotive applications and integrates multiple supplies in a small footprint. The device includes one high-voltage step-down converter (OUT1) and three low-voltage cascaded DC-DC converters (OUT2, OUT3, OUT4). OUT1 and OUT2 are step-down DC-DC converters, and OUT3/OUT4 are linear regulators. The device also includes a reset output ($\overline{RESET}$) and a high-voltage-compatible enable input (EN).

The 1.2A output high-efficiency, step-down DC-DC converter (OUT1) operates from a voltage up to 28V continuous and is protected from load-dump transients up to 45V. The 600mA output high-efficiency step-down DC-DC converter (OUT2) runs from a voltage up to 5.5V. The two 300mA LDO linear regulators offer low dropout of only 130mV (typ). The power-good $\overline{RESET}$ output provides voltage monitoring for OUT1 and OUT2.

OUT1 and OUT2 use fast 2.2MHz PWM switching and small external components. The high-voltage converter (OUT1) enters skip mode automatically under light loads to prevent an overvoltage condition from occurring at the output. The low-voltage synchronous DC-DC converter (OUT2) can operate in forced-PWM mode to prevent any AM band interference or high-efficiency auto-PWM mode.

The MAX16922 includes overtemperature shutdown and overcurrent limiting. The device is designed to operate from -40°C to +125°C ambient temperature.

Features

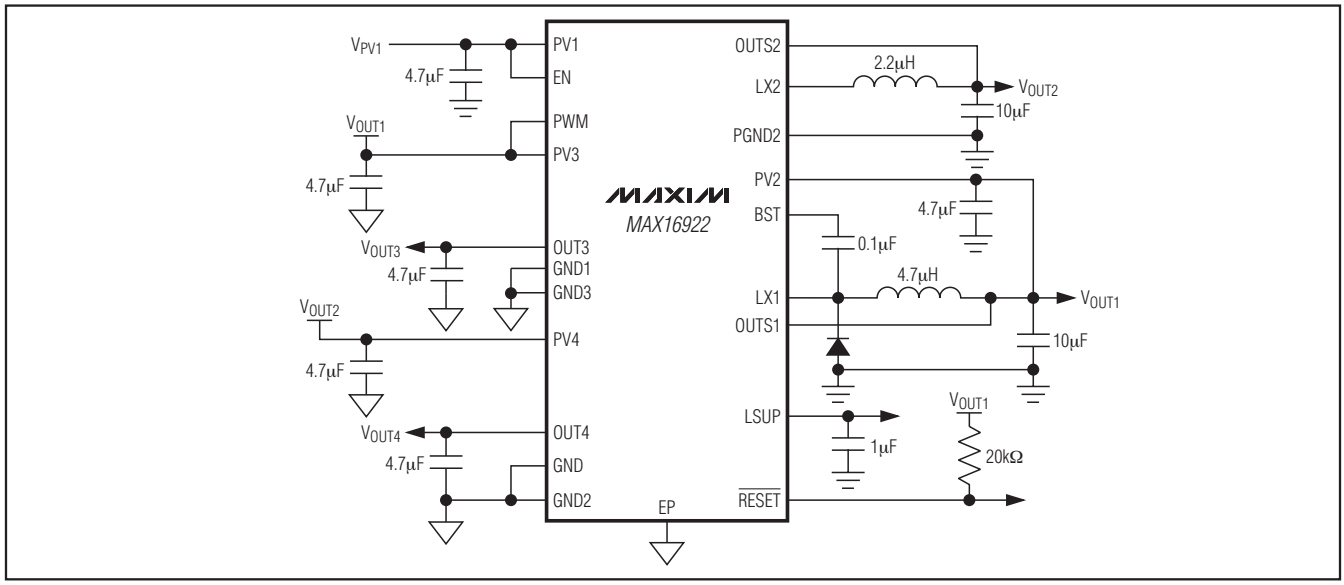
- **1.2A High-Efficiency 2.2MHz DC-DC Converter**
  - **3.7V to 28V Operating Supply Voltage**
  - **45V Load-Dump Protection**
  - **Output Voltage: 3.0V to 5.5V**
- **600mA High-Efficiency 2.2MHz DC-DC Converter**
  - **2.7V to 5.5V Supply Voltage**
  - **Output Voltage: 1.0V to 3.9V**
  - **180° Out-of-Phase Operation**
  - **Forced-PWM and Auto-PWM Modes**
- **LDO Linear Regulators**
  - **OUT3: 1.0V to 4.15V at 300mA**
  - **OUT4: 1.0V to 4.15V at 300mA**
  - **Separate Inputs for Increased Efficiency**
- **Enable Input**
- **$\overline{RESET}$ Output Monitoring on OUT1 and OUT2**
- **Overtemperature and Short-Circuit Protection**
- **Available in**
  - **5mm x 5mm x 0.8mm, 20-Pin TQFN-EP**
  - **4.5mm x 6.5mm, 20-Pin TSSOP-EP**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16922ATP_ /V+*	-40°C to +125°C	20 TQFN-EP**
MAX16922AUP_ /V+*	-40°C to +125°C	20 TSSOP-EP**

*Insert the desired suffix letters (from the Selector Guide) into the blank "_" to complete the part number.
+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.
**EP = Exposed pad.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

2.2MHz, Dual, Step-Down DC-DC Converters, Dual LDOs, and RESET

ABSOLUTE MAXIMUM RATINGS

PV1, EN to GND .....-0.3V to +45V
LX1 to GND.....-0.5V to (PV1 + 0.3V)
LX2 to GND.....-0.5V to (PV2 + 0.3V)
BST to LX1.....-0.3V to +6.0V
PV2, PV3, PV4, OUTS1, PWM, $\overline{RESET}$ to GND_....-0.3V to +6.0V
OUTS2 .....-0.3V to (PV2 + 0.3V)
OUT3 .....-0.3V to (PV3 + 0.3V)
OUT4 .....-0.3V to (PV4 + 0.3V)
LX1 RMS Current 2.0A
LX2 RMS Current 1.2A
PGND2 to GND_.....-0.3V to +0.3V
LSUP to GND.....-0.3V to +6V
OUTS_, OUT_ Output Short-Circuit Duration .....Continuous

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 31.3 mW/°C above +70°C) 2500mW
TSSOP (derate 26.5 mW/°C above +70°C) 2122mW
ESD_{HB} (all pins) .....±2kV
ESD_{MM} (all pins) .....±200V
ESD_{CDM} (corner pins) .....±750V
ESD_{CDM} (other pins).....±500V
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 32°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 2.7°C/W

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 37.7°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{PV1} = 13.5V, V_{PV2} = V_{PV3} = V_{OUT1}, V_{PV4} = V_{OUT2}; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT1—SYNCHRONOUS STEP-DOWN DC-DC CONVERTER						
Supply-Voltage Range	V_{PV1}	(Note 3)	3.7		28	V
		Operation < 500ms			45	
PV1 Undervoltage Lockout	$V_{UVLO,R}$	PV1 rising		3.7	4.0	V
	$V_{UVLO,F}$	PV1 falling	2.85	3.3		
BST Refresh Load Enable	V_{BRLE}	PV1 falling (option enabled)		6.45		V
BST Refresh Load Hysteresis				0.65		V
LSUP Regulator Voltage	V_{LSUP}	6V ≤ V_{PV1} ≤ 28V	4.75	5.0	5.45	V
Supply Current	I_{PV1}	EN = low		14		µA
PWM Switching Frequency	f_{SW}	Internally generated	2.0	2.2	2.4	MHz
Voltage Accuracy	V_{OUT1}	Duty cycle = 20% to 90%; I_{LOAD} = 300mA to 1.2A	-3		+3	%
		SKIP mode (Note 4)	-2		+4	
DMOS On-Resistance		V_{PV1} = 4V, V_{BST} = 9V, I_{LX1} = 0.2A		300	700	mΩ
Current-Limit Threshold			1.4	1.75	2.1	A
Soft-Start Ramp Time				2.2		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{PV1} = 13.5V, V_{PV2} = V_{PV3} = V_{OUT1}, V_{PV4} = V_{OUT2}; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Current	I_{OUT1}	(V_{OUT1} + 1.0V) ≤ V_{PV1} ≤ 28V	1.2			A
LX1 Leakage Current		V_{PV1} = 12V, LX1 = GND or V_{PV1}; T_A = -40°C to +85°C		±1		µA
Maximum Duty Cycle	DC_{MAX}			94		%
Minimum Duty Cycle	DC_{MIN}	f_{SW} = 2.2MHz		20		%
OUTS1 Discharge Resistance		EN = low (or optionally EN = high and V_{PV1} < 5.7V)		70		Ω
OUT2—SYNCHRONOUS STEP-DOWN DC-DC CONVERTER						
Supply-Voltage Range	V_{PV2}	Fully operational	2.7		5.5	V
PWM Switching Frequency	f_{SW}	Internally generated	2.0	2.2	2.4	MHz
Voltage Accuracy	V_{OUT2}	Duty cycle = 20% to 90%; I_{LOAD} = 1mA to 600mA, PWM = high	-3		+3	%
		SKIP mode (Note 4)	-2		+4	%
pMOS On-Resistance		V_{PV2} = 5.0V, I_{LX2} = 0.2A		150	250	mΩ
nMOS On-Resistance		V_{PV2} = 5.0V, I_{LX2} = 0.2A		200	350	mΩ
pMOS Current-Limit Threshold			0.75	0.9	1.05	A
nMOS Zero-Crossing Threshold				50		mA
Soft-Start Ramp Time				1.5		ms
Maximum Output Current	I_{OUT2}	V_{OUT2} + 0.5V ≤ V_{PV2} ≤ 5.5V	600			mA
LX2 Leakage Current		V_{PV2} = 6V, LX2 = PGND2 or V_{PV2}; T_A = -40°C to +85°C		±1		µA
Duty-Cycle Range		Forced-PWM mode only, minimum duty cycle in skip mode is 0% (Note 4)	15		100	%
OUTS2 Discharge Resistance		V_{EN} = 0V		70		Ω
OUT3—LDO REGULATOR						
Input Voltage	V_{PV3}		1.7		5.5	V
Voltage Accuracy	V_{OUT3}	V_{OUT3} + 0.4V ≤ V_{PV3} ≤ 5.5V, I_{LOAD} = 1mA	-2		+2	%
Load Regulation		I_{LOAD} = 0 to 300mA		-0.2		%
Dropout Voltage		V_{PV3} = 1.8V, I_{LOAD} = 250mA (Note 4)		130	320	mV
Current Limit				450		mA
Power-Supply Rejection Ratio		I_{OUT3} = 30mA, f = 1kHz		57		dB
Shutdown Output Resistance		EN = low		1		kΩ
OUT4—LDO REGULATOR						
Input Voltage	V_{PV4}		1.7		5.5	V
Voltage Accuracy	V_{OUT4}	(V_{OUT4} + 0.4V) ≤ V_{PV4} ≤ 5.5V, I_{LOAD} = 1mA	-2		+2	%
Load Regulation		I_{LOAD} = 0 to 300mA		-0.2		%
Dropout Voltage		V_{PV4} = 1.8V, I_{LOAD} = 250mA (Note 4)		130	320	mV
Current Limit				450		mA

2.2MHz, Dual, Step-Down DC-DC Converters, Dual LDOs, and RESET

ELECTRICAL CHARACTERISTICS (continued)

(V_{PV1} = 13.5V, V_{PV2} = V_{PV3} = V_{OUT1}, V_{PV4} = V_{OUT2}; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

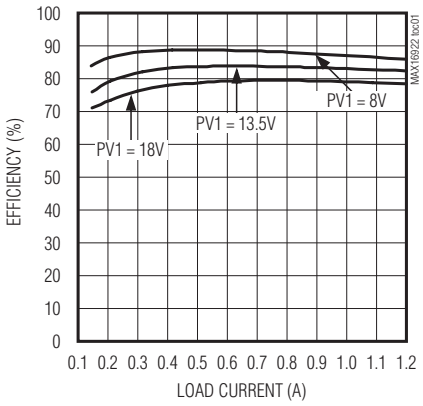
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio		I_{OUT4} = 30mA, f = 1kHz		57		dB
Shutdown Output Resistance		EN = low		1		kΩ
THERMAL OVERLOAD						
Thermal-Shutdown Temperature		(Note 4)	150	175		°C
Thermal-Shutdown Hysteresis				15		°C
$\overline{\text{RESET}}$						
OUT1 OV Threshold				110		%
OUT1 Reset Threshold		Reset option 1 (see the *Selector Guide*)	85	90	95	%
		Reset option 2 (see the *Selector Guide*)	75	80	85	
OUT2 Reset Threshold		Percentage of nominal output	85	90	95	%
Reset Timeout Period		Reset timeout option 1 (see the *Selector Guide*)		14.9		ms
		Reset timeout option 2 (see the *Selector Guide*)		1.9		
Output-High Leakage Current				1		µA
Output Low Level		Sinking -3mA			0.4	V
UV Propagation Time				28		µs
EN LOGIC INPUT						
EN Threshold Voltage		EN rising	1.4	1.8	2.2	V
EN Threshold Hysteresis				0.4		V
Input Current		V_{EN} = 5V		0.5		µA
PWM LOGIC INPUT						
Input High Level		PWM rising	1.8			V
Input Low Level		PWM falling			0.4	V
Logic-Input Current		$0 \le V_{PWM} \le 5.5V$		1		µA

Note 2: All units are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 3: Once PVI exceeds undervoltage-lockout rising threshold 4.0V and the device is in regulation.
Note 4: Guaranteed by design; not product tested.

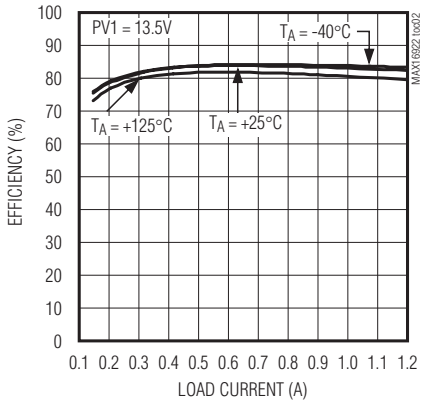
Typical Operating Characteristics

(V_{PV1} = 13.5V, V_{PV2} = V_{PV3} = V_{OUT1}, V_{PV4} = V_{OUT2}; T_A = +25°C, unless otherwise specified.)

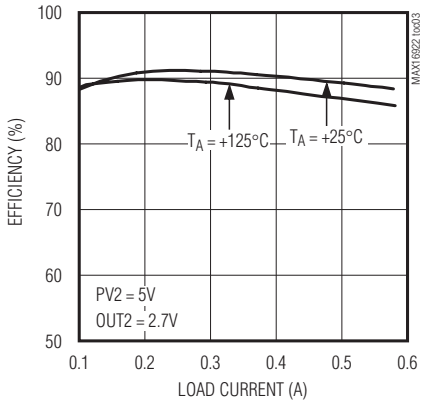
OUT1 EFFICIENCY vs. LOAD CURRENT



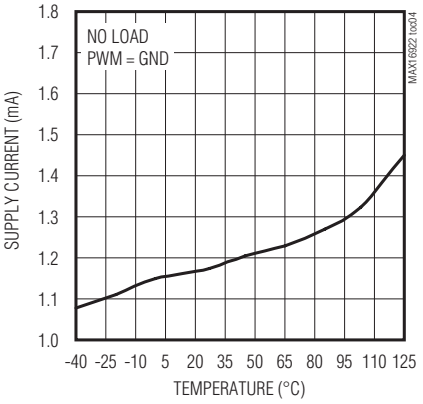
OUT1 EFFICIENCY vs. LOAD CURRENT



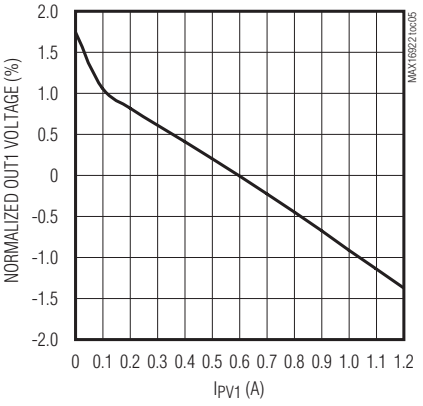
OUT2 EFFICIENCY vs. LOAD CURRENT



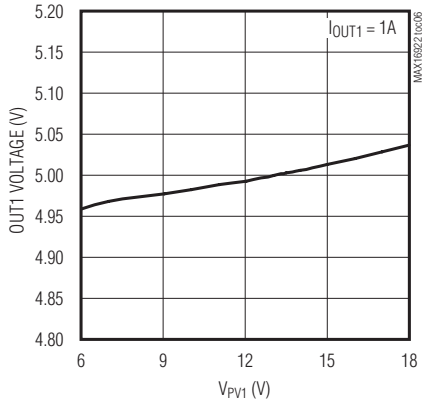
SUPPLY CURRENT vs. TEMPERATURE



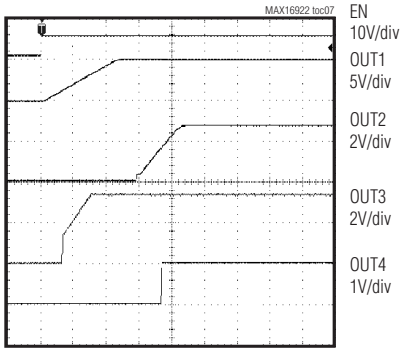
NORMALIZED OUT1 VOLTAGE vs. LOAD CURRENT



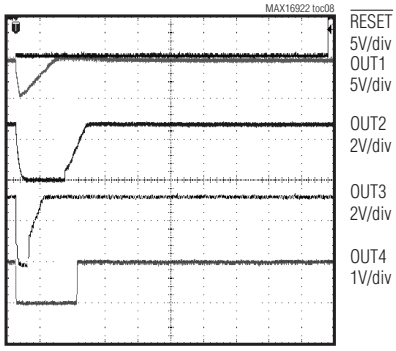
OUT1 VOLTAGE vs. V_{PV1}



POWER-UP ENABLE TURNING ON



POWER-UP/DOWN AT THERMAL SHUTDOWN

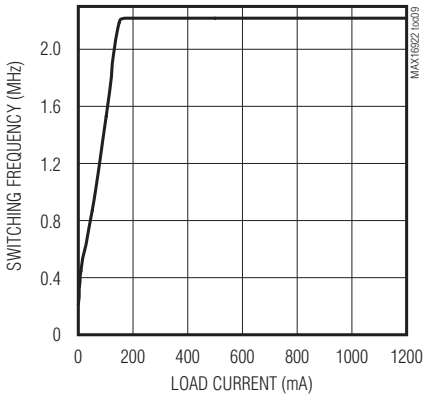


2.2MHz, Dual, Step-Down DC-DC Converters, Dual LDOs, and RESET

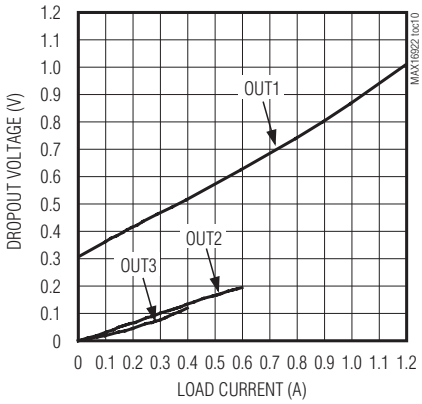
Typical Operating Characteristics (continued)

(V_{PV1} = 13.5V, V_{PV2} = V_{PV3} = V_{OUT1}, V_{PV4} = V_{OUT2}; T_A = +25°C, unless otherwise specified.)

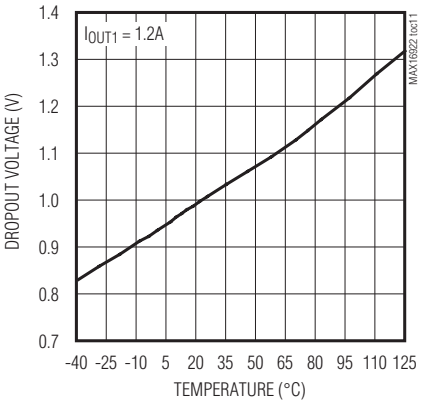
SWITCHING FREQUENCY vs. LOAD CURRENT



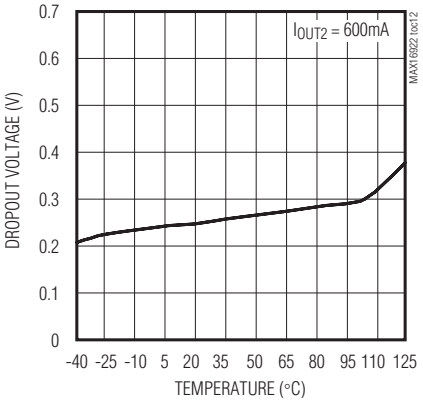
DROPOUT VOLTAGE vs. LOAD CURRENT



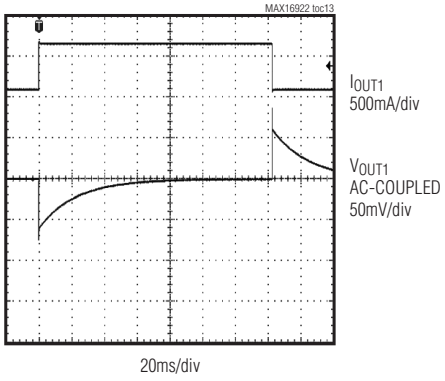
OUT1 DROPOUT VOLTAGE vs. TEMPERATURE



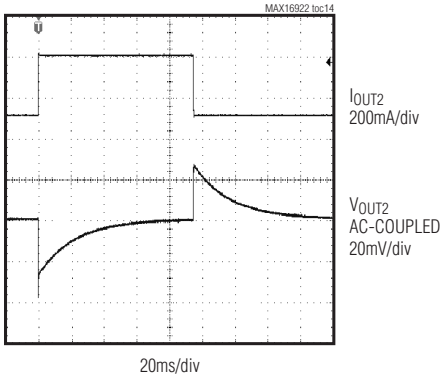
OUT2 DROPOUT VOLTAGE vs. TEMPERATURE



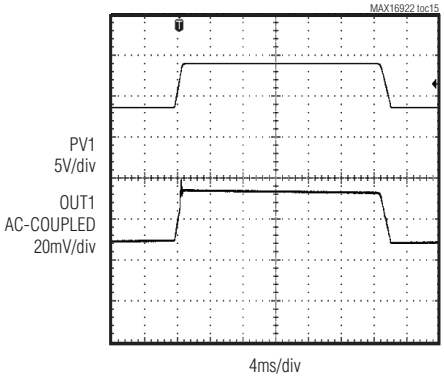
OUT1 LOAD TRANSITION



OUT2 LOAD TRANSIENT



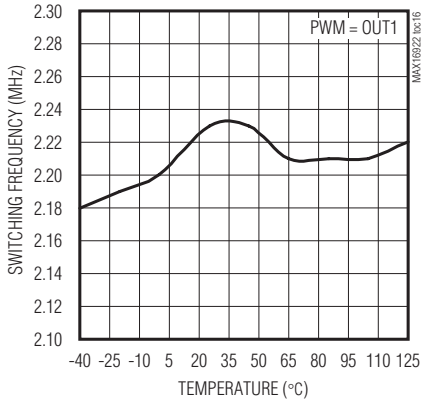
OUT1 LINE TRANSIENT



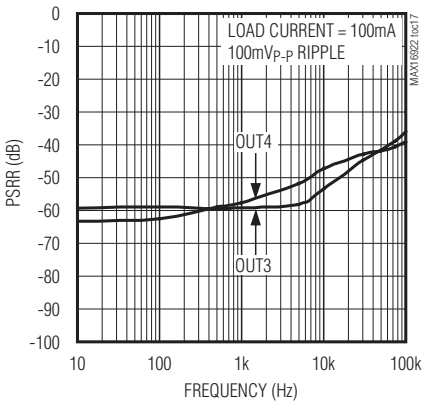
Typical Operating Characteristics (continued)

(V_{PV1} = 13.5V, V_{PV2} = V_{PV3} = V_{OUT1}, V_{PV4} = V_{OUT2}; T_A = +25°C, unless otherwise specified.)

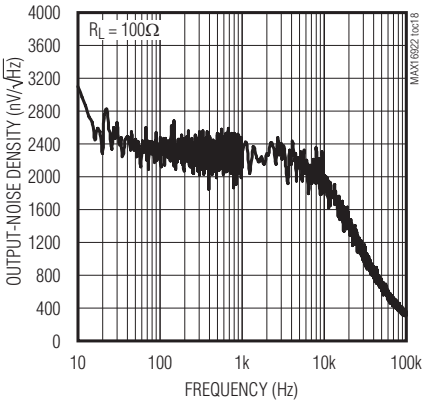
SWITCHING FREQUENCY vs. TEMPERATURE



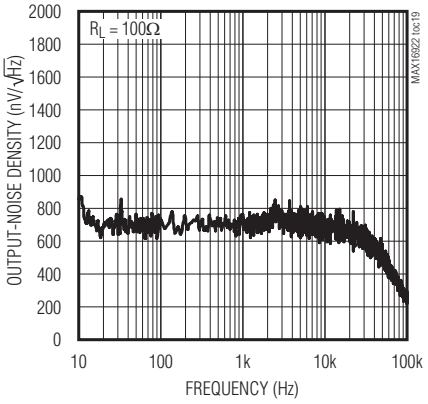
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



OUT3 OUTPUT-NOISE DENSITY vs. FREQUENCY

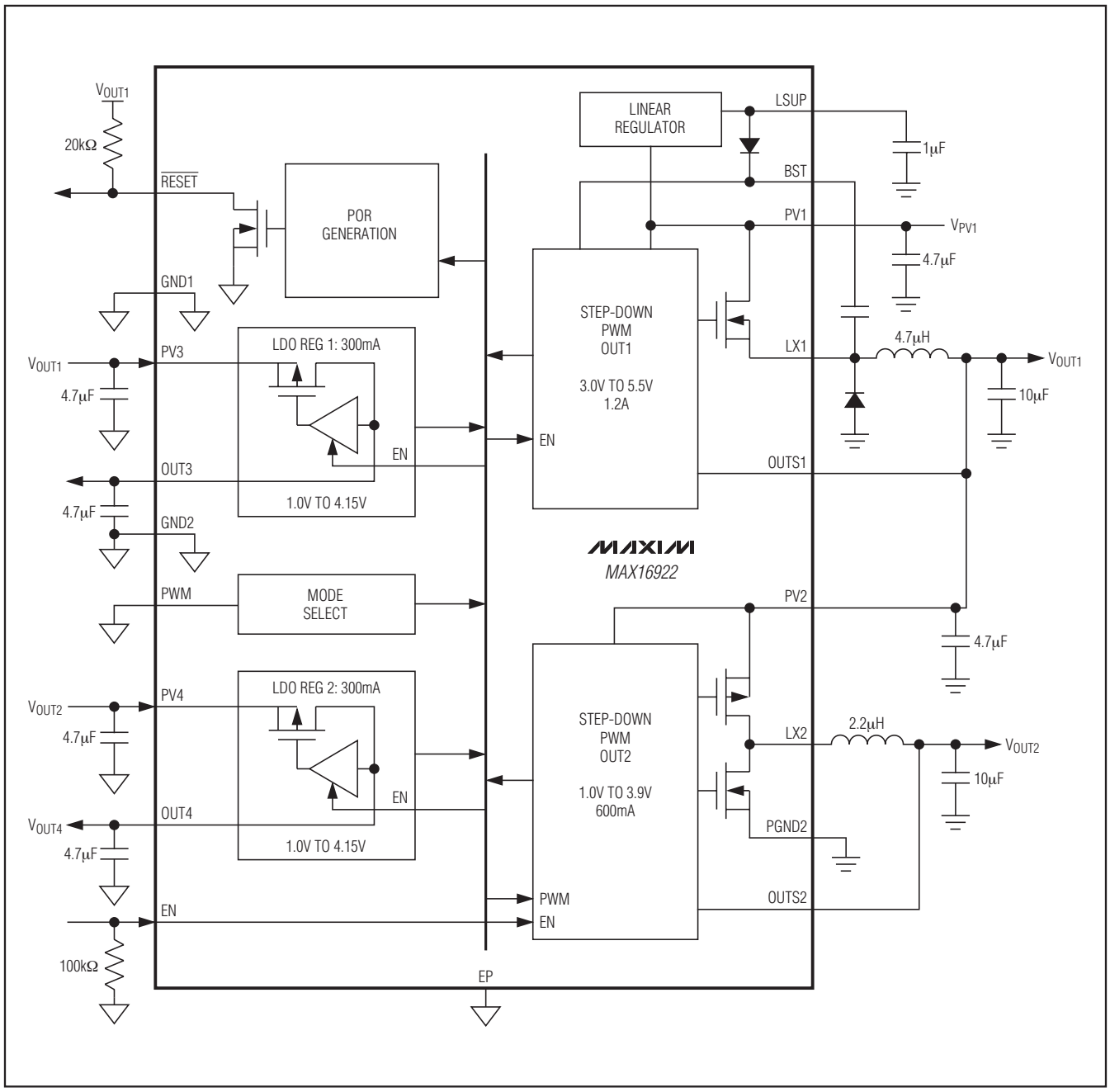


OUT4 OUTPUT-NOISE DENSITY vs. FREQUENCY



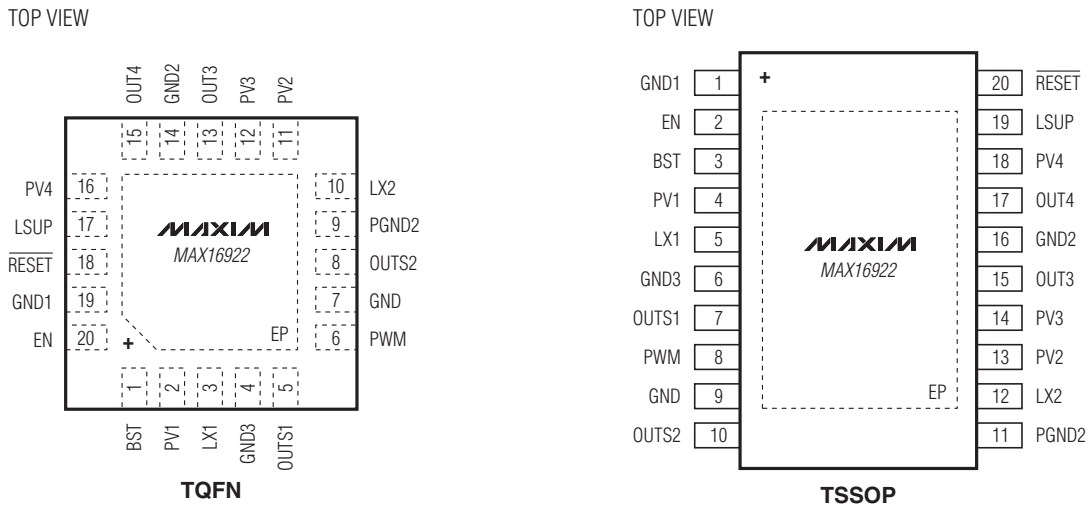
2.2MHz, Dual, Step-Down DC-DC Converters, Dual LDOs, and RESET

Functional Diagram



2.2MHz, Dual, Step-Down DC-DC Converters, Dual LDOs, and RESET

Pin Configurations



Pin Description

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	3	BST	Bootstrap Capacitor Input. Connect a 0.1µF ceramic capacitor from BST to LX1.
2	4	PV1	OUT1 Supply Input. Connect a 4.7µF or larger ceramic capacitor from PV1 to PGND.
3	5	LX1	Inductor Connection for OUT1. Connect a 4.7µH inductor between LX1 and OUTS1, and a Schottky diode between LX1 (cathode) and the power-ground plane (anode) as shown in the *Functional Diagram*.
4	6	GND3	Ground. Connect GND, GND1, GND2, and GND3 together.
5	7	OUTS1	OUT1 Voltage-Sensing Input. Connect OUTS1 directly to the OUT1 output voltage and bypass to power-ground plane with a minimum total capacitance of 15µF. The total capacitance can include input bypass capacitors cascaded from OUT1, discharged by a 70Ω resistance between OUTS1 and GND3 when disabled.
6	8	PWM	PWM Control Input. Connect PWM to OUTS1 to force LX2 to switch every cycle. Connect PWM to high for forced-PWM operation on OUT2. Connect low for auto-PWM operation to improve efficiency at light loads.
7	9	GND	Ground. Connect GND, GND1, GND2, and GND3 together.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	TSSOP		
8	10	OUTS2	OUT2 Voltage Sense Input. Connect OUTS2 directly to the OUT2 output voltage and bypass to PGND2 with a minimum total capacitance of 10µF. The total capacitance can include input bypass capacitors cascaded from OUT2, discharged by a 70Ω resistance between OUTS2 and PGND2 when disabled.
9	11	PGND2	Power Ground for BUCK 2. Connect PGND2 and GND_ together near the device.
10	12	LX2	Inductor Connection for OUT2. Connect a 2.2µH inductor between LX2 and OUT2 as shown in the *Functional Diagram*.
11	13	PV2	OUT2 Supply Input. Connect a 4.7µF or larger ceramic capacitor from PV2 to ground.
12	14	PV3	Linear-Regulator Power Input for OUT3. Bypass PV3 to GND with a minimum 2.2µF ceramic capacitor.
13	15	OUT3	Linear-Regulator 1 Output. Bypass OUT3 to GND with a minimum 2.2µF ceramic capacitor internally discharged by a 1kΩ resistance when disabled.
14	16	GND2	Ground. Connect GND, GND1, GND2, and GND3 together.
15	17	OUT4	Linear-Regulator 2 Output. Bypass OUT4 to GND with a minimum 2.2µF ceramic capacitor. Internally discharged by a 1kΩ resistance when disabled.
16	18	PV4	Linear-Regulator Power Input for OUT4. Bypass PV4 to GND with a minimum 2.2µF ceramic capacitor.
17	19	LSUP	5V Logic Supply to Provide Power to Internal Circuitry. Bypass LSUP to GND1 with a 1µF ceramic capacitor.
18	20	$\overline{\text{RESET}}$	Open-Drain Reset Output for the Input Monitoring OUT1 and OUT2. External pullup required.
19	1	GND1	Ground. Connect GND, GND1, GND2, and GND3 together.
20	2	EN	Active-High Enable Input. Connect EN to PV1 or a logic-high voltage to turn on all regulators. Pull EN input low to place the regulators in shutdown.
—	—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND2 and GND_. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the device.

Detailed Description

The MAX16922 PMIC is designed for medium power level automotive applications requiring multiple supplies in a small footprint. As shown in the *Typical Applications Circuit*, the MAX16922 integrates one high-voltage power supply and three low-voltage cascaded power supplies. OUT1 and OUT2 are step-down DC-DC converters, and OUT3 and OUT4 are linear regulators. The device also includes a reset output ($\overline{RESET}$) and a high-voltage compatible enable input (EN). The operating input voltage range is from 3.5V to 28V and tolerant of transient voltages up to 45V.

OUT1 Step-Down DC-DC Regulator

Step-Down Regulator Architecture

OUT1 is a high-input voltage, high-efficiency 2.2MHz PWM current-mode step-down DC-DC converter that delivers up to 1.2A. OUT1 has an internal high-side n-channel switch and uses a low forward-drop freewheeling diode for rectification. Under normal operating conditions, OUT1 is fixed frequency to prevent unwanted AM radio interference. However, under light loads and high-input voltage, the step-down regulator skips cycles to maintain regulation. The output voltage is factory selectable from 3.0V to 5.5V in 50mV increments.

Soft-Start

When initially powered up or enabled with EN, the OUT1 step-down regulator soft-starts by gradually ramping up the output voltage for approximately 2.2ms. This reduces inrush current during startup. During soft-start the full output current is available. Before a soft-start sequence begins, the outputs of both DC-DC regulators discharge below 1.25V through an internal resistor. See the startup waveforms in the *Typical Operating Characteristics* section.

Current Limit

The MAX16922 limits the peak inductor current sourced by the n-channel MOSFET. When the peak current limit is reached, the internal n-channel MOSFET turns off for the remainder of the cycle. If the current limit is exceeded for 16 consecutive cycles and the output voltage is less than 1.25V, the n-channel MOSFET is turned off for 256 clock cycles to allow the inductor current to discharge and then initiate a soft-start sequence for all four outputs.

Dropout

The high-voltage, step-down converter (OUT1) of the MAX16922 is designed to operate near 100% duty-cycle. When the input voltage is close to the output voltage, the device tries to maintain the high-side switch on with 100% duty cycle. However, to maintain proper gate charge, the high-side switch must be turned off periodically so the LX pin can go to ground and charge the BST capacitor. As the input voltage approaches the output voltage, the effective duty cycle of the n-channel MOSFET approaches 94%. Every 4th cycle is limited to a maximum duty cycle of 75% (recharge period is approximately 112ns) while the remaining cycles can go to 100% duty cycle. As a result, when the MAX16922 is in dropout, the switching frequency is reduced by a factor of 4.

During dropout conditions under light load, the load current may not be sufficient to enable the LX pin to reach ground during the recharge period. To ensure the LX pin is pulled to ground and proper BST capacitor recharge occurs, an internal load is applied to OUTS1 when PV1 falls below approximately 6.5V. This load is approximately 70Ω and is connected between OUTS1 and GND3 through an internal switch.

OUT2 Step-Down DC-DC Regulator

Step-Down Regulator Architecture

OUT2 is a low-input voltage, high-efficiency 2.2MHz PWM current-mode step-down DC-DC converter that outputs up to 600mA. OUT2 has an internal high-side p-channel switch, and low-side n-channel switch for synchronous rectification. The DC-DC regulator supports auto-PWM operation so that under light loads the device automatically enters high-efficiency skip mode. The auto-PWM mode can be disabled by connecting the PWM input to OUTS1. The output voltage is factory selectable from 1.0V to 3.9V in 50mV increments.

Soft-Start

OUT2 enters soft-start when OUT1 finishes its soft-start sequence to prevent high startup current from exceeding the maximum capability of OUT1. The step-down regulator executes a soft-start by gradually ramping up the output voltage for approximately 1.5ms. This reduces inrush current during startup. During soft-start, the full output current is available. The soft-start sequence on OUT2 begins after the soft-start sequence is completed on OUT1. See the startup waveforms in the *Typical Operating Characteristics* section.

2.2MHz, Dual, Step-Down DC-DC Converters, Dual LDOs, and RESET

Current Limit

The MAX16922 limits the peak inductor current sourced by the p-channel MOSFET. When the peak current limit is reached, the internal p-channel MOSFET turns off for the remainder of the cycle. If the current limit is exceeded for 16 consecutive cycles, and the output voltage is less than 1.25V, the p-channel MOSFET is turned off and enters output discharge mode for 256 clock cycles, allowing the inductor current and output voltage to discharge. Once completed, a soft-start sequence is initiated on OUT2.

Dropout

As the input voltage approaches the output voltage, the duty cycle of the p-channel MOSFET reaches 100%. In this state, the p-channel MOSFET is turned on constantly (not switching), and the dropout voltage is the voltage drop due to the output current across the on-resistance of the internal p-channel MOSFET (R_{PCH}) and the inductor's DC resistance (R_L):

$$V_{DO} = I_{LOAD} (R_{PCH} + R_L)$$

PWM

The MAX16922 operates in either auto-PWM or forced-PWM modes. At light load, auto-PWM switches only as needed to supply the load to improve light-load efficiency of the step-down converter. At higher load currents (~160mA), the step-down converter transitions to fixed 2.2MHz switching frequency. Forced PWM always operates with a constant 2.2MHz switching frequency regardless of the load. Connect PWM high for forced-PWM applications or low for auto-PWM applications.

LDO Linear Regulators

The MAX16922 contains two low-dropout linear regulators (LDOs), OUT3 and OUT4. The LDO output voltages are factory preset, and each LDO supplies loads up to 300mA. The LDOs include an internal reference, error amplifier, p-channel pass transistor, and internal voltage-dividers. Each error amplifier compares the reference voltage to the output voltage (divided by the internal voltage-divider) and amplifies the difference. If the divided feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, allowing more current to pass to the outputs and increasing the output voltage. If the divided feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output. Each output voltage is factory selectable from 1.0V to 4.15V in 50mV increments. If not using one of the LDO outputs, then tie the associated input power pin (PV_) to ground.

Input Supply and Undervoltage Lockout

An undervoltage-lockout circuit turns off the LDO regulators when the input supply voltage is too low to guarantee proper operation. When PV3 falls below 1.25V (typ), OUT3 powers down. When PV4 falls below 1.5V (typ), OUT4 powers down.

Soft-Start

OUT3 enters soft-start when PV3 exceeds 1.25V, and OUT4 enters soft-start when PV4 exceeds 1.5V. This staggers the surge current during startup to prevent excess current draw from OUT1 or OUT2 that could trigger an overcurrent shutdown. The soft-start time for each LDO is 0.1ms (typ). See the startup waveforms in *the Typical Operating Characteristics* section.

Current Limit

The OUT3 and OUT4 output current is limited to 450mA (typ). If the output current exceeds the current limit, the corresponding LDO output voltage drops out of regulation. Excess power dissipation in the device can cause the device to turn off due to thermal shutdown.

Dropout

The dropout voltage for the linear regulators is 320mV (max) at 250mA load. To avoid dropout, make sure the input supply voltage corresponding to OUT3 and OUT4 is greater than the corresponding output voltage plus the dropout voltage based on the application output current requirements.

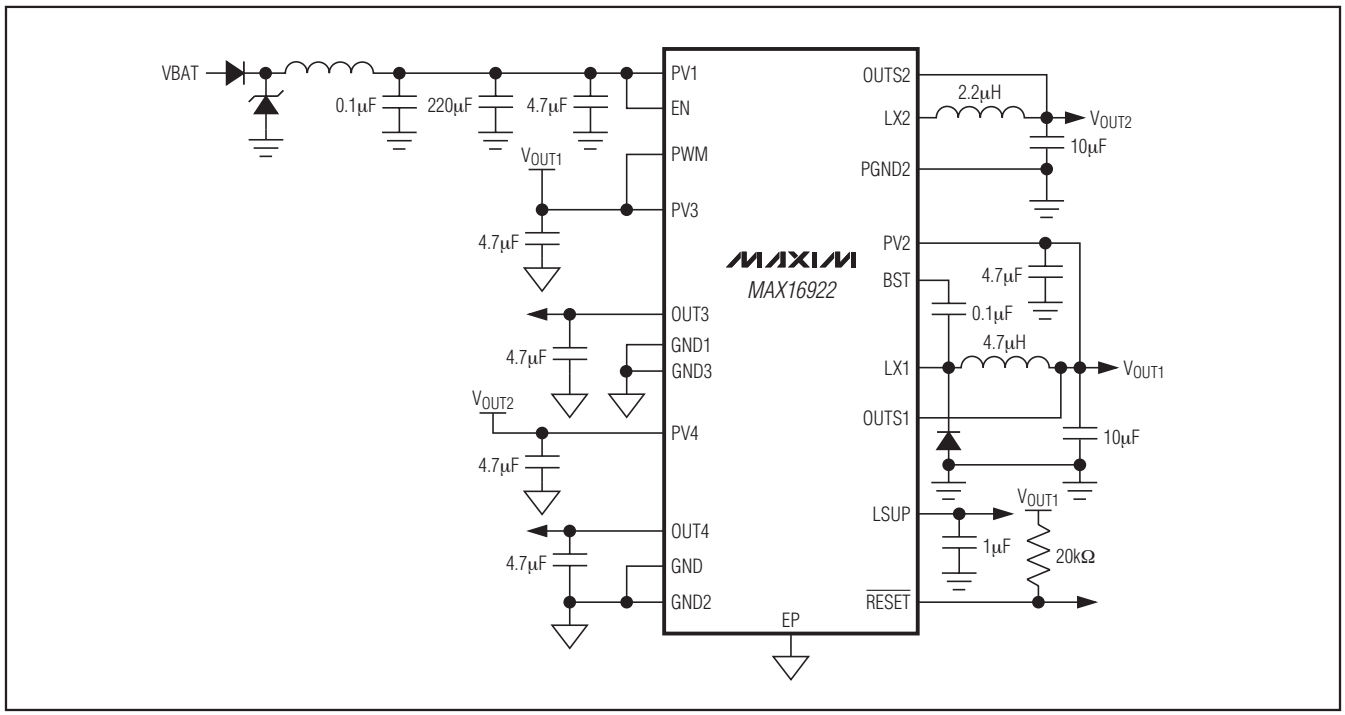
LSUP Linear Regulator

LSUP is the output of a 5V linear regulator that powers MAX16922 internal circuitry. LSUP is internally powered from PV1 and automatically powers up when EN is high and PV1 exceeds approximately 3.7V. LSUP automatically powers down when EN is taken low. Bypass LSUP to GND with a 1µF ceramic capacitor. LSUP remains on even during a thermal fault.

Thermal-Overload Protection

Thermal-overload protection limits the total power dissipation in the MAX16922. Thermal-protection circuits monitor the die temperature. If the die temperature exceeds +175°C, the device shuts down, allowing it to cool. Once the device has cooled by 15°C, the device is enabled again. This results in a pulsed output during continuous thermal-overload conditions. The thermal-overload protection protects the MAX16922 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature of +150°C. See the *Thermal Considerations* section for more information.

Typical Applications Circuit



Applications Information

Power-On Sequence

When the EN input is pulled high and PV1 is greater than 3.7V (typ), the 5V LSUP linear regulator turns on. Once LSUP exceeds 2.5V, the internal reference and bias are enabled. When the internal bias has stabilized OUT1, soft-start is initiated. After completion of soft-start on OUT1 (2.8ms typ), OUT2 soft-start is initiated. OUT3 soft-start is enabled when PV3 is greater than or equal to 1.25V (typ), and OUT4 soft-start is enabled when PV4 is greater than or equal to 1.5V (typ).

Care must be taken when driving the EN pin. Digital input signals deliver a fast edge that is properly detected by the MAX16922. If driving the EN pin with an analog voltage that has a slew rate of less than 1V/ms or a voltage-divider from PV1, then the input voltage on PV1 must always be less than 6V when the voltage at EN is near the turn-off threshold of 1.6V. If this cannot be guaranteed, then a 1kΩ resistor or 5.6V zener diode must be placed in parallel with the LSUP output capacitor to prevent possible damage to the device.

Power-Down and Restart Sequence

The MAX16922 can be shut down by thermal shutdown, enable low (EN), LSUP regulator undervoltage, or when PV1 falls below 3.0V (typ). When a shutdown occurs, all outputs discharge through an internal resistor connected between each output and ground. When enable is high, the die temperature is okay, the LSUP linear regulator is greater than 2.5V (typ), and OUT1 is less than 1.25V (typ); a complete soft-start power-on sequence is reinitiated.

Inductor Selection

The OUT1 step-down converter operates with a 4.7µH inductor and the OUT2 step-down converter operates with a 2.2µH inductor. The inductor's DC current rating must be high enough to account for peak ripple current and load transients. The step-down converter's architecture has minimal current overshoot during startup and load transients. In most cases, an inductor capable of 1.3 times the maximum load current is acceptable.

For optimum performance choose an inductor with DC-series resistance in the 50mΩ to 150mΩ range. For higher efficiency at heavy loads (above 400mA) and minimal load regulation, the inductor resistance should be kept as small as possible. For light-load applications (up to 200mA), higher resistance is acceptable with very little impact on performance.

2.2MHz, Dual, Step-Down DC-DC Converters, Dual LDOs, and RESET

Capacitor Selection

Input Capacitors

The input capacitor, CIN1, reduces the current peaks drawn from the supply and reduces switching noise in the MAX16922. The impedance of CIN1 at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their small size, low ESR, and small temperature coefficients. Use a 4.7µF ceramic capacitor or an equivalent amount of multiple capacitors in parallel between PV1 and ground. Connect CIN1 as close to the device as possible to minimize the impact of PCB trace inductance.

Connect a minimum 4.7µF ceramic capacitor between PV2 to ground, and a 2.2µF ceramic capacitor between PV3 to ground and PV4 to ground. Since PV2 is cascaded from OUT1, the input capacitor connected to PV2 can be used as part of the total output capacitance for OUT1.

Step-Down Output Capacitors

The step-down output capacitors are required to keep the output-voltage ripple small and to ensure regulation loop stability. These capacitors must have low impedance at the switching frequency. Surface-mount ceramic capacitors are recommended due to their small size and low ESR. The capacitor should maintain its capacitance overtemperature and DC bias. Ceramic capacitors with X5R or X7R temperature characteristics generally perform well. The output capacitance can be very low. Place a minimum of 15µF ceramic capacitance from OUTS1 to ground and a minimum of 10µF from OUTS2 to ground. When the OUT2 output voltage selection is below 2.35V, the output capacitance should be increased to prevent instability. For optimum load-transient performance and very low output ripple, the output capacitance can be increased. The maximum output capacitance should not exceed 3.8mF for OUT1 and 2.0mF for OUT2.

LDO Output Capacitors and Stability

Connect a 4.7µF ceramic capacitor between OUT3 and GND, and a second 4.7µF ceramic capacitor from OUT4 to GND. When the input voltage of an LDO is greater than 2.35V, the output capacitor can be decreased to 2.2µF. The equivalent series resistance (ESR) of the LDO output capacitors affects stability and output noise. Use output capacitors with an ESR of 0.1Ω or less to ensure stable operation and optimum transient response. Connect these capacitors as close as possible to the device to minimize PCB trace inductance.

Thermal Considerations

The maximum package power dissipation of the MAX16922 in the 20-pin thin QFN package is 2500mW. The power dissipated by the MAX16922 should not exceed this rating. The total device power dissipation is the sum of the power dissipation of the four regulators:

$$P_D = P_{D1} + P_{D2} + P_{D3} + P_{D4}$$

Estimate the OUT1 and OUT2 power dissipations as follows:

$$P_{D1} = I_{OUT1} \times V_{OUT1} \times \frac{1-\eta}{\eta}$$

$$P_{D2} = I_{OUT2} \times V_{OUT2} \times \frac{1-\eta}{\eta}$$

where η is the efficiency (see the *Typical Operating Characteristics* section).

Calculate the OUT3 and OUT4 power dissipations as follows:

$$P_{D3} = I_{OUT3} \times (V_{PV3} - V_{OUT3})$$

$$P_{D4} = I_{OUT4} \times (V_{PV4} - V_{OUT4})$$

The maximum junction temperature of the MAX16922 is +150°C. The junction-to-case thermal resistance (θ_{JC}) of the MAX16922 is 2.7°C/W.

When mounted on a single-layer PCB, the junction to ambient thermal resistance (θ_{JA}) is approximately 48°C/W. Mounted on a multilayer PCB, θ_{JA} is approximately 32°C/W. Calculate the junction temperature of the MAX16922 as follows:

$$T_J = T_A \times P_D \times \theta_{JA}$$

where T_A is the maximum ambient temperature. Make sure the calculated value of T_J does not exceed the +150°C maximum.

PCB Layout

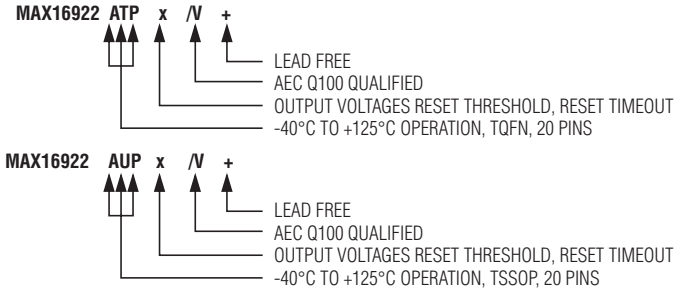
High-switching frequencies and relatively large peak currents make PCB layout a very important aspect of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Connect the input capacitors as close as possible to the PV_ and ground. Connect the inductor and output capacitors as close as possible to the device and keep the traces short, direct, and wide to minimize the current loop area.

The OUTS_ feedback connections are sensitive to inductor magnetic field interference so route these traces away from the inductors and noisy traces such as LX_.

Connect GND_ and PGND2 to the ground plane. Connect the exposed paddle to the ground plane with multiple vias to help conduct heat away from the device.

Refer to the MAX16922 evaluation kit for a PCB layout example.

Selector Guide



PART NUMBER SUFFIX*	OUT1 VOLTAGE (V)	OUT2 VOLTAGE (V)	OUT3 VOLTAGE (V)	OUT4 VOLTAGE (V)	OUT1 RESET THRESHOLD (%)	RESET TIMEOUT (ms)	BST REFRESH LOAD ENABLE
A	5.00	2.70	3.30	1.0	90	14.9	On
B	5.00	1.20	1.80	3.3	90	14.9	On
C	5.00	3.30	1.20	3.0	90	14.9	On
D	3.6	1.2	3.3	3.3	90	14.9	Off
E	5.00	3.30	2.50	1.80	90	14.9	On
F	5.00	1.20	3.15	3.00	90	14.9	On
G	3.30	Off	2.80	1.80	90	14.9	On
H	3.30	1.20	2.50	1.80	90	14.9	Off
I	3.30	1.20	2.85	1.80	90	14.9	Off
J	3.80	3.30	2.50	1.20	90	14.9	Off
K	3.30	2.20	1.60	1.80	90	14.9	On

**Other standard versions may be available. Contact factory for availability.*

2.2MHz, Dual, Step-Down DC-DC Converters, Dual LDOs, and RESET

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2055+4	**21-0140**	**90-0009**
20 TSSOP-EP	U20E+1	**21-0108**	**90-0114**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/09	Initial release	—
1	5/10	Updated *Absolute Maximum Ratings*, *Electrical Characteristics*, *Typical Operating Characteristics*, *Dropout*, and *Power-On Sequence* sections	1, 2, 4, 6, 11, 13
2	10/10	Added a new voltage trim option (I) to the *Selector Guide*	15
3	11/10	Added a new voltage trim option (J) to the *Selector Guide*	15
4	4/11	Added a new voltage trim option (K) to the *Selector Guide*	15
5	1/12	Updated the *Functional Diagram* to eliminate the PWM signal on OUT1 and changed PV2 polarized capacitor to an unpolarized capacitor	8

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