

## 2.5Gbps High Sensitivity Transimpedance Amplifier

### Features

- -29dBm Sensitivity
- Up to 2.5Gbps (NRZ) data rates
- 150nA rms typical input referred noise
- Automatic gain control of output over full input range
- Flexible bond pad layout and output signal inversion for simple ROSA layout
- Received Signal Strength Indicator output
- -40 to +95°C operating temperature range

### Applications

- Telecom Infrastructure OC48
- GPON Optical Network Unit (ONU)
- 2.5GEPON

### Description

The PHY1097 is a transimpedance amplifier designed for use within small form factor fibre optic modules targeted at Gigabit capable Passive Optical Network (GPON) applications.

Working from a 3.3V power supply the PHY1097 integrates a low noise transimpedance amplifier, with a typical differential transimpedance of 25k $\Omega$ , an AGC and an output stage.

The RSSI pad can be used to implement a signal strength monitor circuit. This is designed to sink or source a current equal to the photodiode current for ease of interfacing.

Sensitivity of -29dBm can be achieved at 2.5Gbps.

The PHY1097 is available in die form for mounting on a header to create a ROSA when combined with suitable optics and photo-detector diode.

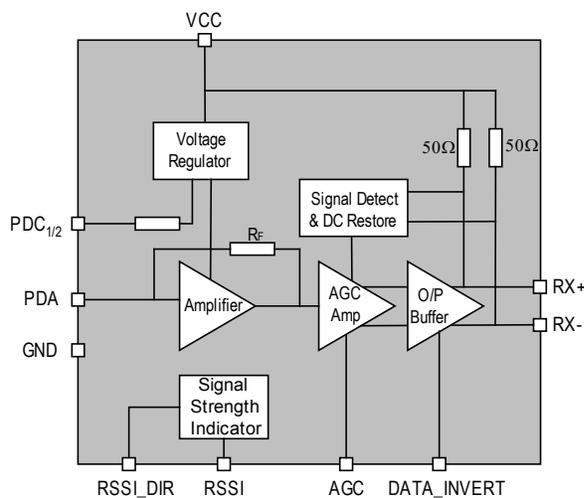


Figure 1: Outline block diagram

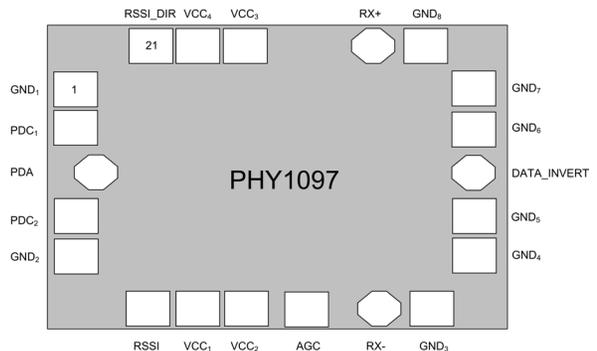


Figure 2: Device pad layout

# 1 Ordering Information

Part Number	Description	Package
PHY1097-03DS-WR	2.5G TIA	Bare die in wafer pack
PHY1097-03DS-FR	2.5G TIA	Film on 10" wafer ring
PHY1097-03DS-QR	2.5G TIA	Film on quarter 8" wafer ring

# 2 Pad Description

Number	Name	Type	Description
1	GND <sub>1</sub>	PWR	Connect to Analog Ground
2	PDC <sub>1</sub>	Analog	Regulated Power supply to Photodiode Cathode
3	PDA	Analog	Connect to Photodiode anode, input to TIA stage
4	PDC <sub>2</sub>	Analog	Regulated Power supply to Photodiode Cathode
5	GND <sub>2</sub>	PWR	Connect to Analog Ground
6	RSSI	Analog Out	Received Signal Strength output. Sources current equal to PD current
7	VCC <sub>1</sub>	PWR	3.3 Volt Power supply connection
8	VCC <sub>2</sub>	PWR	3.3 Volt Power supply connection
9	RX-	Analog Out	Differential Analog Output pair with RX+
10	GND <sub>3</sub>	GND	Connect to Analog Ground
11	GND <sub>4</sub>	GND	Connect to Analog Ground
12	GND <sub>5</sub>	GND	Connect to Analog Ground
13	DATA_INVERT	Analog Input	Inverts polarity of data output pins RX+ and RX-
14	GND <sub>6</sub>	GND	Connect to Analog Ground
15	GND <sub>7</sub>	GND	Connect to Analog Ground
16	GND <sub>8</sub>	GND	Connect to Analog Ground
17	RX+	Analog Out	Differential Analog Output pair with RX-
18	AGC	Analog	Disables AGC amplifier function when connected to GND
19	VCC <sub>3</sub>	PWR	3.3 Volt Power supply connection
20	VCC <sub>4</sub>	PWR	3.3 Volt Power supply connection
21	RSSI_DIR	Analog Input	Selects whether RSSI output is a current sink or source. Open circuit is a current sink, connect to Ground for current source

## 3 Device Specifications

### 3.1 Absolute Maximum Ratings

Exceeding these limits may cause permanent damage. Correct operation under these conditions is not implied. Extended periods of operation under these conditions may affect device reliability.

Parameter	Conditions	Min	Max	Unit
Supply voltage		-0.5	4.0	V
Maximum Voltage on signal pins	Vcc within the maximum rating conditions	-0.5	Vcc + 0.5V	V
Device Operating Temperature	Measured on Die		+115	°C
Storage Temperature		-55	150	°C
Die Attach Temperature	For a maximum 30 secs		400	°C
PDA Input Current	VCC > 3.0V		3.0	mA
PDA Input current	VCC < 3.0V		2.0	mA
ESD Performance	Human Body Model (Excluding PDA pin)	2.0		kV
	Human Body Model (PDA pin)	0.5		kV

### 3.2 Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage		3.0	3.3	3.6	V
Current consumption	Including output termination	40	48	60	mA
Ambient Operating temperature		-40		95	°C
Photodiode Capacitance	Photodiode bias voltage 1.8V			1.0	pF

### 3.3 Parametric Performance

All typical parameters are tested at 25°C and at VCC = 3.3V

Parameter	Conditions	Min	Typ	Max	Unit
High-speed data input rate	C <sub>IN</sub> = 0.5pF			2.5	Gbps
Sensitivity	C <sub>IN</sub> = 0.5pF, Responsivity = 0.9A/W, BER = 10 <sup>-10</sup> , ER = 10dB		-29		dBm
Input referred noise	C <sub>IN</sub> = 0.5pF, Measured into a 1.866GHz, 4 <sup>th</sup> order Bessel filter.		150	200	nA rms
Small Signal Bandwidth (-3dB)	Cpd = 0.35pF, -3dB point at -27dBm, Guaranteed by characterization of reference ROSA assemblies.	1400	1700		MHz
Low frequency cut-off	Relative to 100MHz		25	35	kHz
Gain Variation with Frequency	1MHz to 1250MHz, with respect to 100MHz Input current < 500µA pp		±2		dB
Differential Output Swing <sup>1</sup>	Input current > 16µA pp 100Ω differential load, 2.5Gbps	320	400	480	mVp-p

Parameter	Conditions	Min	Typ	Max	Unit
Transimpedance (differential)	Input current $<8\mu\text{A}_{p-p}$ , $100\Omega$ load	20k	25k	30k	$\Omega$
Deterministic Jitter	K28.5 Pattern		50	100	mUI <sub>p-p</sub>
Overshoot	$2^7$ -1PRBS (wrt to average 0/1 level)			$\pm 15$	%
Undershoot	$2^7$ -1PRBS (wrt average 0/1 level)			$\pm 15$	%
Input Overload, a.c.	DJ within spec, $ER = \infty$	4.4			mApp
Input Overload d.c.	DJ within spec, $TJ = 95^\circ\text{C}$	2.2			mA
AGC settling time				50	$\mu\text{s}$
Output resistance	Differential $V_{OUT+}$ to $V_{OUT-}$	80	100	120	$\Omega$
Output Common Mode Voltage	Measured relative to VCC	-0.5	-0.37	-0.25	V
Photodiode Cathode Voltage		2.5	2.6	2.7	V
Photodiode Anode Voltage			0.8	1.0	V
RSSI Current Accuracy	Measured relative to photodiode current			$\pm 20$	%
RSSI Compliance Voltage	Current source mode	1.0			V
	Current sink mode			0.8	V
Power Supply Rejection Ratio	100kHz – 4MHz	30	40		dB

## 4 Device Description

The PHY1097 implements a complete analog front end, converting the photo-detector current, which has been modulated by light from an optical fibre, to a differential analog voltage signal.

The PHY1097 also provides a filtered bias current to the photo-detector to increase the level of component integration as well as the signal processing functions.

### 4.1 Photodiode Connection

A PIN Photodiode should be connected to the PHY1097 as shown in Figure 3, using the internal voltage reference to bias the Photodiode. The internal reference supplies a low noise output with high power supply rejection to 4MHz.

The voltage across the photodiode is equal to the power supply voltage,  $V_{pdc}$  minus the base emitter voltage of the input transistor on the PHY1097, equal to  $V_{pda}$ . The anode voltage,  $V_{pda}$  is sensitive to temperature and has a typical value of 0.8V.

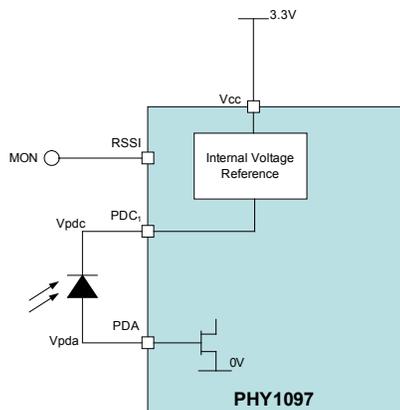


Figure 3 – Photodiode biased by internal voltage regulator

Single ended connection of a PIN photodiode to the PDA input with an external bias supply can produce inconsistent sensitivity and bandwidth operation.

If an Avalanche Photodiode (APD) is to be used this can be connected as shown in figure 4, filtering of the bias voltage must be provided externally to the PHY1097 to avoid damaging the device. The input current applied to the PDA pad with Vcc off (<3.0V) must not exceed the value given in the section 3.1 maximum ratings table, if exceeded damage may occur to the PDA input. The RSSI senses the MPD current from the PDC pad, this is not used in single ended applications such as APD. In this case a current mirror should be included on the APD bias to provide the RSSI current.

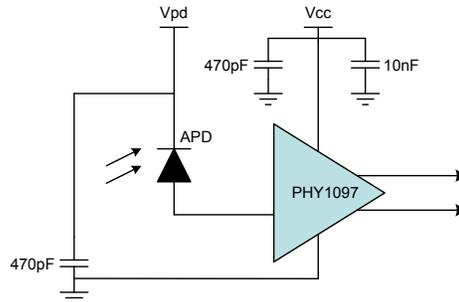


Figure 4 – Connection of an avalanche photodiode

## 4.2 DC Cancellation

The removal of the direct current component of the input signal is necessary to reduce the pulse width distortion for signals with a 50% mark density.

The DC cancellation block provides low frequency feedback using an internally compensated amplifier, removing the need for external compensation capacitors.

## 4.3 Transimpedance Amplifier (TIA)

The transimpedance (current to voltage) stage is a very low noise amplifier with a feedback resistor to set the gain. This stage features automatic gain control, where the transimpedance depends on the output signal level. This ensures that the output does not overload the subsequent stage in the signal path.

An internal voltage regulator is used to power the front-end transimpedance amplifier in order to improve the rejection of power supply noise.

## 4.4 Output Data Polarity

The data polarity pin has an internal 8kΩ pull-up resistor. In normal non-inverting operation, where there is no external connection, the pin pulls to VDD. In this mode an optical '1' gives maximum input current and a voltage '1' on the positive output pin Rx+. Connection of the pad to ground selects an inverted sense output.

## 4.5 Output Gain Stage

The output gain stage features a voltage amplifier, a single ended to differential converter and a supply referenced differential output buffer.

The PHY1097 has a 50Ω single ended output impedance, which is suitable for the majority of applications. For optimum supply-noise rejection, the PHY1097 should be terminated differentially.

## 4.6 Received Signal Strength Indication (RSSI)

The PHY1097 provides a RSSI output which can be used to measure the strength of the received optical signal. The photodiode current is proportional to the received optical power. The PHY1097 generates an output current which is a mirror of the photodiode current at the PDC input and is valid only for differential photodiode connections. The RSSI output is a current sink or a current source.

The direction of current flow is selected by using the RSSI\_DIR bond. Leaving this bond pad unconnected selects a current sink, connecting this bond pad to ground selects a current source.

An alternative method of measuring the received signal power is by using the received Optical Modulation Amplitude (OMA). This method is provided by the PHY2078 integrated burst mode laser driver and post amplifier device.

## 5 Typical Application

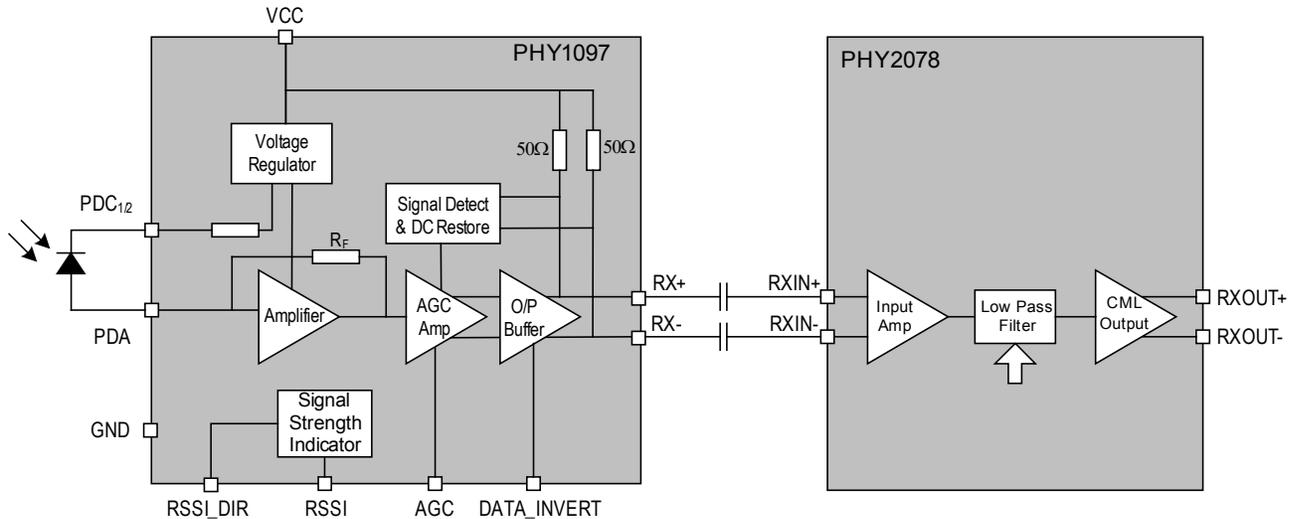


Figure 5 - Typical Application - GPON ONU Receiver path

Figure 5 shows a typical application for the PHY1097. In this application the output of the PHY1097 is connected to the Phyworks PHY2078 PON Laser Driver and Post Amplifier circuit to form the receive path for a fibre optic module.

The PHY2078 provides the receive signal monitoring functions such as loss of signal and converts the input data into a variety of electrical formats.

### 5.1 Layout and Bonding

In order to achieve the best performance it is necessary to minimise noise pickup and to reduce the effects of parasitic components.

Noise is picked up through the signal paths or through the power supply. Noise at the input of the TIA will be amplified and mixed with the wanted signal. This can be a result of noise pickup in the other components connected to the TIA input, such as the photodiode, the capacitors and the bond wires.

Noise picked up in the signal path can be reduced by keeping bond wires short and by making sure the output and input bond wires are not close and are orthogonal to each other,

Power supply noise will be present as a result of the power supply design, the quality of decoupling precautions and pickup in the bond wires.

To effectively de-couple supply rail noise to ground a capacitor may be placed inside the ROSA TO can. This should be placed as close as possible to the VCC pin on the TIA. This reduces the effect of the bond wire inductance.

Noise on the power supply can also be a result of coupling between the TIA output and the power supply. This coupling takes place between the output bond wires and the power supply bond wires. As a result these must also be kept as short as possible and be routed orthogonally to each other.

The PHY1097 provides alternative bonding options through the replication of some device inputs and outputs, allowing a variety of ROSA pin outs to be realised without compromising performance.

For stable operation the ground bonds GND1, GND2, GND4 and GND7 should not be omitted.

## 6 Mechanical Specifications

### 6.1 TO-Can Connections

Top-view: looking into the CD header. The diagrams below show an internal power supply decoupling capacitor and illustrate the optimum bondwire lengths and orientation. The value of the supply de-coupling capacitor should be 250 – 500 pF.

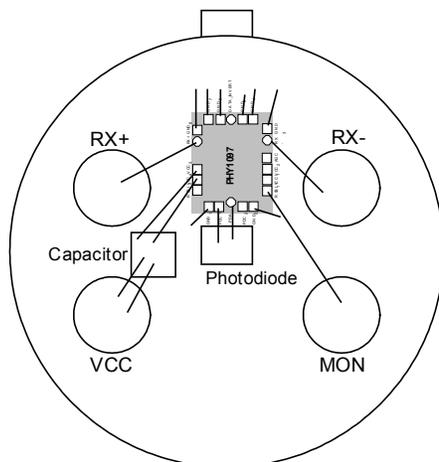


Figure 6 - 5 pin ROSA layout 1

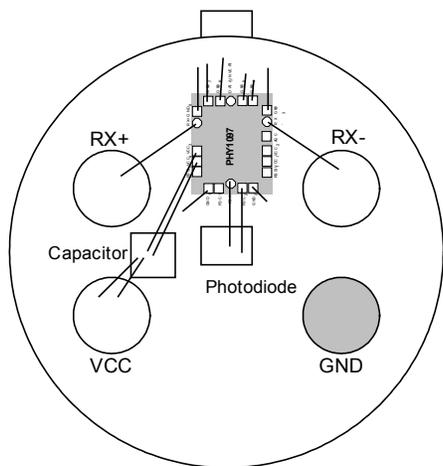


Figure 7 - 4 pin ROSA layout 1

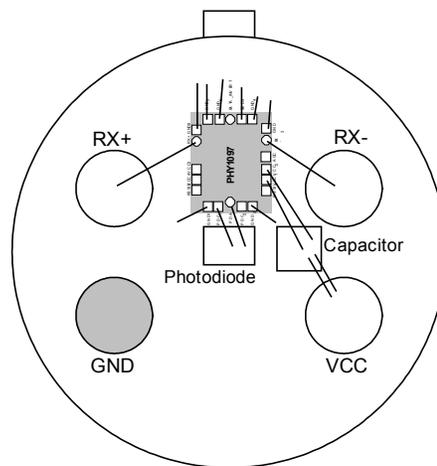


Figure 8 - 4 Pin ROSA layout 2

## 7 Pad Positions and Sizes

Die Size: 1100 $\mu$ m x 900 $\mu$ m

Thickness: 290 $\mu$ m +/- 10  $\mu$ m

Pad Opening: 80 $\mu$ m x 80 $\mu$ m measured between parallel sides

Number	Name	Pad centres	
		X	Y
1	GND <sub>1</sub>	-439.5	221.5
2	PDC <sub>1</sub>	-439.5	113
3	PDA	-412.5	0
4	PDC <sub>2</sub>	-439.5	-113
5	GND <sub>2</sub>	-439.5	-221.5
6	RSSI	-320.095	-339.5
7	VCC <sub>1</sub>	-219.5	-339.5
8	VCC <sub>2</sub>	-121.5	-339.5
9	AGC	55.09	-339.5
10	RX-	222.1	-339.5
11	GND <sub>3</sub>	321.5	-339.5
12	GND <sub>4</sub>	439.5	-221.5
13	GND <sub>5</sub>	439.5	-123.5
14	DATA_INVERT	439.5	0
15	GND <sub>6</sub>	439.5	123.5
16	GND <sub>7</sub>	439.5	221.5
17	GND <sub>8</sub>	321.5	339.5
18	RX+	222.1	339.5
19	VCC <sub>3</sub>	-121.5	339.5
20	VCC <sub>4</sub>	-219.5	339.5
21	RSSI_DIR	-320.095	339.5

Table 1: PHY1097 pad coordinates

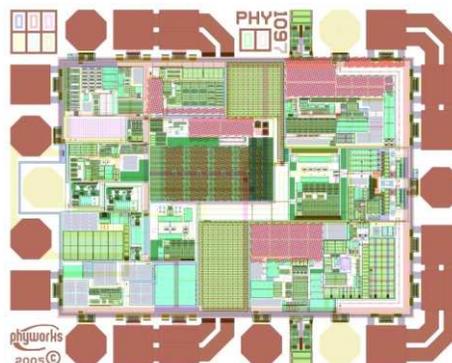


Figure 9: PHY1097 Die image

## 8 Contact Information

For technical support, contact Maxim at [www.maxim-ic.com/support](http://www.maxim-ic.com/support).

### Disclaimer

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