



# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

MAX5974E/MAX5974F

## General Description

The MAX5974E/MAX5974F provide control for wide-input-voltage, current-mode PWM, nonisolated, synchronous flyback converters in Power-over-Ethernet (PoE) powered device (PD) applications. The MAX5974E is well-suited for universal or telecom input range, while the MAX5974F also accommodates low input voltage down to 8.4V.

The devices include several features to enhance supply efficiency, including a synchronous MOSFET driver output. The AUX driver drives an output synchronous rectifier to lower conduction losses. Programmable dead time between the AUX and main driver allows for zero-voltage switching (ZVS). Under light-load conditions, the devices reduce the switching frequency (frequency foldback) to reduce switching losses.

An internal error amplifier with a 1% reference eliminates the need for an external shunt regulator and optocoupler.

The programmable frequency dithering feature provides low-EMI, spread-spectrum operation.

The MAX5974E/MAX5974F are available in 16-pin TQFN-EP packages and are rated for operation over the -40°C to +85°C temperature range.

## Applications

PoE IEEE® 802.3af/at Powered Devices  
High-Power PD (Beyond the 802.3af/at Standard)  
IP Phones  
Wireless Access Nodes  
Security Cameras

## Features

- ◆ Peak Current-Mode Control, Synchronous Flyback PWM Controller
- ◆ Synchronous MOSFET Driver Output
- ◆ Internal 1% Error Amplifier Eliminates Shunt Regulator and Optocoupler
- ◆ 100kHz to 600kHz Programmable  $\pm 8\%$  Switching Frequency, Synchronization Up to 1.2MHz
- ◆ Programmable Frequency Dithering for Low-EMI, Spread-Spectrum Operation
- ◆ Programmable Dead Time, PWM Soft-Start, Current Slope Compensation
- ◆ Programmable Feed-Forward Maximum Duty-Cycle Clamp, 80% Maximum Limit
- ◆ Frequency Foldback for High-Efficiency Light-Load Operation
- ◆ Internal Bootstrap UVLO with Large Hysteresis
- ◆ 100 $\mu$ A (typ) Startup Supply Current
- ◆ Fast Cycle-by-Cycle Peak Current-Limit, 35ns Typical Propagation Delay
- ◆ 115ns Current-Sense Internal Leading-Edge Blanking
- ◆ Output Short-Circuit Protection with Hiccup Mode
- ◆ Internal 18V Zero Clamp on Supply Input
- ◆ 3mm x 3mm, Lead-Free, 16-Pin TQFN-EP

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	UVLO THRESHOLD (V)	TOP MARK
MAX5974EETE+	-40°C to +85°C	16 TQFN-EP*	16	+AIR
MAX5974FETE+	-40°C to +85°C	16 TQFN-EP*	8.4	+AIS

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

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## ABSOLUTE MAXIMUM RATINGS

IN to GND ( $V_{EN} = 0V$ )	-0.3V to +26V
EN, NDRV, AUXDRV to GND	-0.3V to ( $V_{IN} + 0.3V$ )
RT, DT, FFB, COMP, SS, DCLMP, DITHER/SYNC to GND	-0.3V to +6V
FB to GND (MAX5974E only)	-6V to +6V
FB to GND (MAX5974F only)	-0.3V to +6V
CS, CSSC to GND	-0.8V to +6V
PGND to GND	-0.3V to +0.3V
Maximum Input/Output Current (continuous)	
NDRV, AUXDRV	100mA
NDRV, AUXDRV (pulsed for less than 100ns)	$\pm 1A$

Continuous Power Dissipation ( $T_A = +70^\circ C$ )	
16-Pin TQFN (derate 20.8mW/ $^\circ C$ above $+70^\circ C$ )	1666mW
Operating Temperature Range	$-40^\circ C$ to $+85^\circ C$
Maximum Junction Temperature	$+150^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (soldering, 10s)	$+300^\circ C$
Soldering Temperature (reflow)	$+260^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ )	$48^\circ C/W$
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ )	$7^\circ C/W$

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

## ELECTRICAL CHARACTERISTICS

( $V_{IN} = 12V$  (for MAX5974E, bring  $V_{IN}$  up to 17V for startup),  $V_{CS} = V_{CSSC} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}$ ,  $V_{EN} = +2V$ ,  $NDRV = AUXDRV = SS = COMP =$  unconnected,  $R_{RT} = 34.8k\Omega$ ,  $R_{DT} = 25k\Omega$ ,  $C_{IN} = 1\mu F$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>UNDERVOLTAGE LOCKOUT/STARTUP (IN)</b>							
Bootstrap UVLO Wakeup Level	$V_{INUVR}$	$V_{IN}$ rising	MAX5974E	15.4	16	16.5	V
			MAX5974F	8	8.4	8.85	
Bootstrap UVLO Shutdown Level	$V_{INUVF}$	$V_{IN}$ falling	6.65	7	7.35	V	
IN Clamp Voltage	$V_{IN\_CLAMP}$	$I_{IN} = 2mA$ (sinking)	17	18.5	20	V	
IN Supply Current in Undervoltage Lockout	$I_{START}$	$V_{IN} = +15V$ (for MAX5974E); $V_{IN} = +7.5V$ (for MAX5974F), when in bootstrap UVLO		100	150	$\mu A$	
IN Supply Current After Startup	$I_C$	$V_{IN} = +12V$		1.8	3	mA	
<b>ENABLE (EN)</b>							
Enable Threshold	$V_{ENR}$	$V_{EN}$ rising	1.17	1.215	1.26	V	
	$V_{ENF}$	$V_{EN}$ falling	1.09	1.14	1.19		
Input Current	$I_{EN}$				1	$\mu A$	
<b>OSCILLATOR (RT)</b>							
RT Bias Voltage	$V_{RT}$			1.23		V	
NDRV Switching Frequency Range	$f_{sw}$		100		600	kHz	

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## ELECTRICAL CHARACTERISTICS (continued)

(VIN = 12V (for MAX5974E, bring VIN up to 17V for startup), VCS = VCSSC = VDITHER/SYNC = VFB = VFFB = VDCLMP = VGND, VEN = +2V, NDRV = AUXDRV = SS = COMP = unconnected, RRT = 34.8kΩ, RDT = 25kΩ, CIN = 1μF, TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NDRV Switching Frequency Accuracy			-8		+8	%
Maximum Duty Cycle	DMAX	fsw = 250kHz	79	80	82	%
<b>SYNCHRONIZATION (SYNC)</b>						
Synchronization Logic-High Input	VIH-SYNC		2.91			V
Synchronization Pulse Width				50		ns
Synchronization Frequency Range	fSYNCIN		1.1 x fsw		2 x fsw	kHz
Maximum Duty Cycle During Synchronization			DMAX x fSYNC/ fsw			%
<b>DITHERING RAMP GENERATOR (DITHER)</b>						
Charging Current		VDITHER = 0V	45	50	55	μA
Discharging Current		VDITHER = 2.2V	43	50	57	μA
Ramp's High Trip Point				2		V
Ramp's Low Trip Point				0.4		V
<b>SOFT-START AND RESTART (SS)</b>						
Charging Current	ISS-CH		9.5	10	10.5	μA
Discharging Current	ISS-D	VSS = 2V, normal shutdown	0.65	1.34	2	mA
	ISS-DH	(VEN < VENF or VIN < VINUVF), VSS = 2V, hiccup mode discharge for tRSTRT (Note 3)	1.6	2	2.4	μA
Discharge Threshold to Disable Hiccup and Restart	VSS-DTH			0.15		V
Minimum Restart Time During Hiccup Mode	tRSTRT-MIN			1024		Clock Cycles
Normal Operating High Voltage	VSS-HI			5		V
Duty-Cycle Control Range	VSS-DMAX	DMAX (typ) = (VSS-DMAX/2.43V)	0		2	V
<b>DUTY-CYCLE CLAMP (DCLMP)</b>						
DCLMP Input Current	IDCLMP	VDCLMP = 0 to 5V	-100	0	+100	nA
Duty-Cycle Control Range	VDCLMP-R	VDCLMP = 0.5V	73	75.4	77.5	%
		VDCLMP = 1V	54	56	58	
		VDCLMP = 2V	14.7	16.5	18.3	
<b>NDRV DRIVER</b>						
Pulldown Impedance	RNDRV-N	INDRV (sinking) = 100mA		1.9	3.4	Ω
Pullup Impedance	RNDRV-P	INDRV (sourcing) = 50mA		4.7	8.3	Ω
Peak Sink Current				1		A
Peak Source Current				0.65		A
Fall Time	tNDRV-F	CNDRV = 1nF		14		ns
Rise Time	tNDRV-R	CNDRV = 1nF		27		ns

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = 12V$  (for MAX5974E, bring  $V_{IN}$  up to 17V for startup),  $V_{CS} = V_{CSSC} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}$ ,  $V_{EN} = +2V$ ,  $NDRV = AUXDRV = SS = COMP =$  unconnected,  $R_{RT} = 34.8k\Omega$ ,  $R_{DT} = 25k\Omega$ ,  $C_{IN} = 1\mu F$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>AUXDRV DRIVER</b>							
Pulldown Impedance	$R_{AUX-N}$	$I_{AUXDRV}$ (sinking) = 50mA		4.3	7.7	$\Omega$	
Pullup Impedance	$R_{AUX-P}$	$I_{AUXDRV}$ (sourcing) = 25mA		10.6	18.9	$\Omega$	
Peak Sink Current				0.5		A	
Peak Source Current				0.3		A	
Fall Time	$t_{AUX-F}$	$C_{AUXDRV} = 1nF$		24		ns	
Rise Time	$t_{AUX-R}$	$C_{AUXDRV} = 1nF$		45		ns	
<b>DEAD-TIME PROGRAMMING (DT)</b>							
DT Bias Voltage	$V_{DT}$			1.215		V	
NDRV to AUXDRV Delay (Dead Time)	$t_{DT}$	From NDRV falling to AUXDRV rising	$R_{DT} = 10k\Omega$	40			ns
			$R_{DT} = 100k\Omega$	300	350	410	
		From AUXDRV falling to NDRV rising	$R_{DT} = 10k\Omega$	40			ns
			$R_{DT} = 100k\Omega$	310	360	420	
<b>CURRENT-LIMIT COMPARATOR (CS)</b>							
Cycle-by-Cycle Peak Current-Limit Threshold	$V_{CS-PEAK}$		375	393	410	mV	
Number of Consecutive Peak Current-Limit Events to Hiccup	$N_{HICCUP}$			8		Events	
Current-Sense Leading-Edge Blanking Time	$t_{CS-BLANK}$	From NDRV rising edge		115		ns	
Propagation Delay from Comparator Input to NDRV	$t_{PDCS}$	From CS rising (10mV overdrive) to NDRV falling (excluding leading-edge blanking)		35		ns	
Minimum On-Time	$t_{ON-MIN}$		100	150	200	ns	
<b>SLOPE COMPENSATION (CSSC)</b>							
Slope Compensation Current Ramp Height		Current ramp's peak added to CSSC input per switching cycle	47	52	58	$\mu A$	
<b>PWM COMPARATOR</b>							
Comparator Offset Voltage	$V_{PWM-OS}$	$V_{COMP} - V_{CSSC}$	1.35	1.7	2	V	
Current-Sense Gain	$A_{CS-PWM}$	$\Delta V_{COMP}/\Delta V_{CSSC}$ (Note 4)	3.1	3.33	3.6	V/V	
Current-Sense Leading-Edge Blanking Time	$t_{CSSC-BLANK}$	From NDRV rising edge		115		ns	
Comparator Propagation Delay	$t_{PWM}$	Change in $V_{CSSC} = 10mV$ (including internal leading-edge blanking)		150		ns	

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MAX5974E/MAX5974F

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = 12V$  (for MAX5974E, bring  $V_{IN}$  up to 17V for startup),  $V_{CS} = V_{CSCS} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}$ ,  $V_{EN} = +2V$ ,  $NDRV = AUXDRV = SS = COMP =$  unconnected,  $R_{RT} = 34.8k\Omega$ ,  $R_{DT} = 25k\Omega$ ,  $C_{IN} = 1\mu F$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>ERROR AMPLIFIER</b>						
FB Reference Voltage	$V_{REF}$	$V_{FB}$ when $I_{COMP} = 0$ , $V_{COMP} = 2.5V$	1.202	1.215	1.227	V
FB Input Bias Current	$I_{FB}$	$V_{FB} = 0$ to 1.75V	-500		+100	nA
Voltage Gain	$A_{EAMP}$			80		dB
Transconductance	$g_M$		1.8	2.66	3.5	mS
Transconductance Bandwidth	BW	Open loop (typical gain = 1) -3dB frequency		30		MHz
Source Current		$V_{FB} = 1V$ , $V_{COMP} = 2.5V$	300	375	455	$\mu A$
Sink Current		$V_{FB} = 1.75V$ , $V_{COMP} = 1V$	300	375	455	$\mu A$
<b>FREQUENCY FOLDBACK (FFB)</b>						
$V_{CSAVG}$ -to-FFB Comparator Gain				10		V/V
FFB Bias Current	$I_{FFB}$	$V_{FFB} = 0V$ , $V_{CS} = 0V$ (not in FFB mode)	26	30	33	$\mu A$
NDRV Switching Frequency During Foldback	$f_{SW-FB}$			$f_{SW}/2$		kHz

**Note 2:** All devices are 100% production tested at  $T_A = +25^\circ C$ . Limits over temperature are guaranteed by design.

**Note 3:** See the *Output Short-Circuit Protection with Hiccup Mode* section.

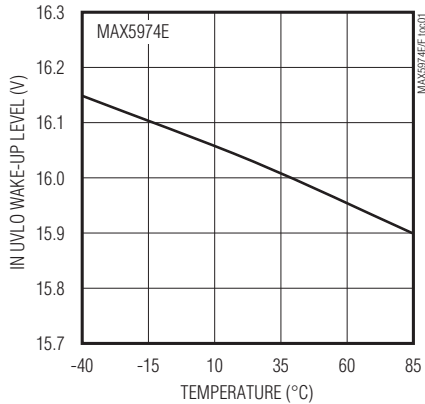
**Note 4:** The parameter is measured at the trip point of latch with  $V_{FB} = 0V$ . Gain is defined as  $\Delta V_{COMP}/\Delta V_{CSCS}$  for  $0.15V < \Delta V_{CSCS} < 0.25V$ .

# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

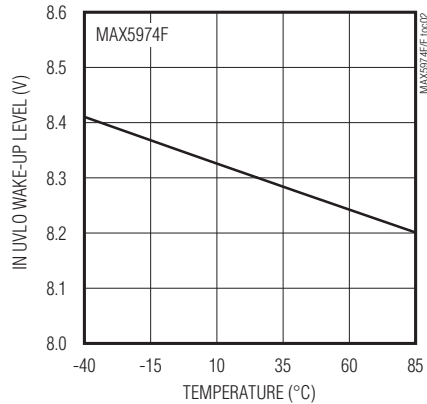
## Typical Operating Characteristics

( $V_{IN} = 12V$  (for MAX5974E, bring  $V_{IN}$  up to 17V for startup),  $V_{CS} = V_{CSSC} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}$ ,  $V_{EN} = 2V$ ,  $NDRV = AUXDRV = SS = COMP =$  unconnected,  $R_{RT} = 34.8k\Omega$ ,  $R_{DT} = 25k\Omega$ , unless otherwise noted.)

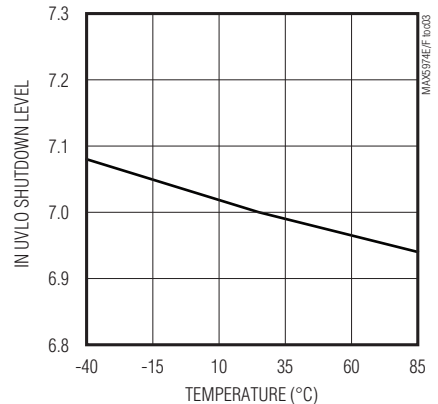
**IN UVLO WAKE-UP LEVEL vs. TEMPERATURE**



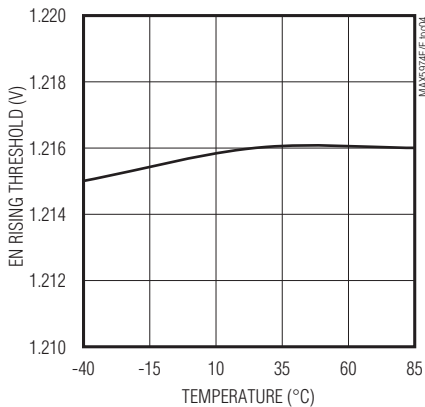
**IN UVLO WAKE-UP LEVEL vs. TEMPERATURE**



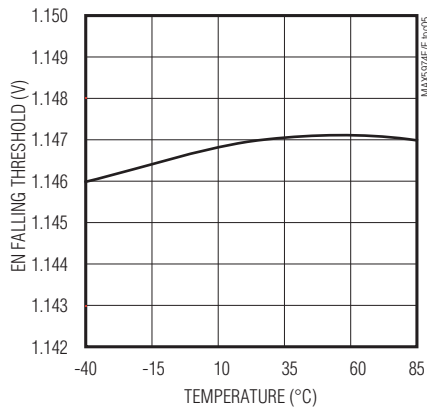
**IN UVLO SHUTDOWN LEVEL vs. TEMPERATURE**



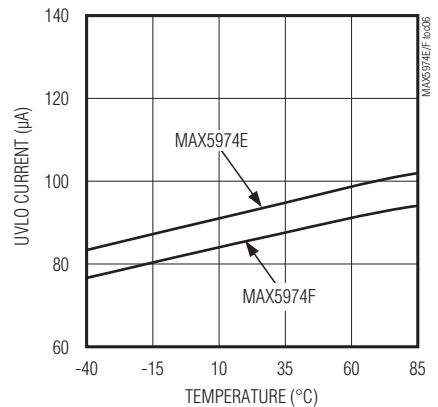
**EN RISING THRESHOLD vs. TEMPERATURE**



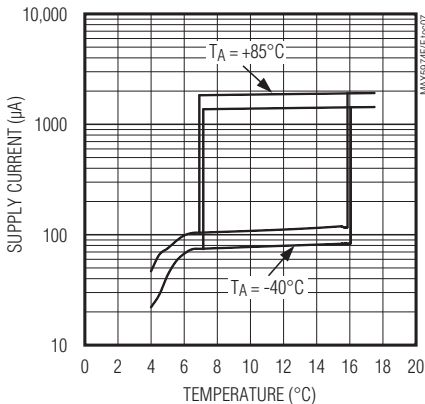
**EN FALLING THRESHOLD vs. TEMPERATURE**



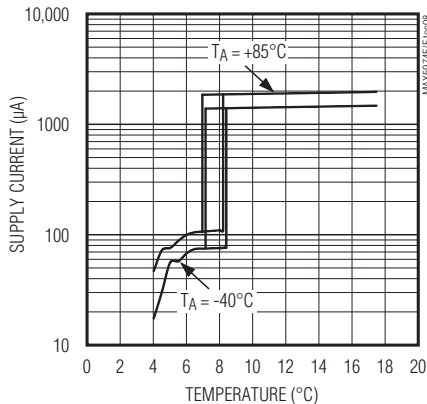
**UVLO SHUTDOWN CURRENT vs. TEMPERATURE**



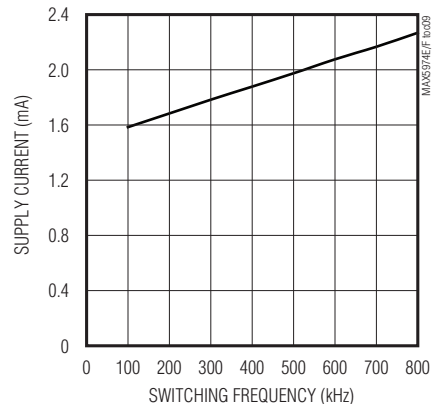
**SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5974E)**



**SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5974F)**



**SUPPLY CURRENT vs. SWITCHING FREQUENCY**



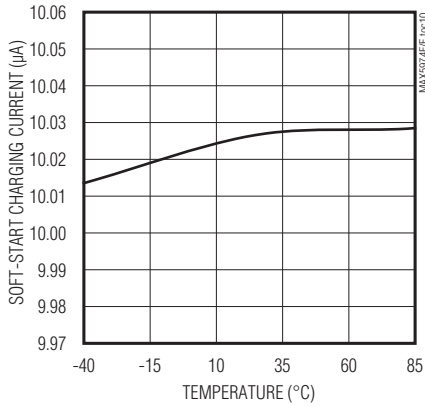
# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

## Typical Operating Characteristics (continued)

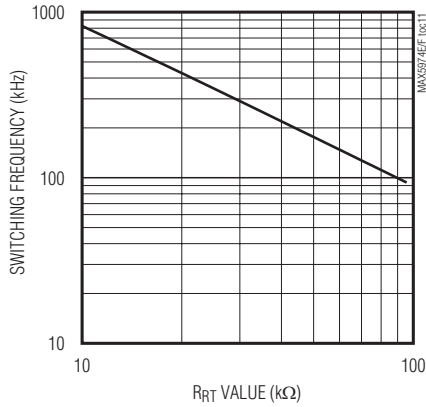
( $V_{IN} = 12V$  (for MAX5974E, bring  $V_{IN}$  up to 17V for startup),  $V_{CS} = V_{CSSC} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}$ ,  $V_{EN} = 2V$ ,  $NDRV = AUXDRV = SS = COMP =$  unconnected,  $R_{RT} = 34.8k\Omega$ ,  $R_{DT} = 25k\Omega$ , unless otherwise noted.)

MAX5974E/MAX5974F

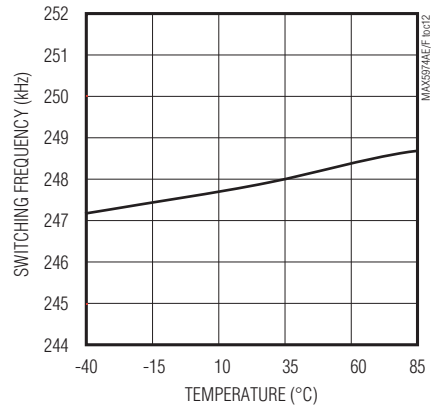
**SOFT-START CHARGING CURRENT vs. TEMPERATURE**



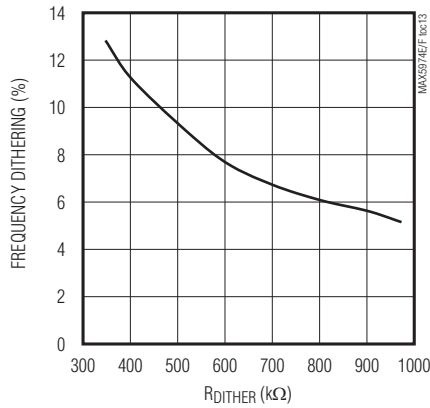
**SWITCHING FREQUENCY vs.  $R_{RT}$  VALUE**



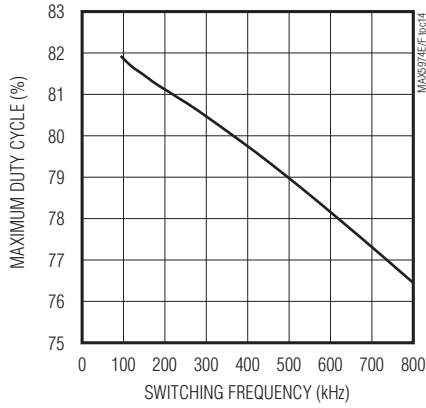
**SWITCHING FREQUENCY vs. TEMPERATURE**



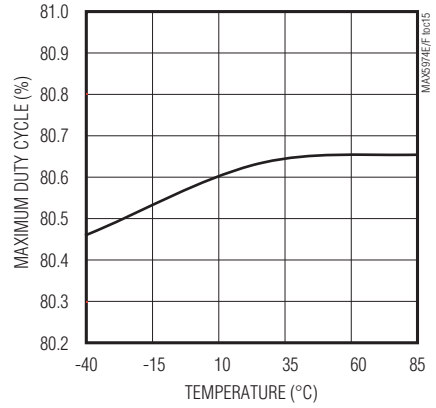
**FREQUENCY DITHERING vs.  $R_{DITHER}$**



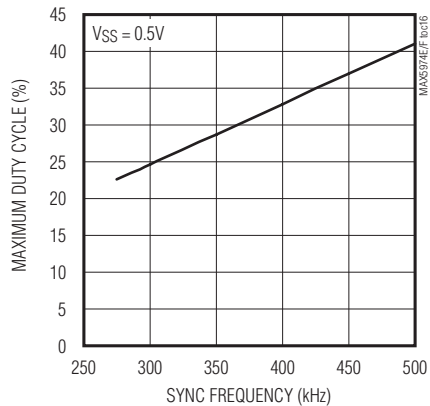
**MAXIMUM DUTY CYCLE vs. SWITCHING FREQUENCY**



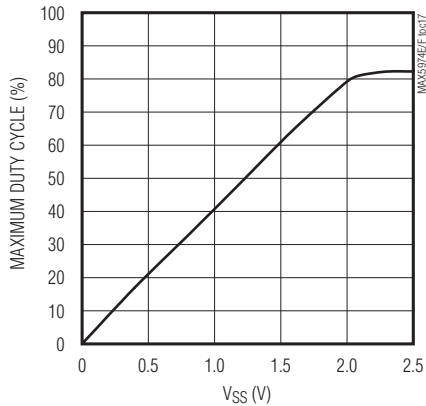
**MAXIMUM DUTY CYCLE vs. TEMPERATURE**



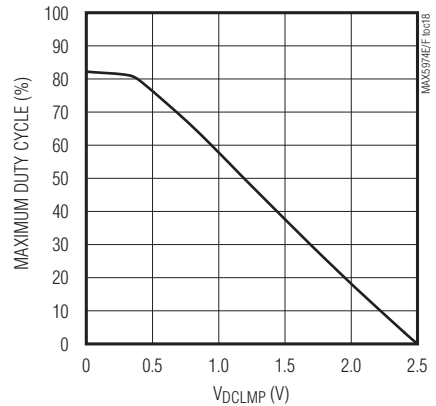
**MAXIMUM DUTY CYCLE vs. SYNC FREQUENCY**



**MAXIMUM DUTY CYCLE vs.  $V_{SS}$**



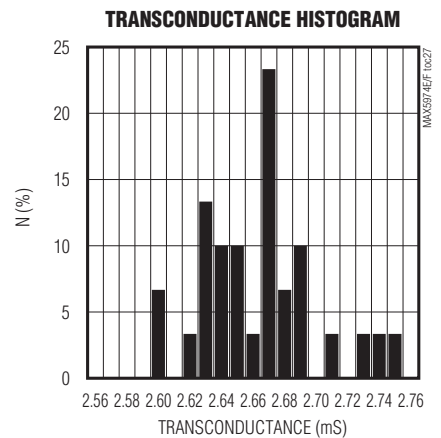
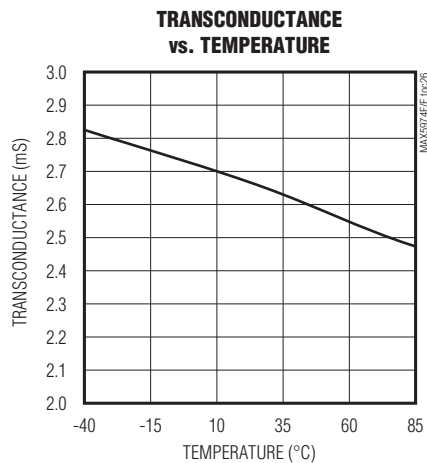
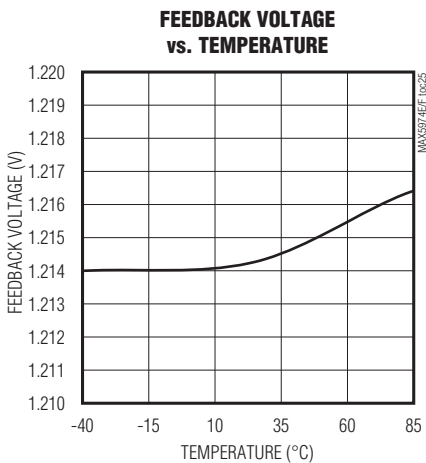
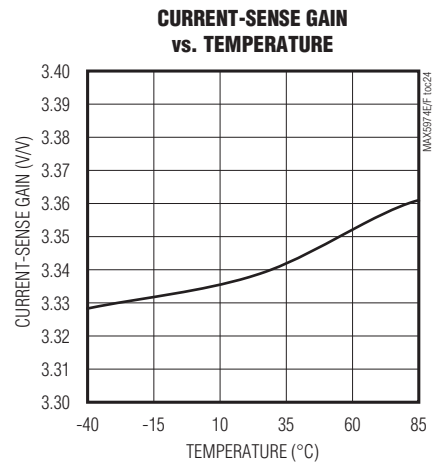
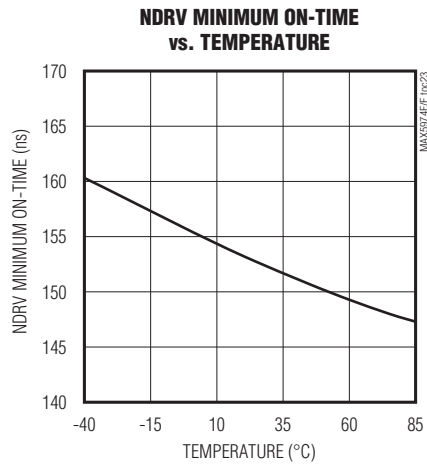
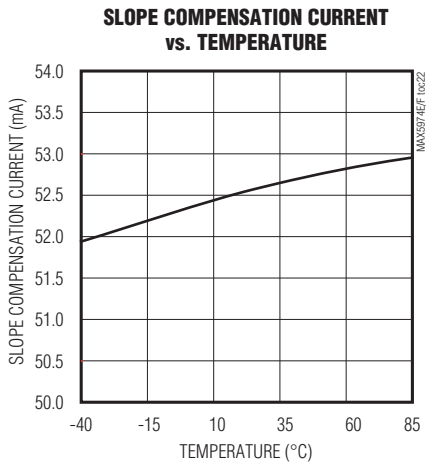
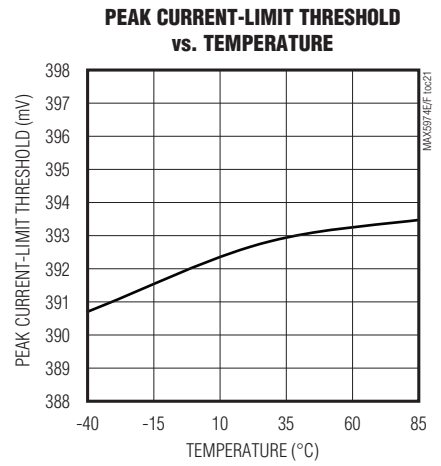
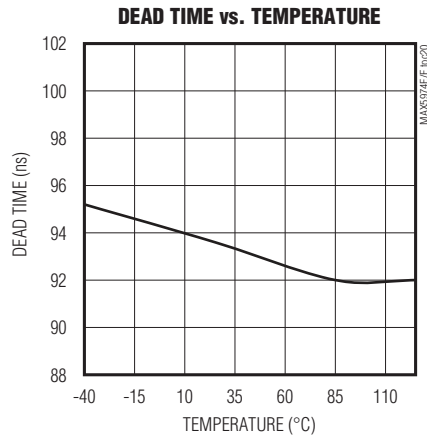
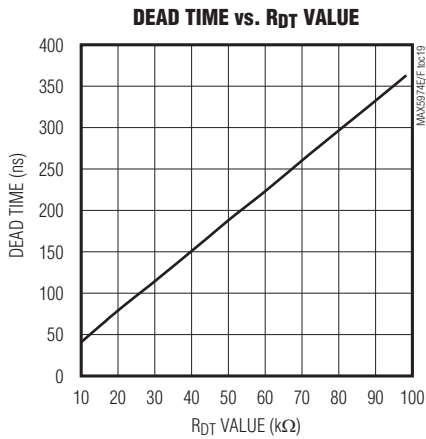
**MAXIMUM DUTY CYCLE vs.  $V_{DCLMP}$**



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## Typical Operating Characteristics (continued)

( $V_{IN} = 12V$  (for MAX5974E, bring  $V_{IN}$  up to 17V for startup),  $V_{CS} = V_{CSSC} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}$ ,  $V_{EN} = 2V$ ,  $NDRV = AUXDRV = SS = COMP =$  unconnected,  $R_{RT} = 34.8k\Omega$ ,  $R_{DT} = 25k\Omega$ , unless otherwise noted.)



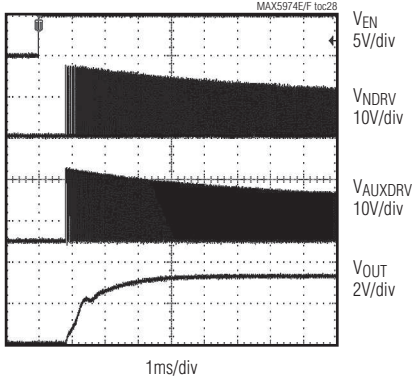
# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

## Typical Operating Characteristics (continued)

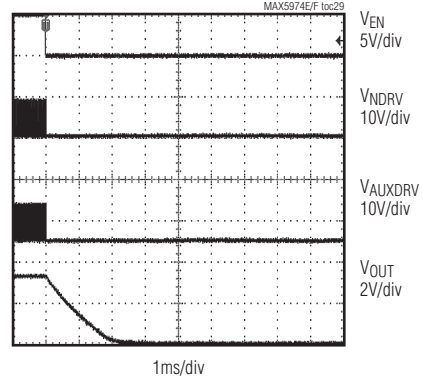
( $V_{IN} = 12V$  (for MAX5974E, bring  $V_{IN}$  up to 17V for startup),  $V_{CS} = V_{CSSC} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}$ ,  $V_{EN} = 2V$ ,  $NDRV = AUXDRV = SS = COMP =$  unconnected,  $R_{RT} = 34.8k\Omega$ ,  $R_{DT} = 25k\Omega$ , unless otherwise noted.)

MAX5974E/MAX5974F

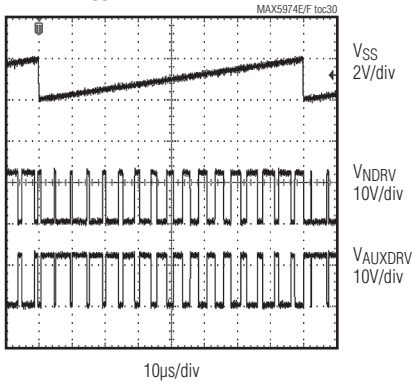
**ENABLE RESPONSE**



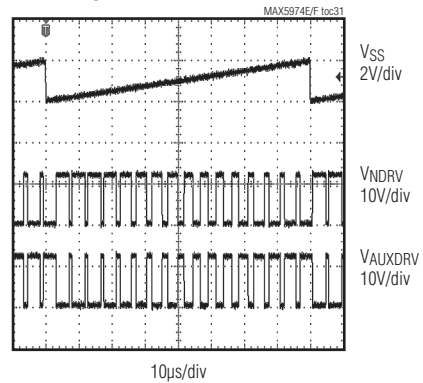
**SHUTDOWN RESPONSE**



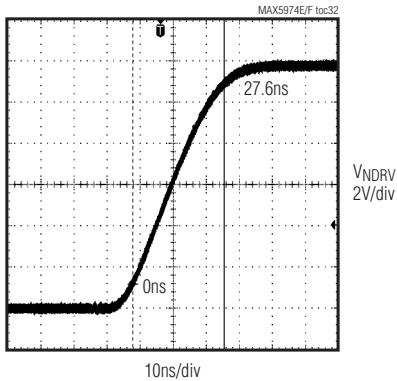
**V<sub>SS</sub> RAMP RESPONSE**



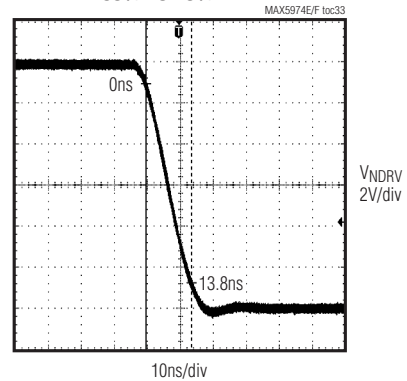
**V<sub>DCLMP</sub> RAMP RESPONSE**



**NDRV 10% TO 90% RISE TIME**



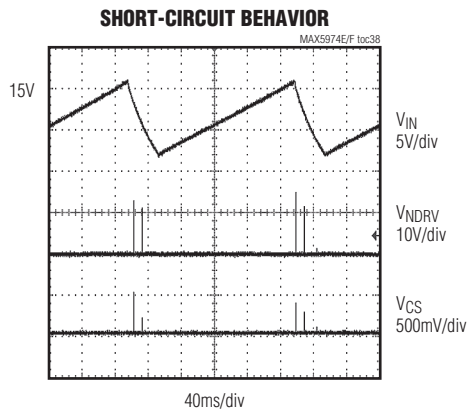
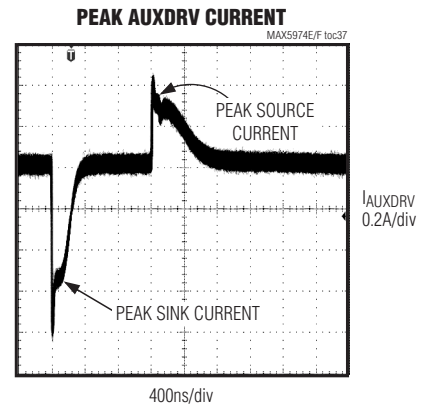
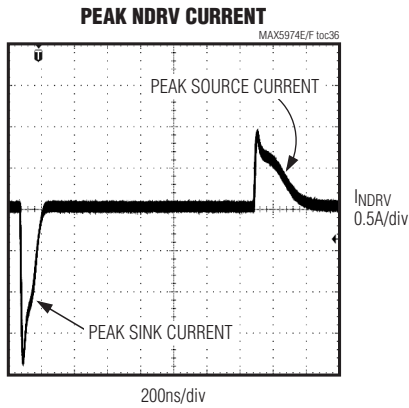
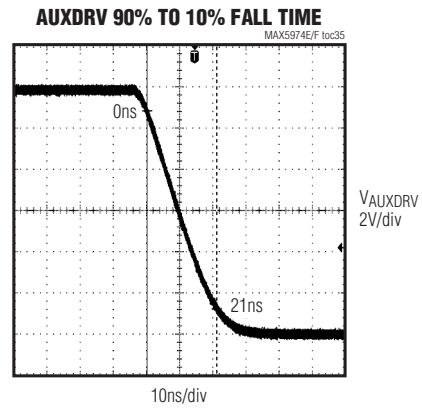
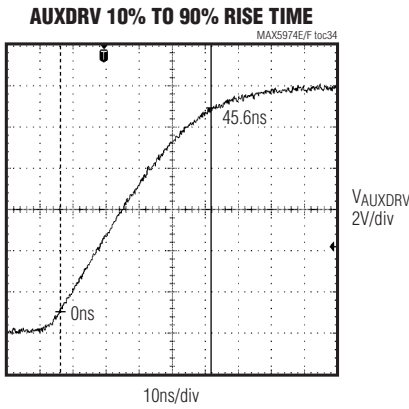
**NDRV 90% TO 10% FALL TIME**



# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

## Typical Operating Characteristics (continued)

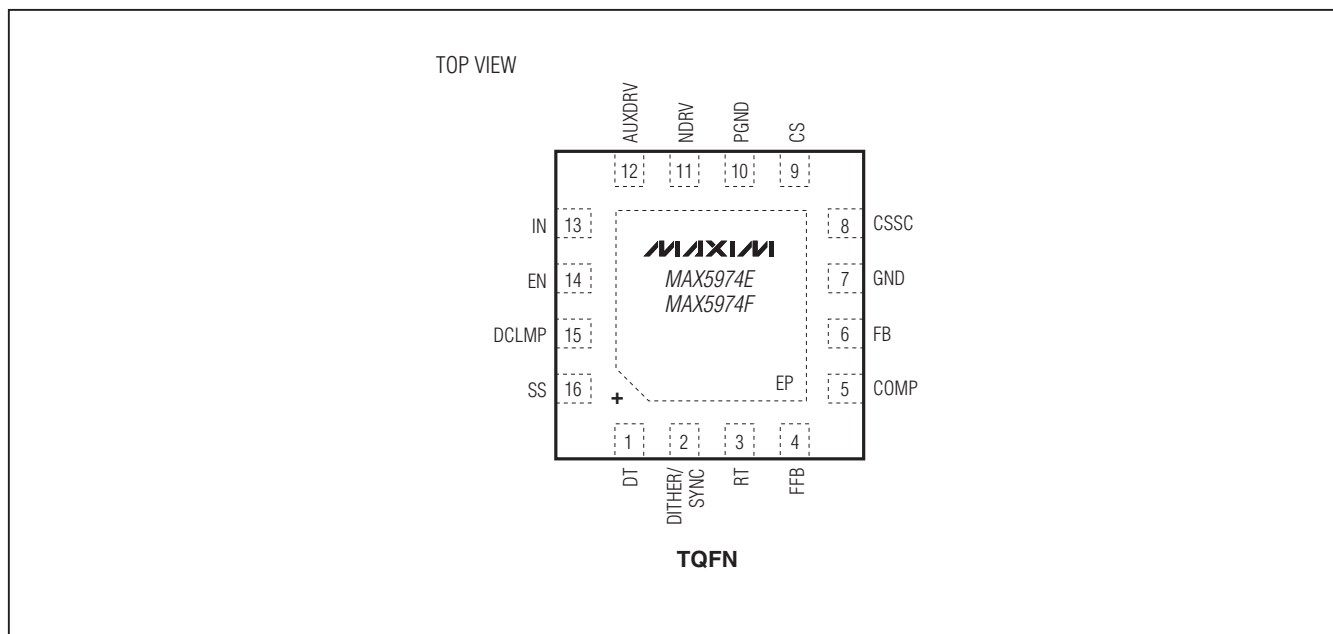
( $V_{IN} = 12V$  (for MAX5974E, bring  $V_{IN}$  up to 17V for startup),  $V_{CS} = V_{CSSC} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}$ ,  $V_{EN} = 2V$ ,  $NDRV = AUXDRV = SS = COMP =$  unconnected,  $R_{RT} = 34.8k\Omega$ ,  $R_{DT} = 25k\Omega$ , unless otherwise noted.)



# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

## Pin Configuration

**MAX5974E/MAX5974F**



## Pin Description

PIN	NAME	FUNCTION
1	DT	Dead-Time Programming Resistor Connection. Connect resistor $R_{DT}$ from DT to GND to set the desired dead time between the NDRV and AUXDRV signals. See the <i>Dead Time</i> section to calculate the resistor value for a particular dead time.
2	DITHER/ SYNC	Frequency Dithering Programming or Synchronization Connection. For spread-spectrum frequency operation, connect a capacitor from DITHER to GND and a resistor from DITHER to RT. To synchronize the internal oscillator to the externally applied frequency, connect DITHER/SYNC to the synchronization pulse.
3	RT	Switching Frequency Programming Resistor Connection. Connect resistor $R_{RT}$ from RT to GND to set the PWM switching frequency. See the <i>Oscillator/Switching Frequency</i> section to calculate the resistor value for the desired oscillator frequency.
4	FFB	Frequency Foldback Threshold Programming Input. Connect a resistor from FFB to GND to set the output average current threshold below which the converter folds back the switching frequency to 1/2 of its original value. Connect to GND to disable frequency foldback.
5	COMP	Transconductance Amplifier Output and PWM Comparator Input. COMP is level shifted down and connected to the inverting input of the PWM comparator.

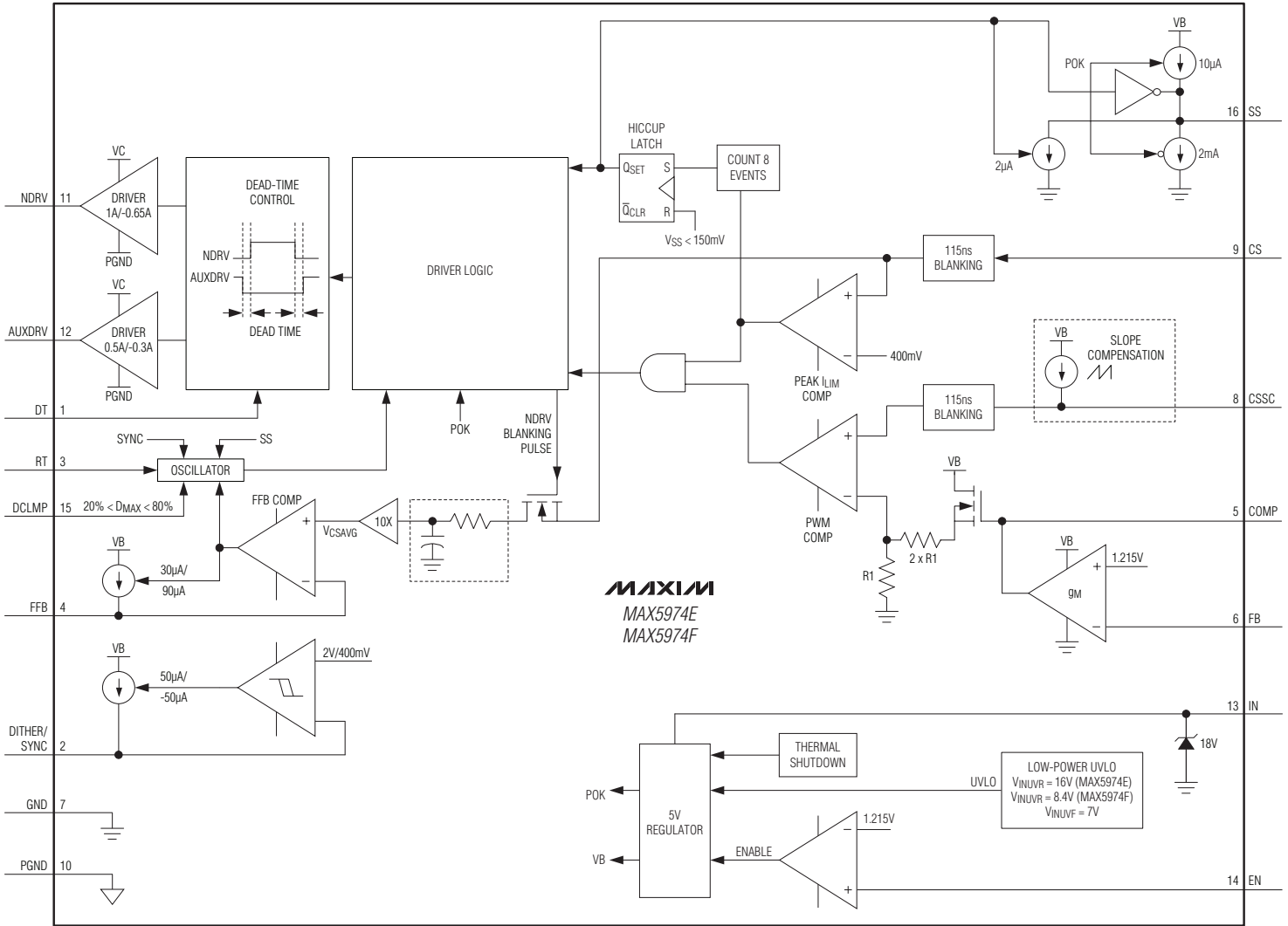
## Current-Mode PWM Controllers for Low-Cost Flyback Supplies

### Pin Description (continued)

PIN	NAME	FUNCTION
6	FB	Transconductance Amplifier Inverting Input
7	GND	Signal Ground
8	CSSC	Current Sense with Slope Compensation Input. A resistor connected from CSSC to CS programs the amount of slope compensation. See the <i>Programmable Slope Compensation</i> section.
9	CS	Current-Sense Input. Current-sense connection for average current sense and cycle-by-cycle current limit. Peak current-limit trip voltage is 400mV.
10	PGND	Power Ground. PGND is the return path for gate-driver switching currents.
11	NDRV	n-Channel Main Switch Gate-Driver Output
12	AUXDRV	Output Synchronous Rectifier Gate-Driver Output
13	IN	Converter Supply Input. IN has wide UVLO hysteresis, enabling the design of efficient power supplies. See the <i>Enable Input</i> section to determine if an external zener diode is required at IN.
14	EN	Enable Input. The gate drivers are disabled and the device is in a low-power UVLO mode when the voltage on EN is below $V_{ENF}$ . When the voltage on EN is above $V_{ENR}$ , the device checks for other enable conditions. See the <i>Enable Input</i> section for more information about interfacing to EN.
15	DCLMP	Feed-Forward Maximum Duty-Cycle Clamp Programming Input. Connect a resistive divider between the input supply voltage DCLMP and GND. The voltage at DCLMP sets the maximum duty cycle ( $D_{MAX}$ ) of the converter inversely proportional to the input supply voltage, so that the MOSFET remains protected during line transients.
16	SS	Soft-Start Programming Capacitor Connection. Connect a capacitor from SS to GND to program the soft-start period. This capacitor also determines hiccup mode current-limit restart time. A resistor from SS to GND can also be used to set the $D_{MAX}$ below 75%.
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

Block Diagram



**MAX5974E/MAX5974F**

# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

## Detailed Description

The MAX5974\_ are optimized for controlling a 25W to 50W synchronous rectification flyback converter in continuous-conduction mode. The main switch gate driver (NDRV) and the output synchronous rectifier driver (AUXDRV) are sized to optimize efficiency for 25W design. The features-rich devices are ideal for PoE IEEE 802.3af/at-powered devices.

The MAX5974E offers a 16V bootstrap UVLO wake-up level with a 9V wide hysteresis. The low startup and operating currents allow the use of a smaller storage capacitor at the input without compromising startup and hold times. The MAX5974E is well-suited for universal input (rectified 85V AC to 265V AC) or telecom (-36V DC to -72V DC) power supplies.

The MAX5974F has a UVLO rising threshold of 8.4V and can accommodate for low-input voltage (12V DC to 24V DC) power sources such as wall adapters.

Power supplies designed with the MAX5974E use a high-value startup resistor,  $R_{IN}$ , that charges a reservoir capacitor,  $C_{IN}$  (see the *Typical Application Circuit*). During this initial period, while the voltage is less than the internal bootstrap UVLO threshold, the device typically consumes only 100 $\mu$ A of quiescent current. This low startup current and the large bootstrap UVLO hysteresis help to minimize the power dissipation across  $R_{IN}$  even at the high end of the universal AC input voltage (265V AC).

Feed-forward maximum duty-cycle clamping detects changes in line conditions and adjusts the maximum duty cycle accordingly to eliminate the clamp voltage's (i.e., the main power FET's drain voltage) dependence on the input voltage.

For EMI-sensitive applications, the programmable frequency dithering feature allows up to  $\pm 10\%$  variation in the switching frequency. This spread-spectrum modulation technique spreads the energy of switching harmonics over a wider band while reducing their peaks, helping to meet stringent EMI goals.

The devices include a cycle-by-cycle current limit that turns off the main and AUX drivers whenever the internally set threshold of 400mV is exceeded. Eight consecutive occurrences of current-limit events trigger hiccup mode, which protects external components by halting switching for a period of time ( $t_{RSTRT}$ ) and allowing the overload current to dissipate in the load and

body diode of the synchronous rectifier before soft-start is reattempted.

### Current-Mode Control Loop

The advantages of current-mode control over voltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Second, the stability requirements of the current-mode controller are reduced to that of a single-pole system, unlike the double pole in voltage-mode control.

The devices use a current-mode control loop where the scaled output of the error amplifier (COMP) is compared to a slope-compensated current-sense signal at CSSC.

### Input Clamp

When the device is enabled, an internal 18V input clamp is active. During an overvoltage condition, the clamp prevents the voltage at the supply input IN from rising above 18.5V (typ).

When the device is disabled, the input clamp circuitry is also disabled.

### Enable Input

The enable input is used to enable or disable the device. Driving EN low disables the device. Note that the internal 18V input clamp is also disabled when EN is low. Therefore, an external 18V zener diode is needed for certain operating conditions as described in the following sections.

### UVLO on Power Source

The enable input has an accurate threshold of 1.26V (max). For applications that require a UVLO on the power source, connect a resistive divider from the power source to EN to GND as shown in Figure 1. A zener diode between IN and PGND is required to prevent the NDRV and AUXDRV gate-drive voltages from exceeding 20V, the maximum allowed gate voltage of power FETs.

The external zener diode should clamp in the following range:

$$20V > V_Z > V_{UVLO(MAX)}$$

where  $V_Z$  is the zener voltage and  $V_{UVLO(MAX)}$  is the maximum wakeup level (16.5V or 8.85V depending on the device version). A 18V zener diode is the best choice.

# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

Design the resistive divider by first selecting the value of  $R_{EN1}$  to be on the order of  $100k\Omega$ . Then calculate  $R_{EN2}$  as follows:

$$V_{EN2} = R_{EN1} \times \frac{V_{EN(MAX)}}{V_{S(UVLO)} - V_{EN(MAX)}}$$

where  $V_{EN(MAX)}$  is the maximum enable threshold voltage and is equal to 1.26V and  $V_{S(UVLO)}$  is the desired UVLO threshold for the power source, below which the device is disabled.

The digital output connected to EN should be capable of withstanding more than the maximum supply voltage.

### MCU Control of Enable Input

When using a microcontroller GPIO to control the enable input, an 18V zener diode is required on IN as shown in Figure 2.

### High-Voltage Logic Control of Enable Input

In the case where EN is externally controlled by a high-voltage open-drain/collector output (e.g., PGOOD indicator of a powered device controller), connect IN to EN through a resistor  $R_{EN}$  and connect EN to an open-drain or open-collector output as shown in Figure 3. Select  $R_{EN}$  so that the voltage at IN, when EN is low, is less than 20V (i.e., the maximum gate voltage of the main and AUX FETs):

$$V_{S(MAX)} \times \frac{R_{EN}}{R_{EN} + R_{IN}} < 20V$$

where  $V_{S(MAX)}$  is the maximum supply voltage. Obeying this relationship eliminates the need for an external zener diode.

The digital output connected to EN should be capable of withstanding more than 20V.

### Always-On Operation

For always-on operation, connect EN to IN as shown in Figure 4. No external zener diode is needed for this configuration.

### Bootstrap Undervoltage Lockout

The devices have an internal bootstrap UVLO that is very useful when designing high-voltage power supplies (see the *Block Diagram*). This allows the device to bootstrap itself during initial power-up. The MAX5974E soft-starts when  $V_{IN}$  exceeds the bootstrap UVLO threshold of  $V_{INUVR}$  (16V typ).

Because the MAX5974F is designed for use with low-voltage power sources such as wall adapters outputting 12V to 24V, they have a lower UVLO wake-up threshold of 8.4V.

### Startup Operation

The devices start up when the voltage at IN exceeds 16V (MAX5974E) or 8.4V (MAX5974F) and the enable input voltage is greater than 1.26V.

During normal operation, the voltage at IN is normally derived from a tertiary winding of the transformer. However, at startup there is no energy being delivered

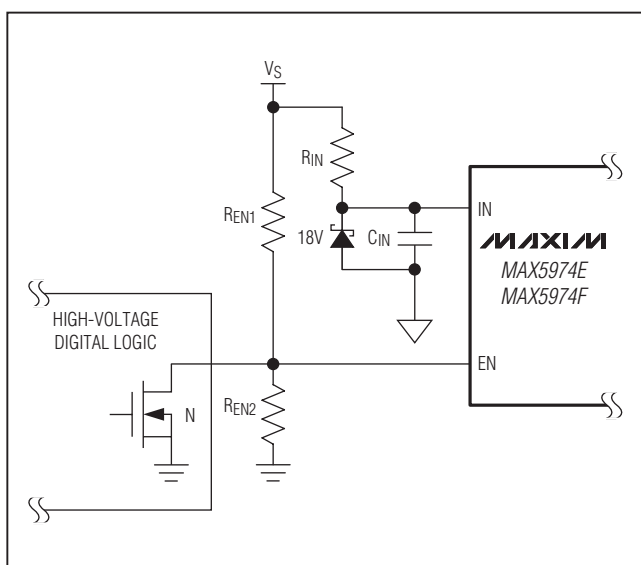


Figure 1. Programmable UVLO for the Power Source

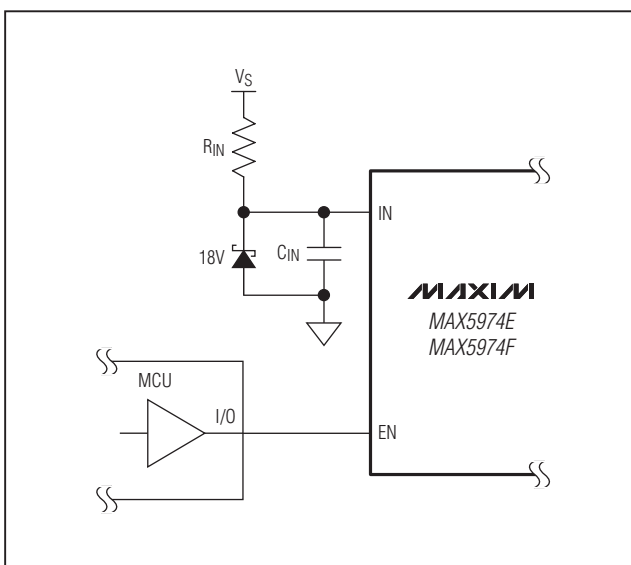


Figure 2. MCU Control of the Enable Input

## Current-Mode PWM Controllers for Low-Cost Flyback Supplies

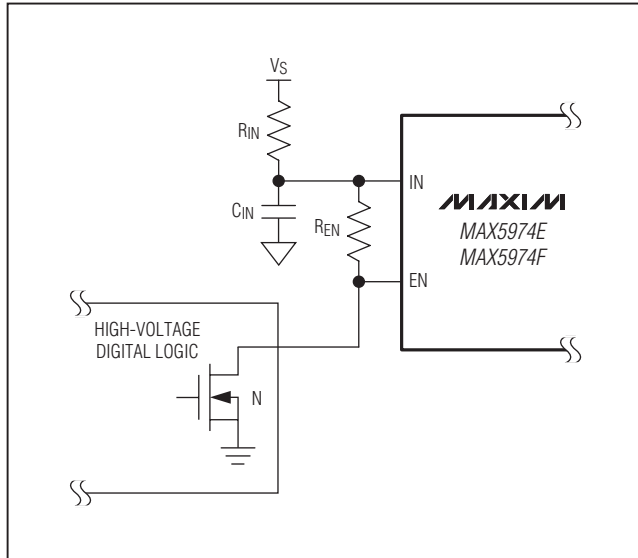


Figure 3. High-Voltage Logic Control of the Enable Input

through the transformer; hence, a special bootstrap sequence is required. In the *Typical Application Circuit*,  $C_{IN}$  charges through the startup resistor,  $R_{IN}$ , to an intermediate voltage. Only  $100\mu\text{A}$  of the current supplied through  $R_{IN}$  is used by the ICs, the remaining input current charges  $C_{IN}$  until  $V_{IN}$  reaches the bootstrap UVLO wake-up level. Once  $V_{IN}$  exceeds this level, NDRV begins switching the n-channel MOSFET and transfers energy to the secondary and tertiary outputs. If the voltage on the tertiary output builds to higher than 7V (the bootstrap UVLO shutdown level), then startup has been accomplished and sustained operation commences. If  $V_{IN}$  drops below 7V before startup is complete, the device goes back to low-current UVLO. In this case, increase the value of  $C_{IN}$  to store enough energy to allow for the voltage at the tertiary winding to build up.

### Soft-Start

A capacitor from SS to GND,  $C_{SS}$ , programs the soft-start time.  $V_{SS}$  controls the oscillator duty cycle during startup to provide a slow and smooth increase of the duty cycle to its steady-state value. Calculate the value of  $C_{SS}$  as follows:

$$C_{SS} = \frac{I_{SS-CH} \times t_{SS}}{2V}$$

where  $I_{SS-CH}$  ( $10\mu\text{A}$  typ) is the current charging  $C_{SS}$  during soft-start and  $t_{SS}$  is the programmed soft-start time.

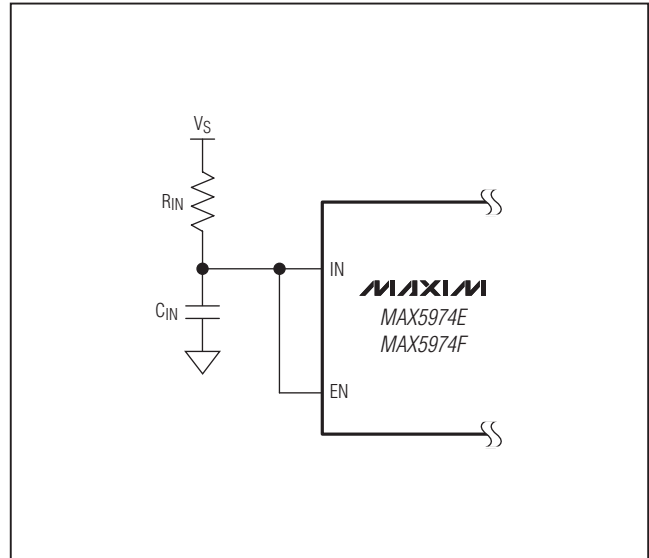


Figure 4. Always-On Operation

A resistor can also be added from the SS pin to GND to clamp  $V_{SS} < 2V$  and, hence, program the maximum duty cycle to be less than 80% (see the *Duty-Cycle Clamping* section).

### NDRV Driver

The NDRV output drives an external n-channel MOSFET. NDRV can source/sink in excess of  $650\text{mA}/1000\text{mA}$  peak current; therefore, select a MOSFET that yields acceptable conduction and switching losses. The external MOSFET used must be able to withstand the maximum clamp voltage.

### AUXDRV Driver

The AUXDRV output drives the output synchronous rectifier to lower conduction losses.

### Dead Time

Dead time between the main and AUX output edges allow ZVS to occur, minimizing conduction losses and improving efficiency. The dead time ( $t_{DT}$ ) is applied to both leading and trailing edges of the main and AUX outputs as shown in Figure 5. Connect a resistor between DT and GND to set  $t_{DT}$  to any value between 40ns and 400ns:

$$R_{DT} = \frac{10\text{k}\Omega}{40\text{ns}} \times t_{DT}$$

# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

MAX5974E/MAX5974F

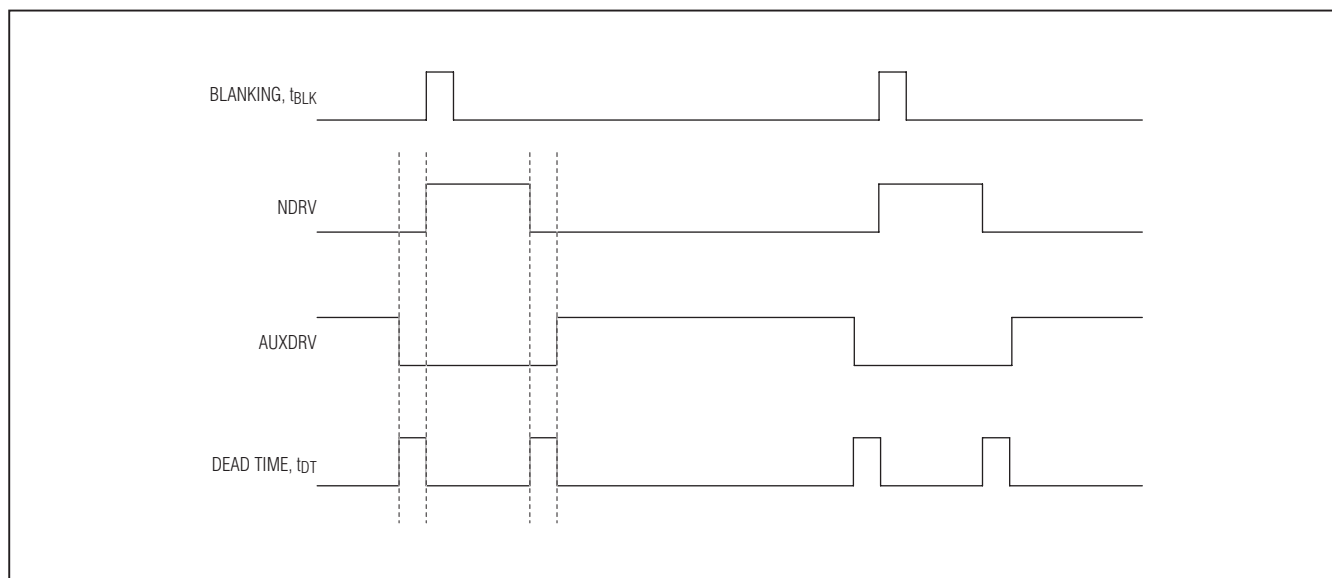


Figure 5. Dead Time Between AUXDRV and NDRV

## Oscillator/Switching Frequency

The ICs' switching frequency is programmable between 100kHz and 600kHz with resistor  $R_{RT}$  connected between RT and GND. Use the following formula to determine the appropriate value of  $R_{RT}$  needed to generate the desired output-switching frequency ( $f_{SW}$ ):

$$R_{RT} = \frac{8.7 \times 10^9}{f_{SW}}$$

where  $f_{SW}$  is the desired switching frequency.

## Peak Current Limit

The current-sense resistor ( $R_{CS}$  in the *Typical Application Circuit*), connected between the source of the n-channel MOSFET and PGND, sets the current limit. The current-limit comparator has a voltage trip level ( $V_{CS-PEAK}$ ) of 400mV. Use the following equation to calculate the value of  $R_{CS}$ :

$$R_{CS} = \frac{400\text{mV}}{I_{PRI}}$$

where  $I_{PRI}$  is the peak current in the primary side of the transformer, which also flows through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (NDRV) terminates the current on-cycle, within 35ns (typ).

The devices implement 115ns of leading-edge blanking to ignore leading-edge current spikes. These spikes are caused by reflected secondary currents, current-discharging capacitance at the FET's drain, and gate-charging current. Use a small RC network for additional filtering of the leading-edge spike on the sense waveform when needed. Set the corner frequency between 10MHz and 20MHz.

After the leading-edge blanking time, the device monitors  $V_{CS}$  for any breaches of the peak current limit of 400mV. The duty cycle is terminated immediately when  $V_{CS}$  exceeds 400mV.

## Output Short-Circuit Protection with Hiccup Mode

When the device detects eight consecutive peak current-limit events, both NDRV and AUXDRV driver outputs are turned off for a restart period,  $t_{RSTRT}$ . After  $t_{RSTRT}$ , the device undergoes soft-start. The duration of the restart period depends on the value of the capacitor at SS ( $C_{SS}$ ). During this period,  $C_{SS}$  is discharged with a pulldown current of  $I_{SS-DH}$  (2 $\mu$ A typ). Once its voltage reaches 0.15V, the restart period ends and the device initiates a soft-start sequence. An internal counter ensures that the minimum restart period ( $t_{RSTRT-MIN}$ ) is 1024 clock cycles when the time required for  $C_{SS}$  to discharge to 0.15V is less than 1024 clock cycles. Figure 6 shows the behavior of the device prior and during hiccup mode.

## Current-Mode PWM Controllers for Low-Cost Flyback Supplies

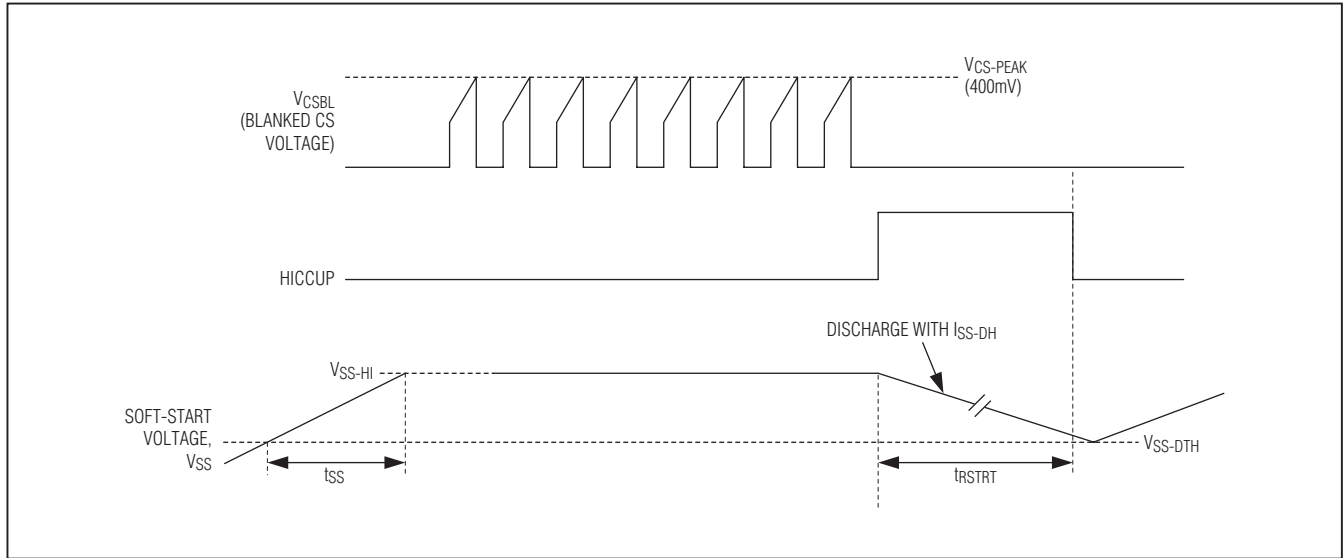


Figure 6. Hiccup Mode Timing Diagram

### Frequency Foldback for High-Efficiency Light-Load Operation

The frequency foldback threshold can be programmed from 0 to 20% of the full load current using a resistor from FFB to GND.

When VCSAVG falls below V<sub>FFB</sub>, the device folds back the switching frequency to 1/2 the original value to reduce switching losses and increase the converter efficiency. Calculate the value of R<sub>FFB</sub> as follows:

$$R_{FFB} = \frac{10 \times I_{LOAD(LIGHT)} \times R_{CS}}{I_{FFB}}$$

where R<sub>FFB</sub> is the resistor between FFB and GND, I<sub>LOAD(LIGHT)</sub> is the current at light-load conditions that triggers frequency foldback, R<sub>CS</sub> is the value of the sense resistor connected between CS and PGND, and I<sub>FFB</sub> is the current sourced from FFB to R<sub>FFB</sub> (30μA typ).

### Duty-Cycle Clamping

The maximum duty cycle is determined by the lowest of three voltages: 2V, the voltage at SS (V<sub>SS</sub>), and the voltage (2.43V - V<sub>DCLMP</sub>). The maximum duty cycle is calculated as:

$$D_{MAX} = \frac{V_{MIN}}{2.43V}$$

where V<sub>MIN</sub> = minimum (2V, V<sub>SS</sub>, 2.43V - V<sub>DCLMP</sub>).

### SS

By connecting a resistor between SS and ground, the voltage at SS can be made to be lower than 2V. V<sub>SS</sub> is calculated as follows:

$$V_{SS} = R_{SS} \times I_{SS-CH}$$

where R<sub>SS</sub> is the resistor connected between SS and GND, and I<sub>SS-CH</sub> is the current sourced from SS to R<sub>SS</sub> (10μA typ).

### DCLMP

To set D<sub>MAX</sub> using supply voltage feed-forward, connect a resistive divider between the supply voltage, DCLMP, and GND as shown in the *Typical Application Circuit*. This feed-forward duty-cycle clamp ensures that the external n-channel MOSFET is not stressed during supply transients. V<sub>DCLMP</sub> is calculated as follows:

$$V_{DCLMP} = \frac{R_{DCLMP2}}{R_{DCLMP1} + R_{DCLMP2}} \times V_S$$

where R<sub>DCLMP1</sub> and R<sub>DCLMP2</sub> are the resistive divider values shown in the *Typical Application Circuit* and V<sub>S</sub> is the input supply voltage.

The maximum duty cycle is then set to:

$$D_{MAX} = 1 - \frac{D_{CLMP}}{2.43}$$

# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

## Oscillator Synchronization

The internal oscillator can be synchronized to an external clock by applying the clock to DITHER/SYNC directly. The external clock frequency can be set anywhere between 1.1x to 2x the internal clock frequency.

Using an external clock increases the maximum duty cycle by a factor equal to  $f_{\text{SYNC}}/f_{\text{SW}}$ . This factor should be accounted for in setting the maximum duty cycle using any of the methods described in the *Duty-Cycle Clamping* section. The formula below shows how the maximum duty cycle is affected by the external clock frequency:

$$D_{\text{MAX}} = \frac{V_{\text{MIN}}}{2.43\text{V}} \times \frac{f_{\text{SYNC}}}{f_{\text{SW}}}$$

where  $V_{\text{MIN}}$  is described in the *Duty-Cycle Clamping* section,  $f_{\text{SW}}$  is the switching frequency as set by the resistor connected between RT and GND, and  $f_{\text{SYNC}}$  is the external clock frequency.

## Frequency Dithering for Spread-Spectrum Applications (Low EMI)

The switching frequency of the converter can be dithered in a range of  $\pm 10\%$  by connecting a capacitor from DITHER/SYNC to GND, and a resistor from DITHER/SYNC to RT as shown in the *Typical Application Circuit*. This results in lower EMI.

A current source at DITHER/SYNC charges the capacitor  $C_{\text{DITHER}}$  to 2V at  $50\mu\text{A}$ . Upon reaching this trip point, it discharges  $C_{\text{DITHER}}$  to 0.4V at  $50\mu\text{A}$ . The charging and discharging of the capacitor generates a triangular waveform on DITHER/SYNC with peak levels at 0.4V and 2V and a frequency that is equal to:

$$f_{\text{TRI}} = \frac{50\mu\text{A}}{C_{\text{DITHER}} \times 3.2\text{V}}$$

Typically,  $f_{\text{TRI}}$  should be set close to 1kHz. The resistor  $R_{\text{DITHER}}$  connected from DITHER/SYNC to RT determines the amount of dither as follows:

$$\% \text{DITHER} = \frac{4}{3} \times \frac{R_{\text{RT}}}{R_{\text{DITHER}}}$$

where %DITHER is the amount of dither expressed as a percentage of the switching frequency. Setting  $R_{\text{DITHER}}$  to  $10 \times R_{\text{RT}}$  generates  $\pm 10\%$  dither.

## Programmable Slope Compensation

The device generates a current ramp at CSSC such that its peak is  $50\mu\text{A}$  at 80% duty cycle of the oscillator. An external resistor connected from CSSC to the CS then converts this current ramp into programmable slope-compensation amplitude, which is added to the current-sense signal for stability of the peak current-mode control loop. The ramp rate of the slope compensation signal is given by:

$$m = \frac{R_{\text{CSSC}} \times 50\mu\text{A} \times f_{\text{SW}}}{80\%}$$

where  $m$  is the ramp rate of the slope-compensation signal,  $R_{\text{CSSC}}$  is the value of the resistor connected between CSSC and CS used to program the ramp rate, and  $f_{\text{SW}}$  is the switching frequency.

## Error Amplifier

The MAX5974\_ include an internal error amplifier for primary feedback. The noninverting input of the error amplifier is connected to the internal reference and feedback is provided at the inverting input. High open-loop gain and unity-gain bandwidth allow good closed-loop bandwidth and transient response. Calculate the power-supply output voltage using the following equation:

$$V_{\text{OUT}} = V_{\text{REF}} \times \frac{R_{\text{FB1}} + R_{\text{FB2}}}{R_{\text{FB2}}}$$

where  $V_{\text{REF}} = 1.215\text{V}$ . The amplifier's noninverting input is internally connected to a soft-start circuit that gradually increases the reference voltage during startup. This forces the output voltage to come up in an orderly and well-defined manner under all load conditions.

# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

## Applications Information

### Startup Time Considerations

The bypass capacitor at IN, C<sub>IN</sub>, supplies current immediately after the devices wake up (see the *Typical Application Circuit*). Large values of C<sub>IN</sub> increase the startup time, but also supply gate charge for more cycles during initial startup. If the value of C<sub>IN</sub> is too small, V<sub>IN</sub> drops below 7V because NDRV does not have enough time to switch and build up sufficient voltage across the tertiary output, which powers the device. The device goes back into UVLO and does not start. Use a low-leakage capacitor for C<sub>IN</sub>.

Typically, offline power supplies keep startup times to less than 500ms even in low-line conditions (85V AC input for universal offline or 36V DC for telecom applications). Size the startup resistor, R<sub>IN</sub>, to supply both the maximum startup bias of the device (150μA) and the charging current for C<sub>IN</sub>. C<sub>IN</sub> must be charged to 16V within the desired 500ms time period. C<sub>IN</sub> must store enough charge to deliver current to the device for at least the soft-start time (t<sub>SS</sub>) set by C<sub>SS</sub>. To calculate the approximate amount of capacitance required, use the following formula:

$$I_G = Q_{GTOT} f_{SW}$$

$$C_{IN} = \frac{(I_{IN} + I_G)(t_{SS})}{V_{HYST}}$$

where I<sub>IN</sub> is the ICs' internal supply current (1.8mA) after startup, Q<sub>GTOT</sub> is the total gate charge for the n-channel and p-channel FETs, f<sub>SW</sub> is the ICs' switching frequency, V<sub>HYST</sub> is the bootstrap UVLO hysteresis (9V typ), and t<sub>SS</sub> is the soft-start time. R<sub>IN</sub> is then calculated as follows:

$$R_{IN} \cong \frac{V_{S(MIN)} - V_{INUVR}}{I_{START}}$$

where V<sub>S(MIN)</sub> is the minimum input supply voltage for the application (36V for telecom), V<sub>INUVR</sub> is the bootstrap UVLO wake-up level (16V), and I<sub>START</sub> is the IN supply current at startup (150μA max).

Choose a higher value for R<sub>IN</sub> than the one calculated above if a longer startup time can be tolerated in order to minimize power loss on this resistor.

### Bias Circuit

An out-of-phase tertiary winding is needed to power the bias circuit. The voltage across the tertiary V<sub>T</sub> during the off-time is:

$$V_T = V_{OUT} \times \frac{N_T}{N_S}$$

where V<sub>OUT</sub> is the output voltage and N<sub>T</sub>/N<sub>S</sub> is the turns ratio from the tertiary to the secondary winding. Select the turns ratio so that V<sub>T</sub> is above the UVLO shutdown level (7.35V max) by a margin determined by the holdup time needed to "ride through" a brownout.

### Layout Recommendations

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dV/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the main MOSFET presents a dV/dt source; therefore, minimize the surface area of the MOSFET heatsink as much as possible. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use a ground plane for best results.

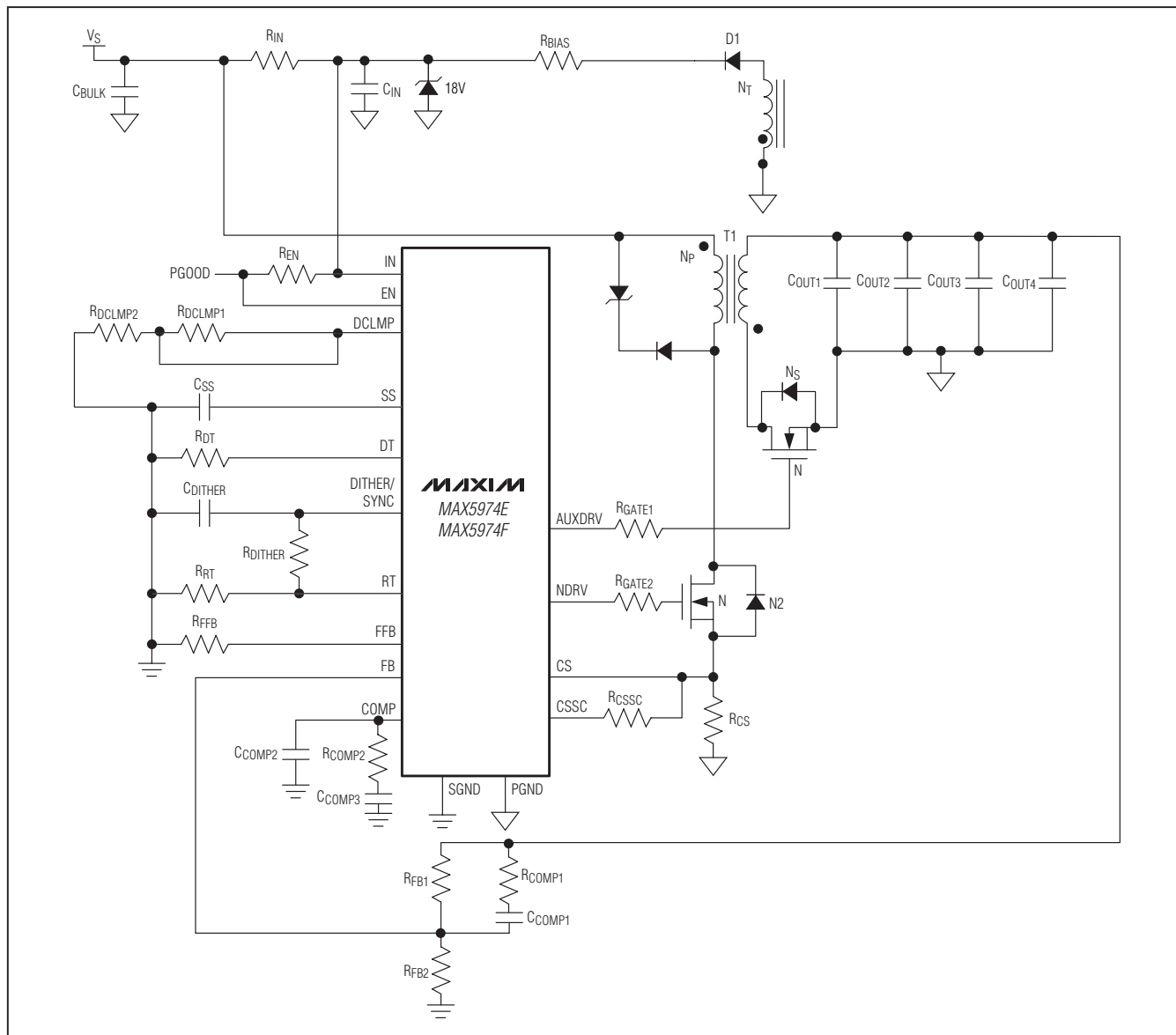
For universal AC input design, follow all applicable safety regulations. Offline power supplies can require UL, VDE, and other similar agency approvals.

Refer to the MAX5974E Evaluation Kit data sheet for a recommended layout and component values.

# Current-Mode PWM Controllers for Low-Cost Flyback Supplies

## Typical Application Circuit

**MAX5974E/MAX5974F**



### Chip Information

PROCESS: BiCMOS

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633+4	<a href="#">21-0136</a>	<a href="#">90-0031</a>

# **Current-Mode PWM Controllers for Low-Cost Flyback Supplies**

## **Revision History**

<b>REVISION NUMBER</b>	<b>REVISION DATE</b>	<b>DESCRIPTION</b>	<b>PAGES CHANGED</b>
0	6/11	Initial release	—
1	8/11	Update <i>Typical Application Circuit</i> .	21

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