19-3150; Rev 2; 10/05

±10V, Dual, 12-Bit, Serial, Voltage-Output DAC

General Description

The MAX5322 dual, 12-bit, serial-interface, digital-to-analog converter (DAC) provides bipolar ±5V to ±10V outputs from ±12V to ±15V analog power-supply voltages, or unipolar 5V to 10V outputs from a single 12V to 15V analog power-supply voltage.

The MAX5322 features excellent linearity with both integral nonlinearity (INL) and differential nonlinearity (DNL) guaranteed to ±1 LSB (max). The device also features a fast 10µs to 0.5 LSB settling time, and a hardware-shutdown feature that reduces current consumption to 2.8µA. The output goes to midscale at power-up in bipolar mode (0V), and to zero scale at power-up in unipolar mode (0V). A clear input ($\overline{CLR}$) asynchronously clears the DAC register and sets the outputs to 0V. The outputs can be asynchronously updated with the load DAC ($\overline{LDAC}$) input.

The device features a fast 10MHz SPI™-/QSPI™-/MICROWIRE™-compatible serial interface that operates with 3V or 5V logic. Additional features include a serial-data output (DOUT) for daisy chaining and read-back functions. The MAX5322 requires external reference voltages of 2V to 5.25V and is available in a 28-pin SSOP package that operates over the extended (-40°C to +85°C) temperature range.

Features

- ♦ **Unipolar or Bipolar Output-Voltage Ranges**
  - **Unipolar: 0 to +2 x V_{REF} (Single or Dual Supply)**
  - **Bipolar: -2 x V_{REF} to +2 x V_{REF} (Dual Supply)**
- ♦ **Guaranteed INL ≤ ±1 LSB (max)**
- ♦ **Guaranteed Monotonic: DNL ≤ ±1 LSB (max)**
- ♦ **10µs Settling Time to 0.5 LSB**
- ♦ **Low 2.8µA Shutdown Current**
- ♦ **Fast 10MHz SPI-/QSPI-/MICROWIRE-Compatible Serial Interface**
- ♦ **Power-On Reset Sets DAC Output to 0V**
- ♦ **Schmitt Trigger Inputs for Direct Optocoupler Interface**
- ♦ **Serial-Data Output Allows Daisy-Chaining of Devices**
- ♦ **28-Pin SSOP (8mm x 10mm)**

Applications

Motor Control

Industrial Process Controls

Industrial Automation

Automatic Test Equipment (ATE)

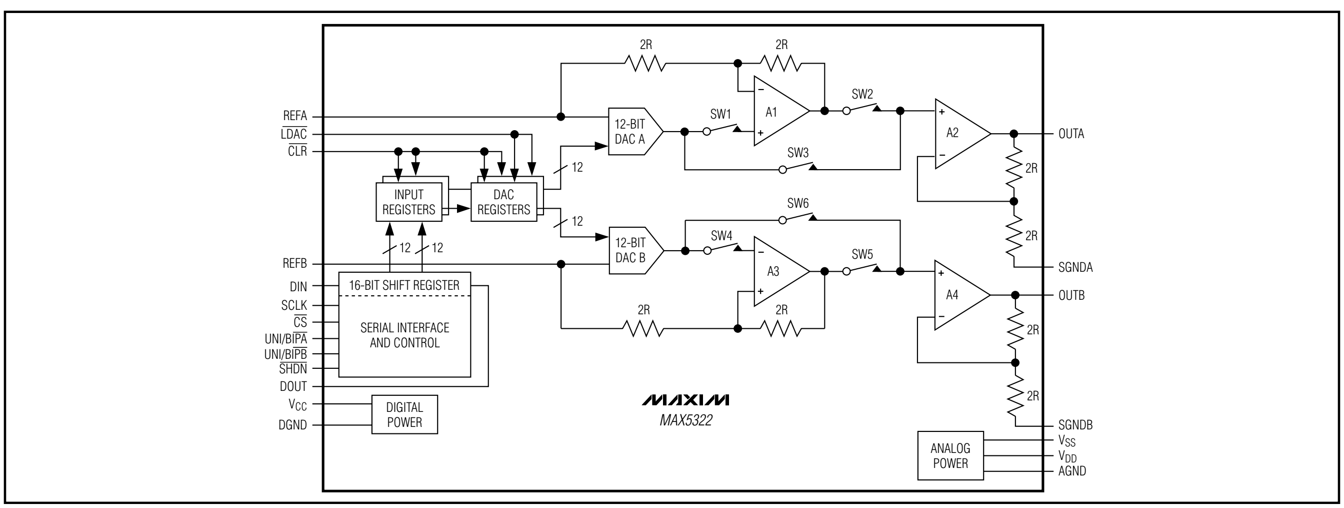
Analog I/O Boards

Data-Acquisition Systems

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5322EAI	-40°C to +85°C	28 SSOP

Functional Diagram



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MICROWIRE is a trademark of National Semiconductor Corp.

±10V, Dual, 12-Bit, Serial, Voltage-Output DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND..-0.3V to +17V
V_{SS} to AGND ....-17V to +0.3V
V_{DD} to V_{SS} ....+34V
V_{CC} to DGND ....-0.3V to +6V
AGND to DGND...-0.3V to +0.3V
SGND_ to AGND ....-0.3V to +0.3V
SCLK, DIN, $\overline{CS}$, $\overline{SHDN}$, UNI/$\overline{BIP}$_, $\overline{CLR}$,
$\overline{LDAC}$, DOUT to DGND ....-0.3V to (V_{CC} + 0.3V)
OUT_ to AGND................................(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
REF_ to AGND...-0.3V to +6V
Maximum Current into REF_..±10mA
Maximum Current into Any Pin Excluding REF_...............±50mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin SSOP (derate 9.5mW/°C above +70°C) 761.9mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (DUAL SUPPLY)

(V_{DD} = +15V ±5%, V_{SS} = -15V ±5%, V_{CC} = +5V ±10%, AGND = DGND = SGND_ = 0V, $V_{REF\_}$ = 5V, R_{LOAD} = 2kΩ, C_{LOAD} = 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12			Bits
Integral Nonlinearity	INL				±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Zero-Scale Error		Bipolar, code = 800hex			±2	LSB
		Unipolar, code = 000hex			±2	
Zero-Scale Temperature Coefficient		Bipolar		0.9		ppm FSR/°C
		Unipolar		0.09		
Gain Error		Bipolar (output unloaded)			±2	LSB
		Unipolar (output unloaded)			±2	
Gain-Error Temperature Coefficient		Bipolar (output unloaded)		2		ppm FSR/°C
		Unipolar (output unloaded)		2		
ANALOG OUTPUTS (OUTA, OUTB)						
Output Voltage Range		(V_{SS} + 1.5V) < V_{OUT} < (V_{DD} - 1.5V)	-2 x V_{REF}		+2 x V_{REF}	V
Resistive Load to GND	R_{LOAD}		2			kΩ
Capacitive Load to GND	C_{LOAD}				250	pF
DC Output Resistance				0.5		Ω
SGND INPUTS (SGNDA, SGNDB)						
Input Impedance				92		kΩ
REFERENCE INPUTS (REFA, REFB)						
Reference Voltage Input Range			2.00		5.25	V
Input Resistance	R_{REF}	Code = 555hex, worst-case code	15	22		kΩ
Reference Bandwidth		V_{REF} = 200mV_{P-P} + 5V_{DC}		200		kHz

ELECTRICAL CHARACTERISTICS (DUAL SUPPLY) (continued)

(V_{DD} = +15V ±5%, V_{SS} = -15V ±5%, V_{CC} = +5V ±10%, AGND = DGND = SGND_ = 0V, $V_{REF\_}$ = 5V, R_{LOAD} = 2kΩ, C_{LOAD} = 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{SHDN}$, UNI/$\overline{BIPA}$, UNI/$\overline{BIPB}$, $\overline{CLR}$, $\overline{LDAC}$)						
Input Voltage High	V_{IH}	+2.7V ≤ V_{CC} ≤ +3.6V	0.7 x V_{CC}			V
		+4.5V ≤ V_{CC} ≤ +5.5V	2.4			
Input Voltage Low	V_{IL}	+2.7V ≤ V_{CC} ≤ +3.6V			0.8	V
		+4.5V ≤ V_{CC} ≤ +5.5V			0.8	
Input Capacitance	C	+2.7V ≤ V_{CC} ≤ +3.6V		10		pF
		+4.5V ≤ V_{CC} ≤ +5.5V		10		
Input Current (Note 1)		0 ≤ all digital inputs ≤ V_{CC}, +2.7V ≤ V_{CC} ≤ +3.6V			±1	µA
		0 ≤ all digital inputs ≤ V_{CC}, +4.5V ≤ V_{CC} ≤ +5.5V			±1	
DIGITAL OUTPUT (DOUT)						
Output Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{CC} - 0.5			V
Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Tri-State Leakage Current				0.1		µA
Tri-State Capacitance				10		pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate				2.5		V/µs
Output Settling Time		To ±0.5 LSB of full scale, code 000 to code FFF		10		µs
Digital Feedthrough		$\overline{CS}$ = high, f_{SCLK} = 10MHz, V_{OUT} = 0V		10		nV-s
DAC-to-DAC Crosstalk				2.5		nV-s
Output-Noise Spectral Density at 10kHz				130		nV/√Hz
POWER SUPPLIES						
Positive Analog-Supply Voltage	V_{DD}		10.80		15.75	V
Negative Analog-Supply Voltage	V_{SS}		-10.80		-15.75	V
Positive Digital-Supply Voltage	V_{CC}		2.7		5.5	V
Positive Analog-Supply Current	I_{DD}	Output unloaded, V_{OUT} = 0		2.8	8	mA
Negative Analog-Supply Current	I_{SS}	Output unloaded, V_{OUT} = 0		-1.5	-8	mA
Digital-Supply Current	I_{CC}	All digital inputs = 0 or V_{CC}			200	µA
Power-Supply Rejection Ratio (Note 2)	PSRR	Positive analog supply		0.0006		LSB/V
		Negative analog supply		0.03		
Shutdown Current		Positive analog supply		2.8	50	µA
		Negative analog supply		4	50	
		Digital supply		4	10	

ELECTRICAL CHARACTERISTICS (SINGLE SUPPLY)

(V_{DD} = +15V ±5%, V_{SS} = 0V, V_{CC} = +5V ±10%, AGND = DGND = SGND_ = 0V, $V_{REF\_}$ = 5V, R_{LOAD} = 10kΩ, C_{LOAD} = 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12			Bits
Integral Nonlinearity	INL	(Note 3)			±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Unipolar Zero-Scale Error					±2	LSB
Unipolar Zero-Scale Temperature Coefficient				0.09		ppm FSR/°C
Gain Error		No load			±2	LSB
Gain-Error Temperature Coefficient		No load		2		ppm FSR/°C
ANALOG OUTPUTS (OUTA, OUTB)						
Output Voltage Range			0		+2 x V_{REF}	V
Resistive Load to GND	R_{LOAD}		10			kΩ
Capacitive Load to GND	C_{LOAD}				250	pF
DC Output Resistance				0.5		Ω
SGND INPUTS (SGNDA, SGNDB)						
Input Impedance				92		kΩ
REFERENCE INPUTS (REFA, REFB)						
Reference Voltage Input Range			2.00		5.25	V
Input Resistance		Code = 555hex, worst-case code	15	22		kΩ
Reference Input Bandwidth		V_{REF} = 200mV_{P-P} + 5V_{DC}		150		kHz
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{SHDN}$, UNI/$\overline{BIP}$A, UNI/$\overline{BIP}$B, $\overline{CLR}$, $\overline{LDAC}$)						
Input Voltage High	V_{IH}	+2.7V ≤ V_{CC} ≤ +3.6V	0.7 x V_{CC}			V
		+4.5V ≤ V_{CC} ≤ +5.5V	2.4			
Input Voltage Low	V_{IL}	+2.7V ≤ V_{CC} ≤ +3.6V			0.8	V
		+4.5V ≤ V_{CC} ≤ +5.5V			0.8	
Input Capacitance	C_{IN}	+2.7V ≤ V_{CC} ≤ +3.6V		10		pF
		+4.5V ≤ V_{CC} ≤ +5.5V		10		
Input Current	I_{IN}	0 ≤ V_{IN} ≤ V_{CC}, +2.7V ≤ V_{CC} ≤ +3.6V			±1	µA
		0 ≤ V_{IN} ≤ V_{CC}, +4.5V ≤ V_{CC} ≤ +5.5V			±1	
DIGITAL OUTPUT (DOUT)						
Output Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{CC} - 0.5			V
Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Tri-State Leakage Current				0.1		µA

ELECTRICAL CHARACTERISTICS (SINGLE SUPPLY) (continued)

(V_{DD} = +15V ±5%, V_{SS} = 0V, V_{CC} = +5V ±10%, AGND = DGND = SGND_ = 0V, $V_{REF\_}$ = 5V, R_{LOAD} = 10kΩ, C_{LOAD} = 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tri-State Capacitance				10		pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate				2.5		V/µs
Output Settling Time		To ±0.5 LSB of full scale		10		µs
Digital Feedthrough		$\overline{CS}$ = high, f_{SCLK} = 10MHz, V_{OUT} = 0V		10		nV-s
DAC-to-DAC Crosstalk				2.5		nV-s
Output-Noise Spectral Density at 10kHz				130		nV/√Hz
POWER SUPPLIES						
Positive Analog Supply Voltage	V_{DD}		10.80		15.75	V
Negative Analog Supply Voltage	V_{SS}			0		V
Positive Digital Supply Voltage	V_{CC}		2.7		5.5	V
Positive Analog Supply Current	I_{DD}	Output unloaded, V_{OUT} = 0		2.5	8	mA
Negative Analog Supply Current	I_{SS}	Output unloaded, V_{OUT} = 0		-0.5	-8	mA
Digital Supply Current	I_{CC}	All digital inputs = 0 or V_{CC}		9	200	µA
Power-Supply Rejection Ratio	PSRR			0.001		LSB/V
Shutdown Current		Analog supply		2.8	5	µA
		Digital supply		2.8	5	

TIMING CHARACTERISTICS

(V_{DD} = +15V, V_{SS} = -15V or 0V, V_{CC} = +2.7V to +5.5V, AGND = DGND = SGND_ = 0, $V_{REF\_}$ = 5V, R_{LOAD} = 2kΩ, ,C_{LOAD} = 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

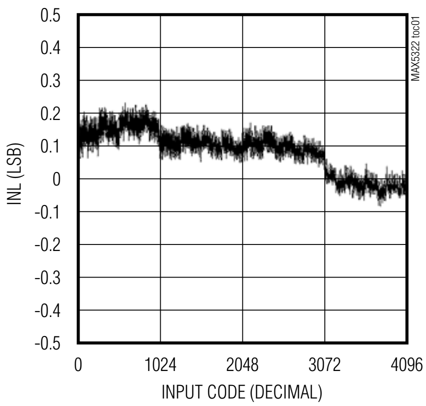
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency					10	MHz
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse-Width High	t_{CH}	For nondaisy-chain use	45			ns
SCLK Pulse-Width Low	t_{CL}	For nondaisy-chain use	45			ns
		For daisy-chain use		98		
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}	+2.7V ≤ V_{CC} ≤ +3.6V	15			ns
		+4.5V ≤ V_{CC} ≤ +5.5V	10			
DIN Setup Time	t_{DS}		20			ns
DIN Hold Time	t_{DH}		10			ns
$\overline{LDAC}$ Pulse Width	t_{LD}		50			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Low Setup Time	t_{LDS}	+2.7V ≤ V_{CC} ≤ +3.6V	100			ns
		+4.5V ≤ V_{CC} ≤ +5.5V	50			
SCLK Fall to DOUT Valid Propagation Delay	t_{DO1}	C_{LOAD} = 20pF, +2.7V ≤ V_{CC} ≤ +3.6V			100	ns
		C_{LOAD} = 20pF, +4.5V ≤ V_{CC} ≤ +5.5V			80	
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Low to DOUT Valid Time	t_{CSE}	C_{LOAD} = 20pF			120	ns
$\overline{CS}$ High to DOUT Disabled Time	t_{CSD}				120	ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		50			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}	+2.7V ≤ V_{CC} ≤ +3.6V	200			ns
		+4.5V ≤ V_{CC} ≤ +5.5V	100			
$\overline{CLR}$ Pulse-Width Low	t_{CLR}		50			ns

Note 1: Output unloaded, digital inputs = V_{CC} or DGND.
Note 2: ΔV_{DD} = 15.5V to 14.5V, ΔV_{SS} = -15.5V to -14.5V, input code = 14hex to FFFhex
Note 3: Accuracy is guaranteed from code 14hex to FFFhex

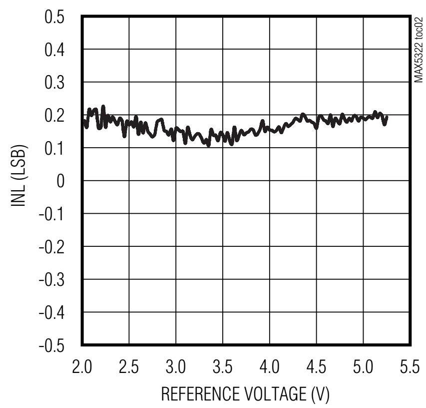
Typical Operating Characteristics

(V_{DD} = +15V, V_{SS} = -15V for bipolar graphs, V_{SS} = 0 for unipolar graphs, V_{CC} = +5V, AGND = DGND = SGND_ = 0, $V_{REF\_}$ = +5.0V, output unloaded, T_A = +25°C, all graphs apply to both unipolar and bipolar, unless otherwise noted.)

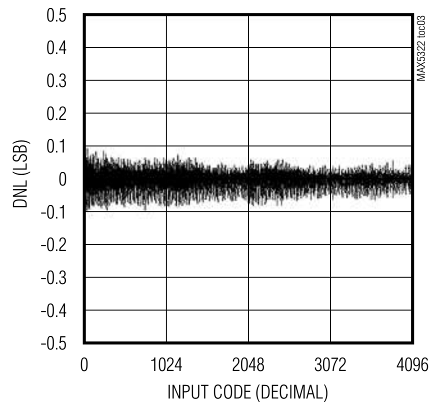
INTERGRAL NONLINEARITY vs. INPUT CODE



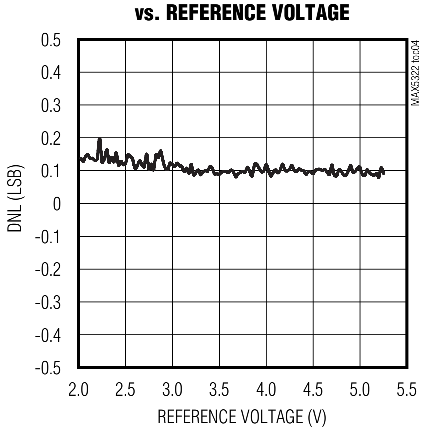
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



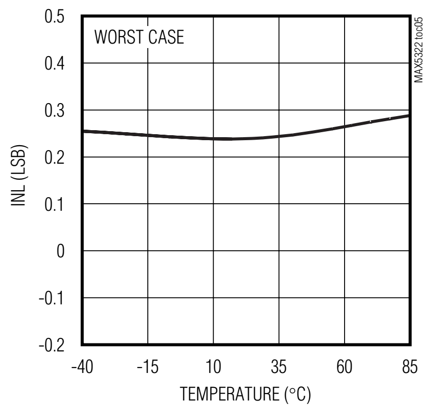
DIFFERENTIAL NONLINEARITY vs. INPUT CODE



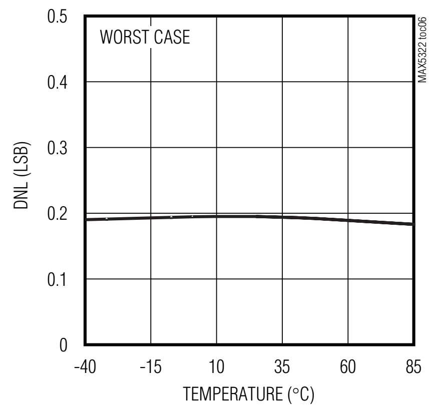
DIFFERENTIAL NONLINEARITY vs. REFERENCE VOLTAGE



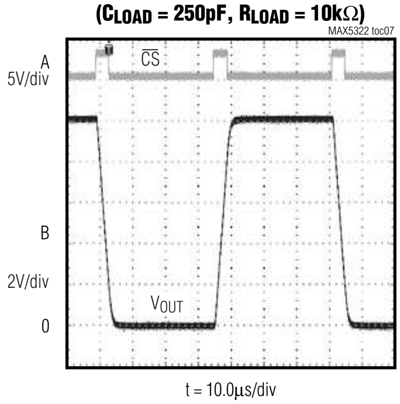
BIPOLAR INL vs. TEMPERATURE



BIPOLAR DNL vs. TEMPERATURE

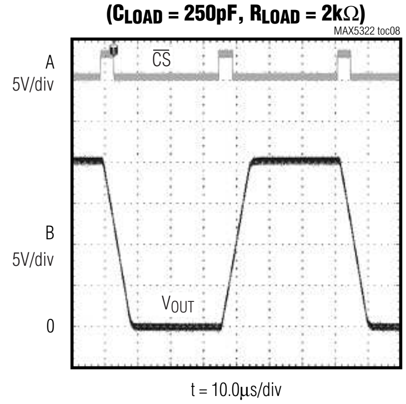


UNIPOLAR SETTLING TIME (C_{LOAD} = 250pF, R_{LOAD} = 10kΩ)



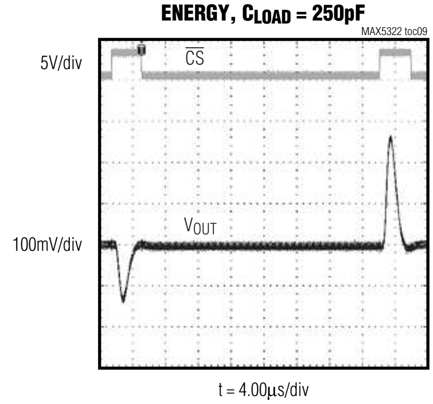
A: $\overline{CS}$, 5.0V/div
B: OUT, 2.0V/div

BIPOLAR SETTLING TIME (C_{LOAD} = 250pF, R_{LOAD} = 2kΩ)



A: $\overline{CS}$, 5.0V/div
B: OUT, 5.0V/div

BIPOLAR MAJOR CARRY GLITCH ENERGY, C_{LOAD} = 250pF

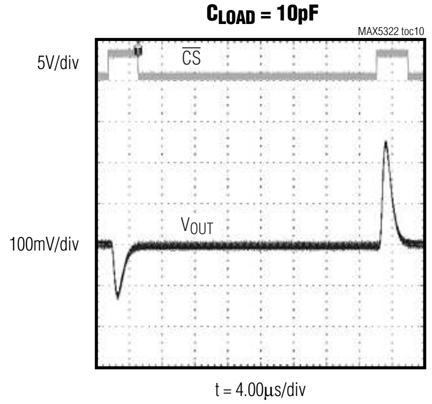


±10V, Dual, 12-Bit, Serial, Voltage-Output DAC

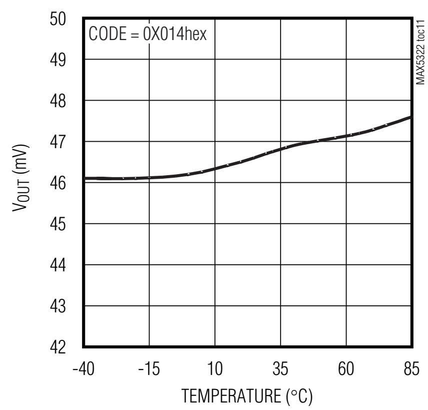
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V for bipolar graphs, V_{SS} = 0 for unipolar graphs, V_{CC} = +5V, AGND = DGND = SGND_ = 0, $V_{REF\_}$ = +5.0V, output unloaded, T_A = +25°C, all graphs apply to both unipolar and bipolar, unless otherwise noted.)

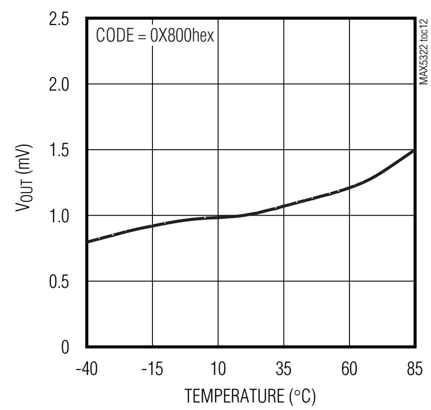
BIPOLAR MAJOR CARRY GLITCH
C_{LOAD} = 10pF



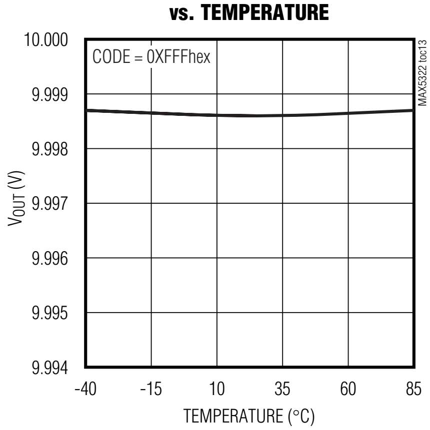
UNIPOLAR ZERO-SCALE VOLTAGE vs. TEMPERATURE



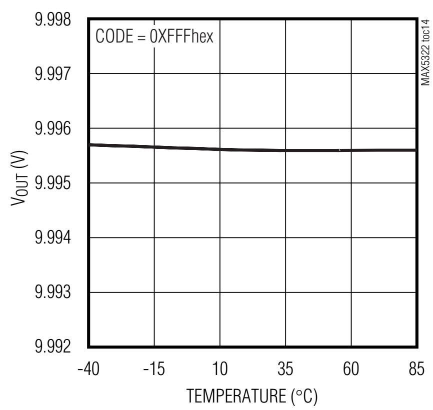
BIPOLAR ZERO-SCALE VOLTAGE vs. TEMPERATURE



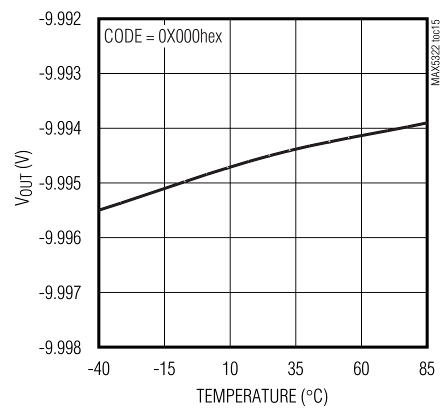
UNIPOLAR FULL-SCALE VOLTAGE vs. TEMPERATURE



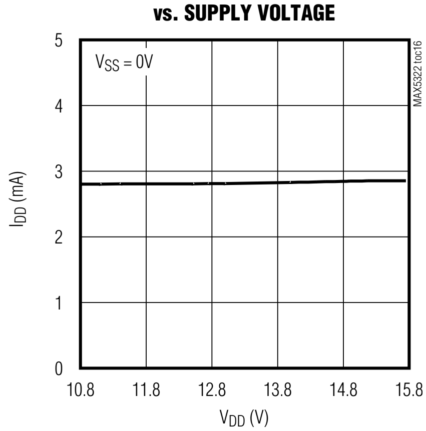
POSITIVE BIPOLAR FULL-SCALE VOLTAGE vs. TEMPERATURE



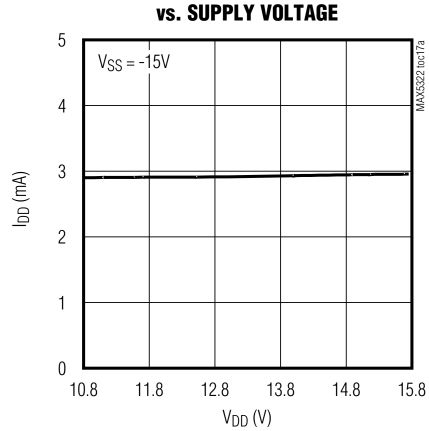
NEGATIVE BIPOLAR FULL-SCALE VOLTAGE vs. TEMPERATURE



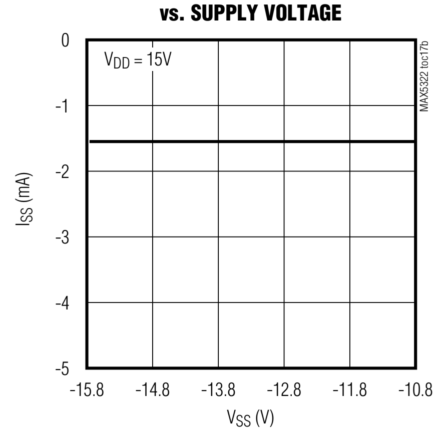
UNIPOLAR SUPPLY CURRENT vs. SUPPLY VOLTAGE



BIPOLAR POSITIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



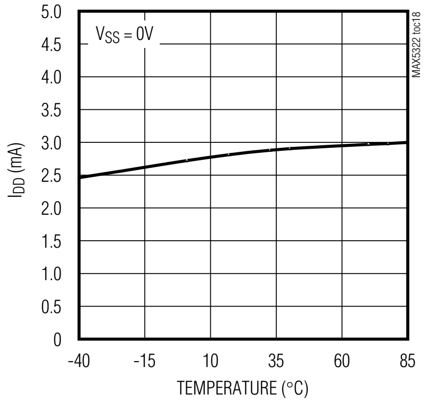
BIPOLAR NEGATIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



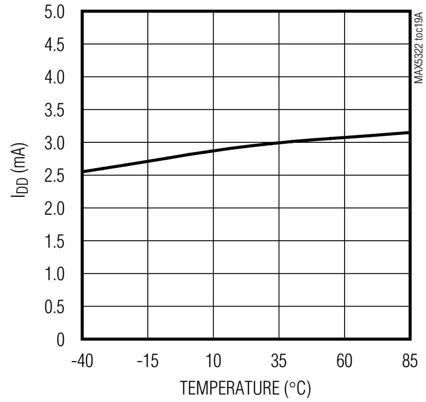
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V for bipolar graphs, V_{SS} = 0 for unipolar graphs, V_{CC} = +5V, AGND = DGND = SGND_ = 0, $V_{REF\_}$ = +5.0V, output unloaded, T_A = +25°C, all graphs apply to both unipolar and bipolar, unless otherwise noted.)

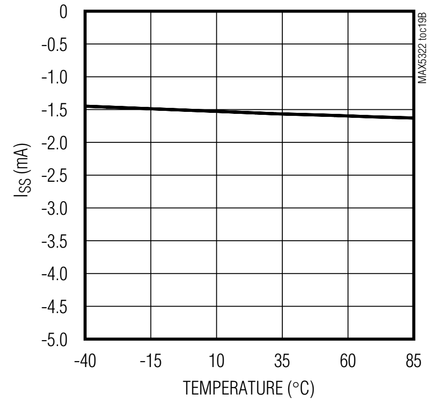
UNIPOLAR SUPPLY CURRENT vs. TEMPERATURE



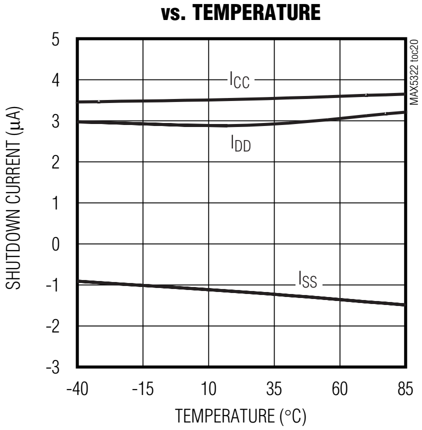
BIPOLAR POSITIVE SUPPLY CURRENT vs. TEMPERATURE



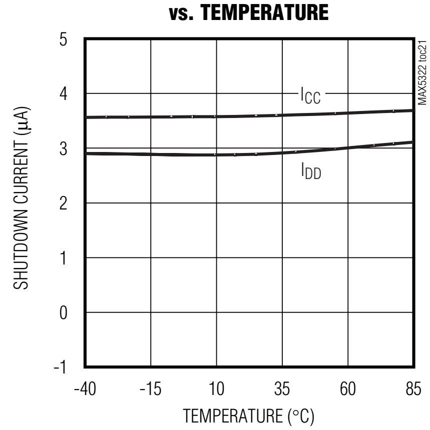
BIPOLAR NEGATIVE SUPPLY CURRENT vs. TEMPERATURE



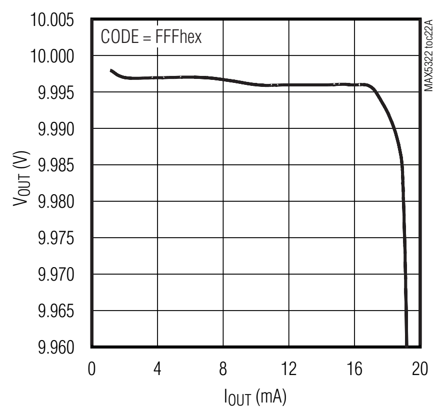
BIPOLAR SHUTDOWN CURRENT vs. TEMPERATURE



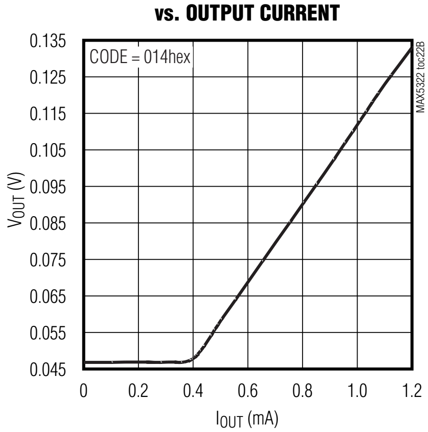
UNIPOLAR SHUTDOWN CURRENT vs. TEMPERATURE



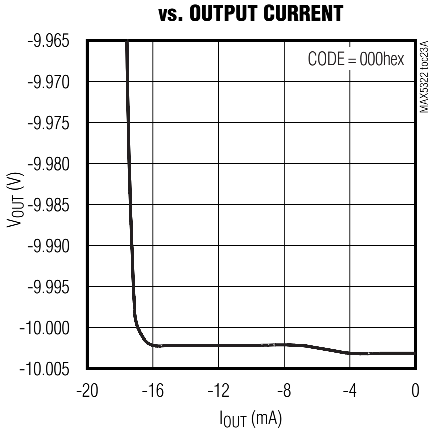
UNIPOLAR OUTPUT VOLTAGE vs. OUTPUT CURRENT



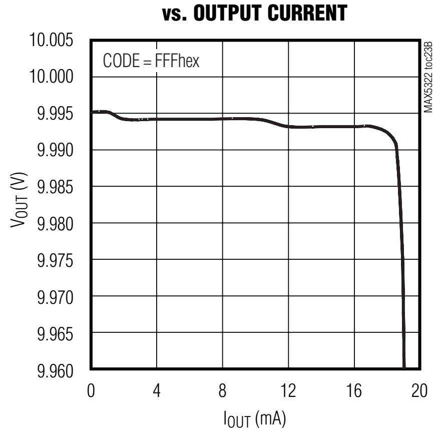
UNIPOLAR OUTPUT VOLTAGE vs. OUTPUT CURRENT



BIPOLAR OUTPUT VOLTAGE vs. OUTPUT CURRENT



BIPOLAR OUTPUT VOLTAGE vs. OUTPUT CURRENT

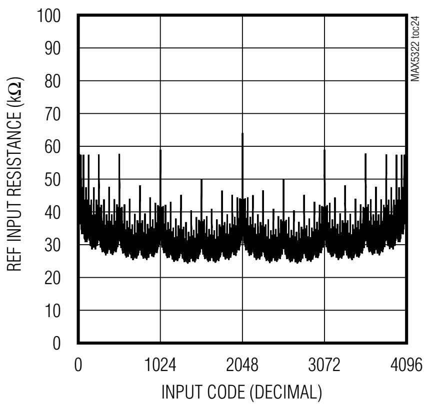


±10V, Dual, 12-Bit, Serial, Voltage-Output DAC

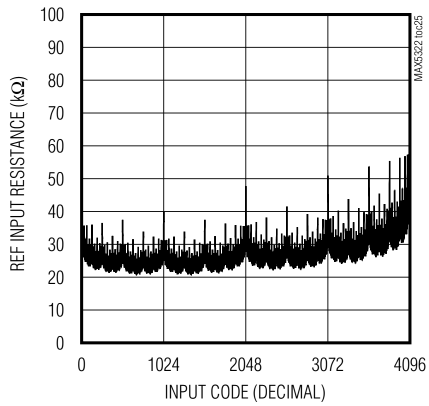
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V for bipolar graphs, V_{SS} = 0 for unipolar graphs, V_{CC} = +5V, AGND = DGND = SGND_ = 0, $V_{REF\_}$ = +5.0V, output unloaded, T_A = +25°C, all graphs apply to both unipolar and bipolar, unless otherwise noted.)

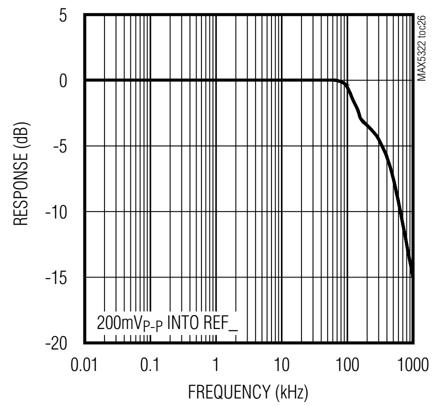
UNIPOLAR REFERENCE INPUT RESISTANCE vs. INPUT CODE



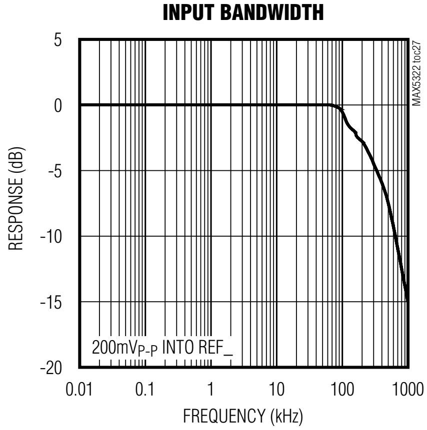
BIPOLAR REFERENCE INPUT RESISTANCE vs. INPUT CODE



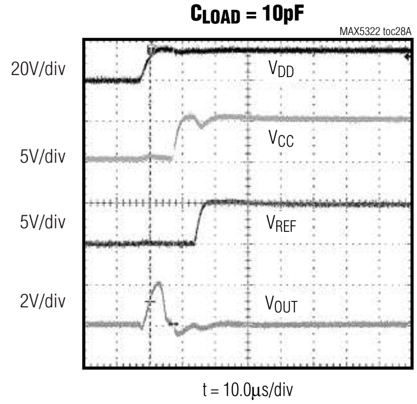
UNIPOLAR REFERENCE INPUT BANDWIDTH



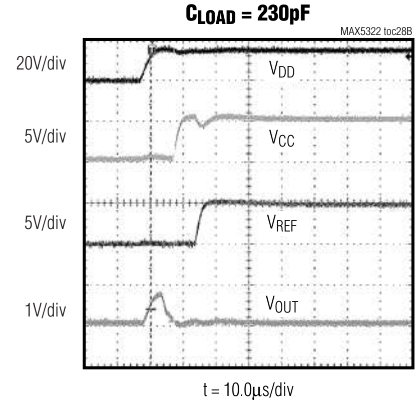
BIPOLAR REFERENCE INPUT BANDWIDTH



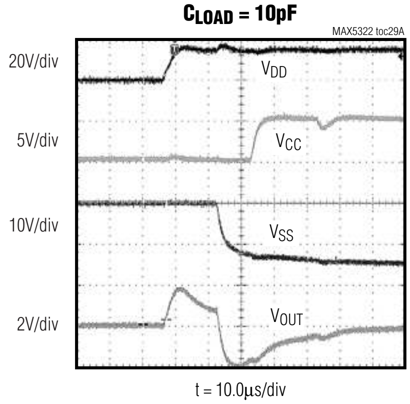
UNIPOLAR STARTUP RESPONSE, C_{LOAD} = 10pF



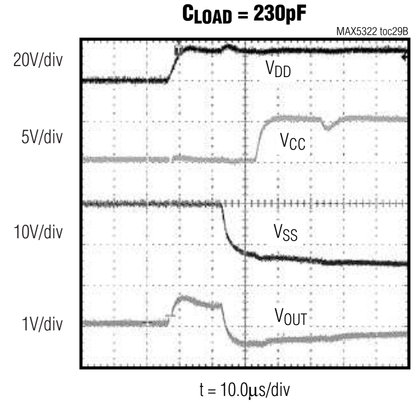
UNIPOLAR STARTUP RESPONSE, C_{LOAD} = 230pF



BIPOLAR STARTUP RESPONSE, C_{LOAD} = 10pF



BIPOLAR STARTUP RESPONSE, C_{LOAD} = 230pF

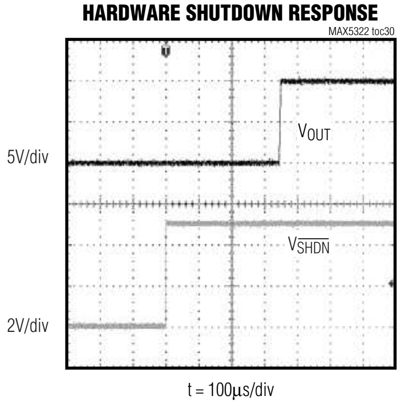


±10V, Dual, 12-Bit, Serial, Voltage-Output DAC

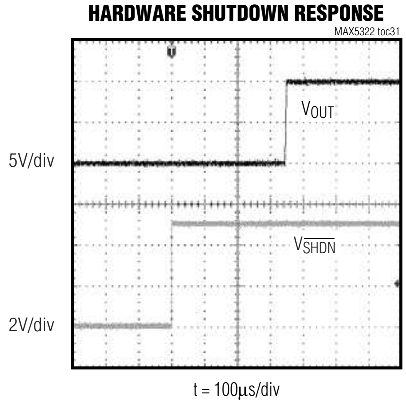
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V for bipolar graphs, V_{SS} = 0 for unipolar graphs, V_{CC} = +5V, AGND = DGND = SGND_ = 0, $V_{REF\_}$ = +5.0V, output unloaded, T_A = +25°C, all graphs apply to both unipolar and bipolar, unless otherwise noted.)

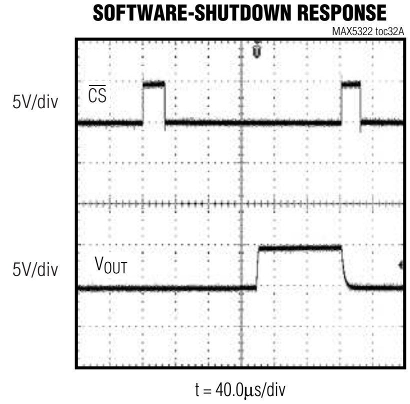
UNIPOLAR RELEASE FROM HARDWARE SHUTDOWN RESPONSE



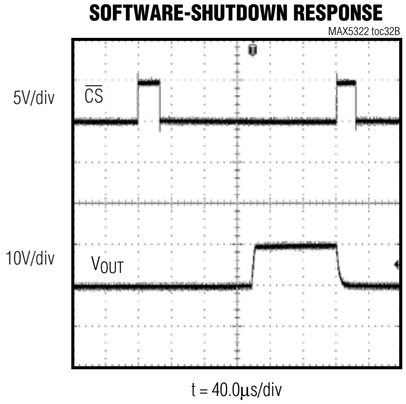
BIPOLAR RELEASE FROM HARDWARE SHUTDOWN RESPONSE



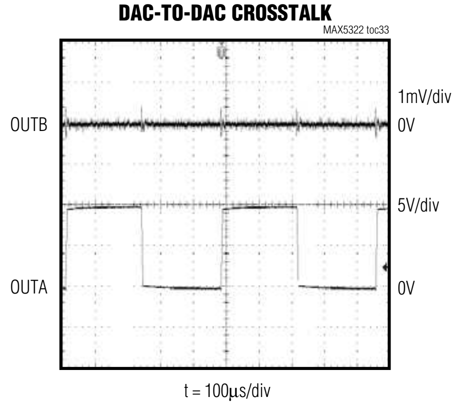
UNIPOLAR SOFTWARE-SHUTDOWN RESPONSE



BIPOLAR SOFTWARE-SHUTDOWN RESPONSE



DAC-TO-DAC CROSSTALK



Pin Description

PIN	NAME	FUNCTION
1, 2, 13–16, 27, 28	N.C.	No Connection. Not internally connected.
3	UNI/$\overline{\text{BIP}}$B	DAC B Output-Mode Selection Input. Selects unipolar or bipolar output. Logic high = unipolar, logic low = bipolar. In unipolar mode, the analog output range is 0 to 2 x V_{REF}. In bipolar mode, the analog output range is (-2 x V_{REF}) to (+2 x V_{REF}).
4	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. Pulling $\overline{\text{SHDN}}$ low forces the DAC buffers into high impedance. Drive $\overline{\text{SHDN}}$ high for normal operation.
5	$\overline{\text{LDAC}}$	Active-Low Load DAC Input. DAC A and DAC B are updated with information in the input register on the $\overline{\text{LDAC}}$ falling edge.
6	$\overline{\text{CLR}}$	Active-Low Asynchronous Clear DAC Input. Pulling $\overline{\text{CLR}}$ low clears all DACs and input registers; resets all outputs to zero.
7	DGND	Digital Ground
8	V_{CC}	Digital Power Input. Connect V_{CC} to a +2.7V to +5.5V power supply. Bypass V_{CC} to DGND with a 10µF and 0.1µF capacitor in parallel as close to the device as possible.
9	DOUT	Serial-Data Output. Data is clocked out on SCLK's falling edge. DOUT is high impedance when $\overline{\text{CS}}$ is high. Data shifted into DIN appears at DOUT 16.5 clock cycles later.
10	SCLK	Serial-Clock Input. SCLK clocks data in and out of the serial interface.
11	DIN	Serial-Data Input. Data is clocked in on the rising edge of SCLK.
12	$\overline{\text{CS}}$	Active-Low Chip-Select Input. Data is not clocked into DIN unless $\overline{\text{CS}}$ is low.
17	UNI/$\overline{\text{BIP}}$A	DAC A Output-Mode Selection. Selects unipolar or bipolar output. Logic high = unipolar, logic low = bipolar. In unipolar mode, the analog output range is 0 to 2 x V_{REF}. In bipolar mode, the analog output range is (-2 x V_{REF}) to (+2 x V_{REF}).
18	OUTA	DAC A Output
19	SGNDA	DAC A Sense Ground. Connect to AGND.
20	REFA	Reference Input for DAC A
21	V_{DD}	Positive Analog-Power Input. Connect V_{DD} to a +10.8V to +15.75V power supply. Bypass V_{DD} to AGND with a 10µF and 0.1µF capacitor in parallel as close to the device as possible.
22	REFB	DAC B Reference Input
23	AGND	Analog Ground
24	SGNDB	DAC B Sense Ground. Connect to AGND.
25	OUTB	DAC B Output
26	V_{SS}	Negative Analog-Power Input. For single-supply operation, connect V_{SS} to AGND. For dual-supply operation, connect V_{SS} to a -10.8V to -15.75V power supply and bypass V_{SS} to AGND with a 10µF and 0.1µF capacitor in parallel, as close to the device as possible.

Detailed Description

The MAX5322 dual, 12-bit DAC operates from either single or dual analog supplies. Dual ±12V to ±15V power supplies provide bipolar ±5V to ±10V outputs, or unipolar 0V to 10V outputs. Single 12V to 15V analog power supplies only provide unipolar 0 to 10V outputs. The reference inputs accept voltages from 2V to 5.25V. The DAC features INL and DNL less than ±1 LSB (max), a fast 10µs settling time, and a hardware shutdown mode that reduces current consumption to 2.8µA. The device features a 10MHz SPI-/QSPI-/MICROWIRE-compatible serial interface that operates with 3V or 5V logic, an asynchronous load input, and a serial-data output. The device offers a $\overline{CLR}$ that sets the DAC outputs to 0V. Figure 1 shows the functional diagram of the MAX5322.

Serial Interface

An SPI-/QSPI-/MICROWIRE-compatible serial interface allows complete control of the DAC through a 16-bit control word. The first 4 bits form the control bits that determine register loading and software shutdown functions. The last 12 bits form the DAC data. The 16-bit word is entered MSB first.

Table 1 shows the serial-data control-word format. Table 2 shows the interface commands. The MAX5322 can be programmed while in shutdown.

The serial interface contains five registers: a 16-bit shift register, two 12-bit input registers, and two 12-bit DAC registers (Figure 1). The shift register accepts data from the serial interface. The input registers act as holding registers for data going to the DAC registers

Table 1. Control-Word Format

CONTROL BITS				DATA BITS											
MSB															LSB
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
CONTROL BITS				DATA BITS	
C3	C2	C1	C0	D11–D0	
0	0	0	0	XXXXXXXXXXXX	No operation (NOP).
0	0	0	1	12-bit DAC data	Load both DAC registers and both input registers from the shift register. (Start both DACs with new data.)
0	0	1	0	12-bit DAC data	Load input register A from the shift register; DAC registers are unchanged.
0	0	1	1	12-bit DAC data	Load input register B from the shift register; DAC registers are unchanged.
0	1	0	0	12-bit DAC data	Load DAC register A and input register A from the shift register.
0	1	0	1	12-bit DAC data	Load DAC register B and input register B from the shift register.
0	1	1	0	XXXXXXXXXXXX	Update DAC register A from input register A (no data sent).
0	1	1	1	XXXXXXXXXXXX	Update DAC register B from input register B (no data sent).
1	0	0	0	XXXXXXXXXXXX	Shut down DAC A (provided $\overline{SHDN}$ = 1).
1	0	0	1	XXXXXXXXXXXX	Shut down DAC B (provided $\overline{SHDN}$ = 1).
1	0	1	0	XXXXXXXXXXXX	Update both DAC registers from their respective input registers. (Start both DACs with data previously stored in the input register.)
1	0	1	1	XXXXXXXXXXXX	Shut down both DACs (provided $\overline{SHDN}$ = 1).
1	1	0	0	XXXXXXXXXXXX	Power up DAC A (no change to any registers).
1	1	0	1	XXXXXXXXXXXX	Power up DAC B (no change to any registers).
1	1	1	0	XXXXXXXXXXXX	Power up both DACs (no change to any registers).
1	1	1	1	XXXXXXXXXXXX	Not used.

X = *Don't care.*

Note: *The DACs can be programmed in shutdown mode.*

and isolate the shift register from the DAC registers. The DAC registers control the DAC ladder and thus the output voltage. Any update to a DAC register updates the respective output voltage.

Data in the shift register is transferred to the input registers during the appropriate software command only. Data in the input registers is transferred to the DAC registers in two ways: using the software command, or through external logic control using the asynchronous load input ($\overline{LDAC}$). Table 2 shows the software commands that transfer the data from the shift register to the input and/or DAC registers. The $\overline{CLR}$, an external logic control, asynchronously forces all outputs to 0V, in both unipolar and bipolar modes. Interface timing is shown in Figures 2 and 3.

Wait a minimum of 100ns after $\overline{CS}$ goes high before implementing $\overline{LDAC}$ or $\overline{CLR}$. If either of these logic inputs activates during a data transfer, the incoming data is corrupted and needs to be reloaded. For software control only, tie $\overline{LDAC}$ and $\overline{CLR}$ high.

DAC Architecture

The MAX5322 uses an inverted DAC ladder architecture to convert the digital input into an analog output voltage. The digital input controls weighted switches that connect the DAC-ladder nodes to either REFA (REFB) or GND (Figure 4). The sum of the weights produces the analog equivalent of the digital-input word and is then buffered at the output.

External Reference and Transfer Functions

Connect an external reference of 2V to 5.25V to REFA and REFB. Set the output voltage range with the reference and the input code by using the equations below.

Unipolar output voltage:

$$V_{OUT\_UNI} = LSB_{UNI} \times CODE$$

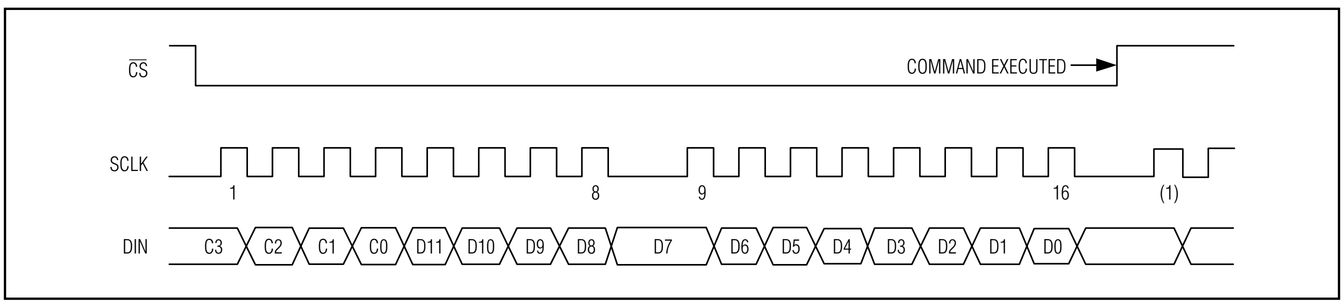


Figure 2. Serial-Interface Signals

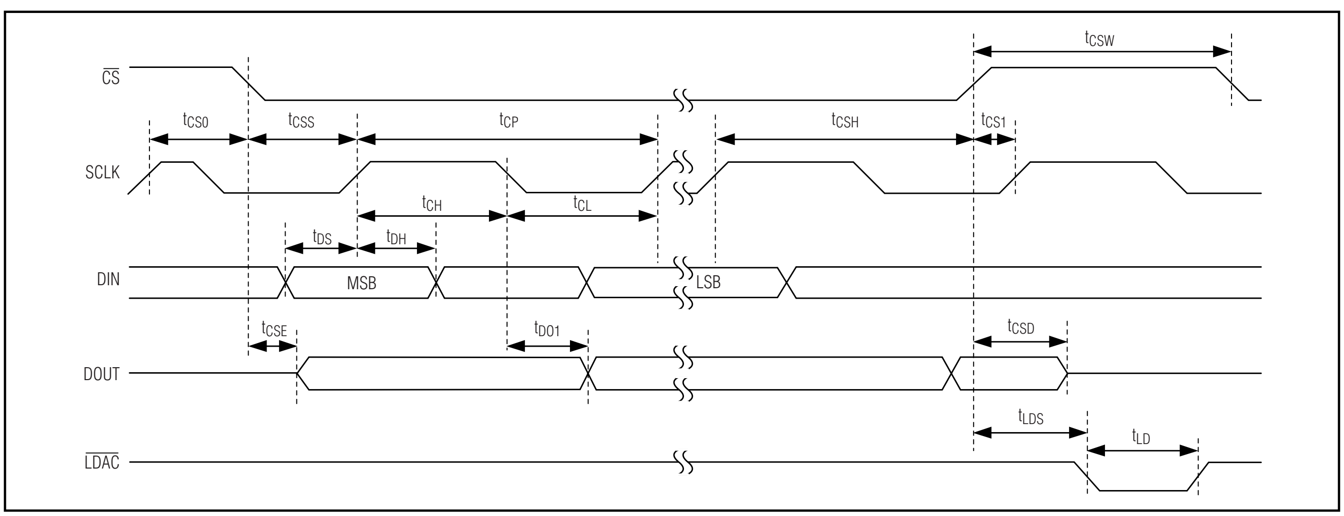


Figure 3. Serial-Interface Timing Diagram

where:

$$LSB_{UNI} = \frac{2 \times V_{REF}}{2^{12}}$$

Bipolar output voltage:

$$V_{OUT\_BIP} = (LSB_{BIP} \times CODE) - (2 \times V_{REF})$$

where:

$$LSB_{BIP} = \frac{4 \times V_{REF}}{2^{12}}$$

where V_{OUT_UNI} is the unipolar output voltage, V_{OUT_BIP} is the bipolar output voltage, LSB_{UNI} is the unipolar LSB step size, LSB_{BIP} is the bipolar LSB step size, V_{REF} is the reference voltage, and CODE is the decimal equivalent of the binary, 12-bit, DAC input code.

In either case, a 000hex input code produces the minimum output (-2 x V_{REF} for bipolar and zero for unipolar), an 800hex input code produces the midscale output (zero for bipolar and V_{REF} for unipolar), and a FFFhex input code produces the full-scale output (2 x V_{REF} for bipolar and unipolar).

Output Amplifiers

The output-amplifier section can be configured as either unipolar or bipolar by the UNI/$\overline{\text{BIP}}$ logic input. With UNI/$\overline{\text{BIP}}$A (UNI/$\overline{\text{BIP}}$B) forced low, SW1 (SW4) and SW2 (SW5) in Figure 1 are closed, and SW3 (SW6) is open. This configuration channels the DAC output through two output stages to generate the ±2 x V_{REF} output swing. The first amplifier generates the ±V_{REF} voltage range and the second amplifier gains it up by two. When configured for bipolar operation, the MAX5322 must be driven with dual ±12V to ±15V power supplies.

With UNI/$\overline{\text{BIP}}$A (UNI/$\overline{\text{BIP}}$B) forced high, switches SW1 (SW4) and SW2 (SW5) are open and SW3 (SW6) is closed. This configuration channels the DAC output through only a single gain stage to generate a 0 to 2 x V_{REF} output swing.

Daisy-Chaining

SPI-/QSPI-/MICROWIRE-compatible devices can be daisy-chained to reduce I/O lines from the host controller (Figure 7). Daisy-chain devices by connecting the DOUT of one device to the DIN of the next, and connect the SCLK of all devices to a common clock. Data is shifted out of DOUT 16.5 clock cycles after it is shifted into DIN, and is available on the rising edge of the 17th clock cycle. The SPI-/QSPI-/MICROWIRE-compatible serial interface normally works at up to 10MHz, but must be slowed to 6MHz if daisy-chaining. DOUT is high impedance when $\overline{\text{CS}}$ is high.

Shutdown

Shutdown is controlled by software commands or by the $\overline{\text{SHDN}}$ logic input. The $\overline{\text{SHDN}}$ logic input may be implemented at any time. The SPI-/QSPI-/MICROWIRE-compatible serial interface remains fully functional, and the device is programmable while shutdown. When shut down, the MAX5322 supply current reduces to 2.8µA

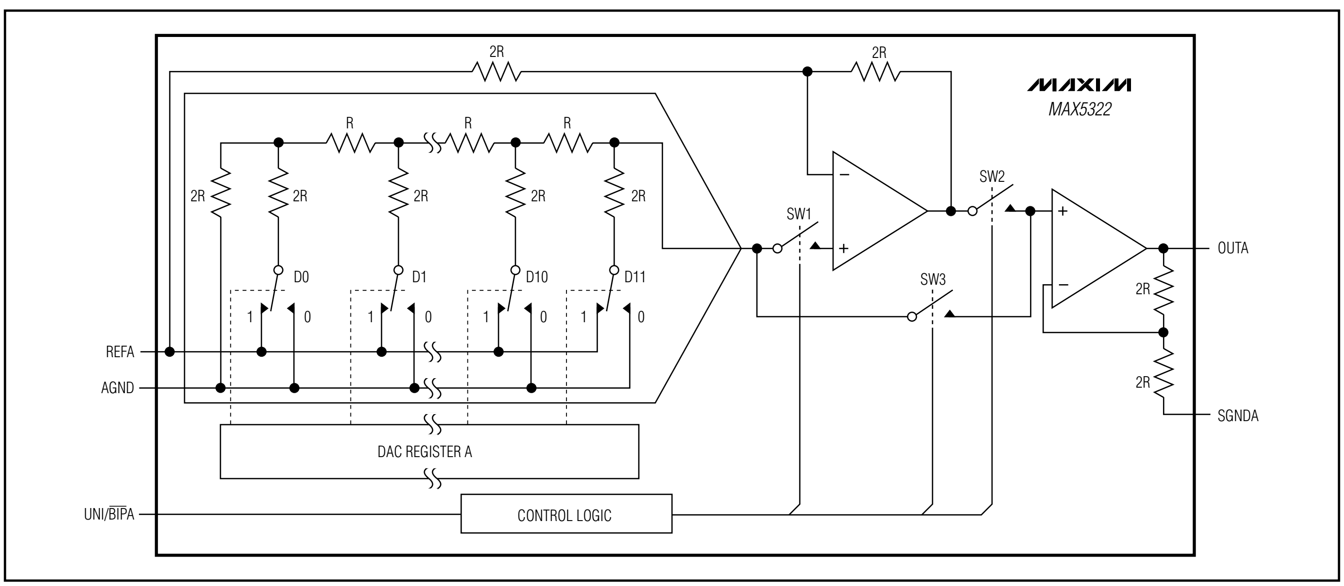


Figure 4. Basic Inverted DAC Ladder

(max), DOUT is high impedance, and OUTA and OUTB are pulled to SGNDA and SGNDB, respectively, through the internal feedback resistors of the output amplifier (Figure 1). When coming out of shutdown, or during device power-up, allow 350µs for the output to stabilize.

Applications Information

Power Supplies

A single supply of +12V to +15V is required to realize an output swing of 0 to 10V. A dual supply of ±12V to ±15V is required to realize an output swing of ±10V, and allows unipolar, 0 to +10V output if UNI/$\overline{\text{BIP}}$_ is forced high. A +3V to +5V digital power supply and two +2.000V to +5.250V external reference voltages are also required. Always bring up the reference voltages last; the other power supplies do not require sequencing.

Power-Supply Bypassing and Ground Management

Bypass V_{DD} and V_{SS} with 1.0µF and 0.1µF capacitors to AGND, and bypass V_{CC} with a 1.0µF and 0.1µF capacitors to DGND. Minimize trace lengths to reduce inductance. Digital and AC transient signals on AGND or DGND can create noise at the output. Connect AGND and DGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane or star connect all ground return paths back to AGND. Carefully lay out the traces between channels to reduce AC cross coupling and crosstalk. Wire-wrapped boards, sockets, and breadboards are not recommended.

Table 3. Output Voltage as Input Code Examples

BINARY DAC CODE	ANALOG OUTPUT	
MSB LSB	UNIPOLAR (UNI/$\overline{\text{BIP}}$_ = HIGH)	BIPOLAR (UNI/$\overline{\text{BIP}}$_ = LOW)
1111 1111 1111	+2 x V_{REF} (4095 / 4096)	+2 x V_{REF} (2047 / 2048)
1000 0000 0001	+2 x V_{REF} (2049 / 4096)	+2 x V_{REF} (1 / 2048)
1000 0000 0000	+2 x V_{REF} (2048 / 4096) = V_{REF}	0
0111 1111 1111	+2 x V_{REF} (2047 / 4096)	-2 x V_{REF} (1 / 2048)
0000 0000 0001	+2 x V_{REF} (1 / 4096)	-2 x V_{REF} (2047 / 2048)
0000 0000 0000	0	-2 x V_{REF} (2048 / 2048) = -2 x V_{REF}

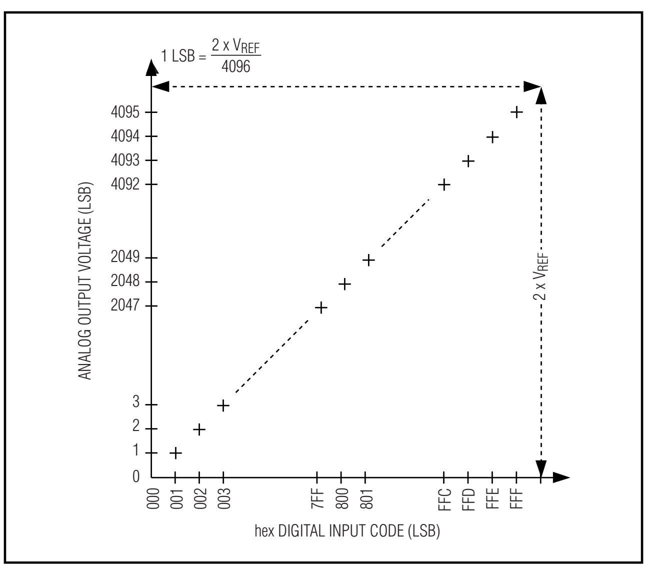


Figure 5. Unipolar Transfer Function

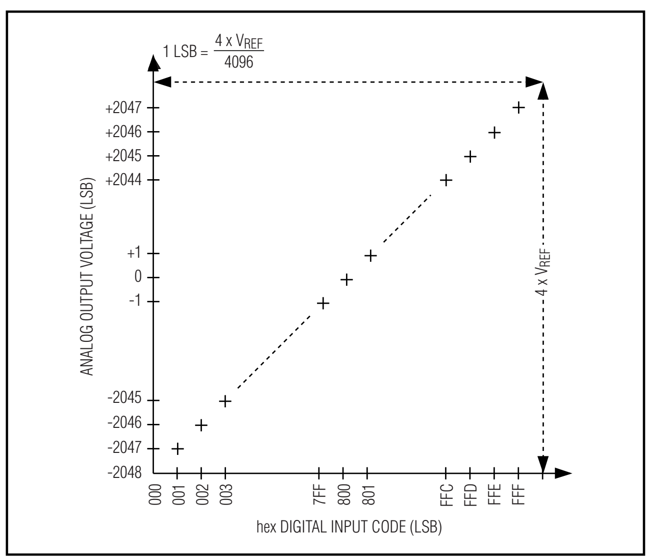


Figure 6. Bipolar Transfer Function

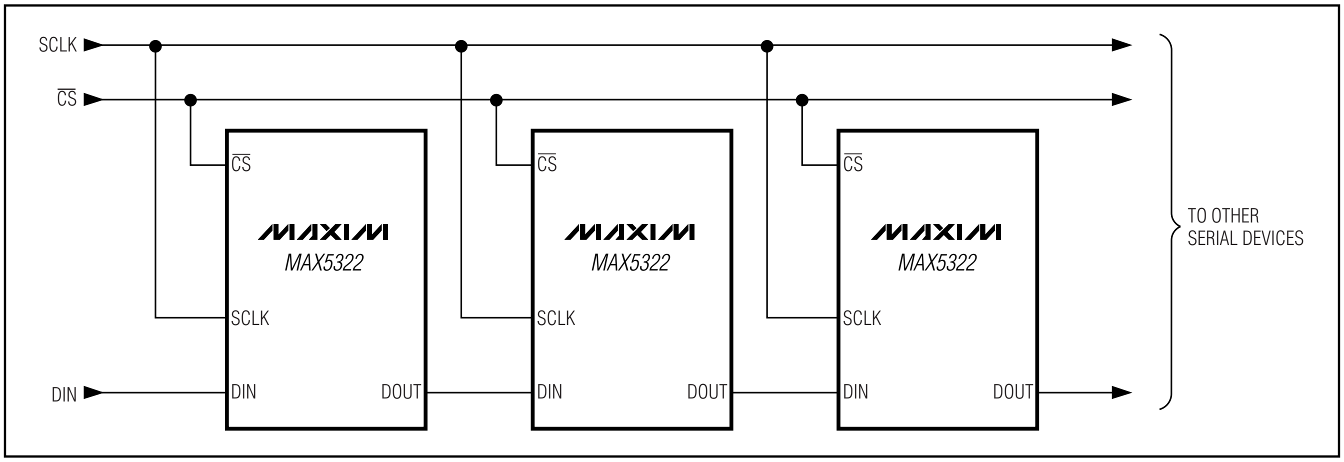
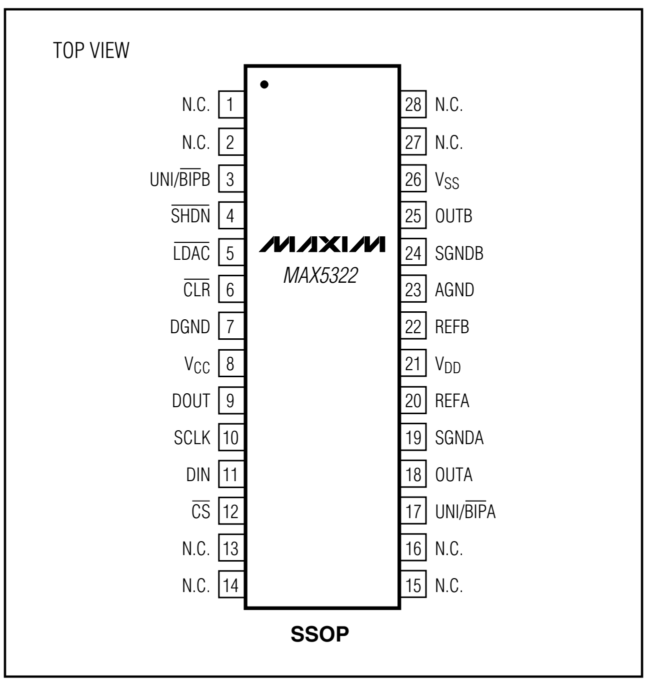


Figure 7. Daisy-Chaining Devices

Pin Configuration



Chip Information

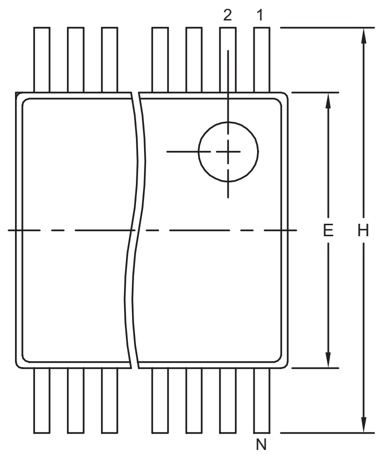
TRANSISTOR COUNT: 5914

PROCESS: BiCMOS

Package Information

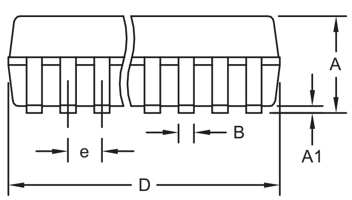
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

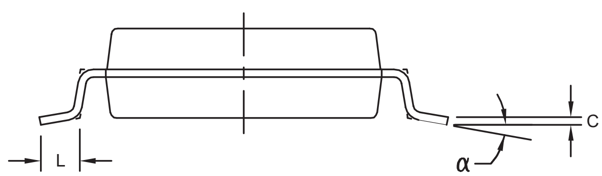
SSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SSOP, 5.3 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0056	C	1/1