19-5933; Rev 0; 6/11

DS3911

Temperature-Controlled, Nonvolatile, I²C Quad DAC

General Description

The DS3911 is a quad, 10-bit delta-sigma output, nonvolatile (NV) controller that features an on-chip temperature sensor and associated analog-to-digital converter (ADC). The integrated temperature sensor indexes the up to 2°C resolution NV lookup tables (LUTs), encompassing a -40°C to +100°C temperature range. The LUT directly drives the delta-sigma digital-to-analog converter (DAC) outputs. This flexible LUT-based architecture allows the device to provide a temperature-compensated DAC output with arbitrary slope. Programming is accomplished by an I²C-compatible interface that operates at speeds of up to 400kHz.

Applications

Active Optical Cables

Optical Transceivers

Linear and Nonlinear Compensation

Instrumentation and Industrial Controls

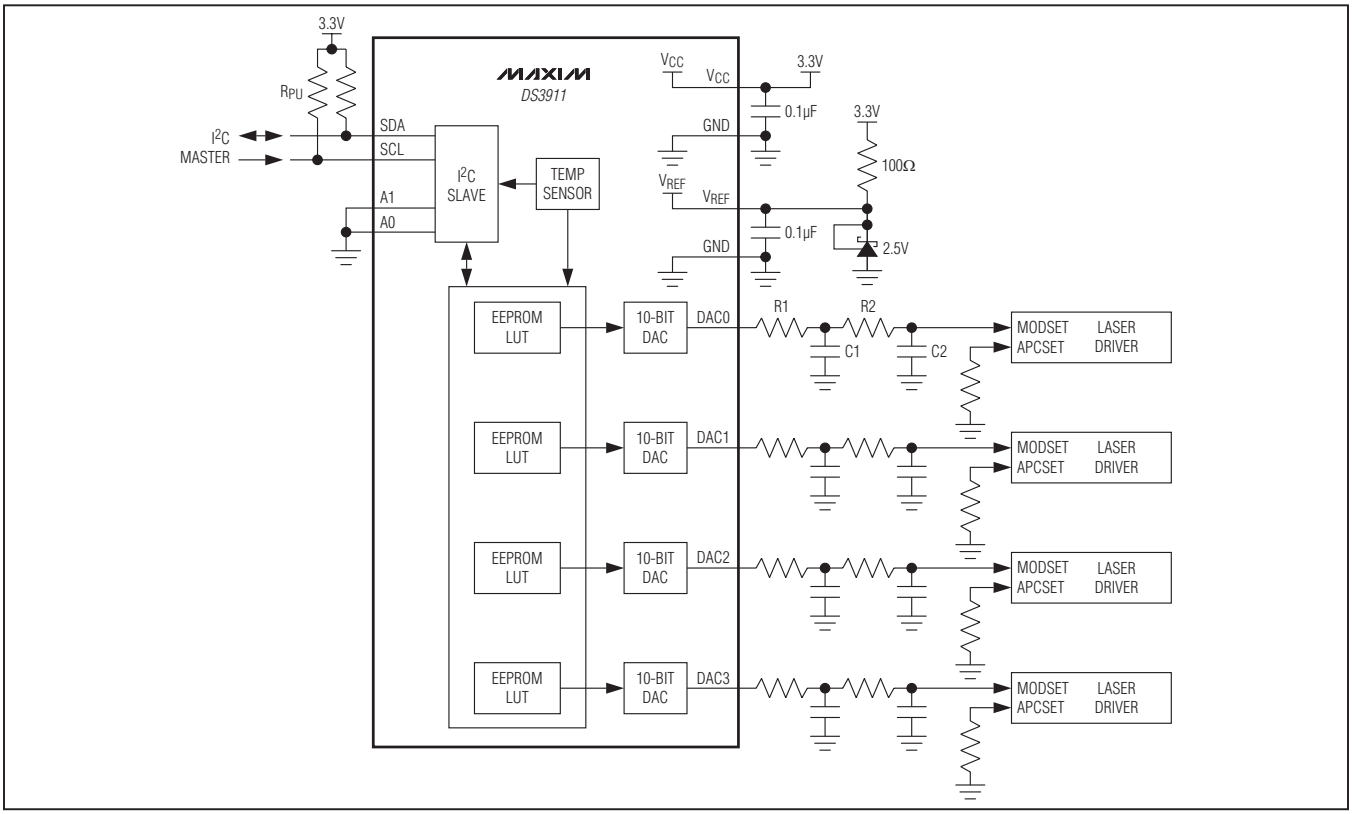
Features

- **Four 10-Bit Delta-Sigma Outputs**
- **On-Chip Temperature Sensor and ADC**
- **Four Temperature-Indexed LUTs, Up to 2°C Resolution**
- **I²C-Compatible Serial Interface**
- **Address Pins Allow Up to Four DS3911s to Share the Same I²C Bus**
- **2.8V to 5.5V Digital Supply**
- **-40°C to +100°C Operating Temperature Range**
- **3mm x 5mm, 14-Pin TDFN Package**

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maxim-ic.com/DS3911.related.

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Voltage Range on SDA, SCL, and V_{CC} Relative to GND ..... -0.3V to +6.0V
Voltage Range on DAC0, DAC1, DAC2, DAC3, V_{REF}, A0, A1 Relative to GND ..... -0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 21.7mW/°C above +70°C)..... 1739.1mW

Operating Temperature Range ..... -40°C to +100°C
Programming Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.8		5.5	V
Input Logic 1 (SCL, SDA, A0, A1)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SCL, SDA, A0, A1)	V_{IL}		-0.3		+0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.8V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (SDA, SCL, A0, A1)	I_L		-1		+1	µA
V_{CC} Supply Current	I_{CC}	(Note 2)		0.9	2.0	mA
Low-Level Output Voltage (SDA)	V_{OL}	3mA sink current	0		0.4	V
I/O Capacitance	$C_{I/O}$			5	10	pF
Power-On Recall Voltage	V_{POR}	(Note 3)	1.6		2.7	V
Power-Up Recall Delay	t_D	(Note 4)			5	ms

DAC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.8V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delta-Sigma Clock Frequency	f_{DS}			2.1		MHz
Reference Voltage Input (V_{REF})	V_{REF}	Minimum 0.1µF to GND	2.4		V_{CC}	V
Output Range			0		V_{REF}	V
Output Resolution		See the *Delta-Sigma DAC Output and Control* section for details			10	Bits
Output Impedance	R_{DS}			35	100	Ω

TEMPERATURE SENSOR CHARACTERISTICS

(V_{CC} = +2.8V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Error		T_A = -40°C to +100°C			±5	°C
Update Rate (Temperature and Supply Conversion Time)	t_{FRAME}			16		ms

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.8V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Resolution	LSB	Full-scale voltage of 6.5536V		800		µV
Input/Supply Accuracy	ACC	At factory setting		0.25	1	%FS
Input Supply Offset	V_{OS}	(Note 5)		0	5	LSB
Update Rate (Temperature and Supply Conversion Time)	t_{FRAME}			16		ms

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.8V to +5.5V, T_A = -40°C to +100°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.) (See Figure 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 6)	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Set-Up Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 7)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 7)	20 + 0.1C_B		300	ns
STOP Set-Up Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 7)			400	pF
EEPROM Write Time	t_W	(Note 8)		10	20	ms
A0, A1 Setup Time	$t_{SU:A}$	Before START	0.6			µs
A0, A1 Hold Time	$t_{HD:A}$	After STOP	0.6			µs
Input Capacitance on A0, A1, SDA, or SCL	C_I			5	10	pF
Startup time	t_{ST}				2	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.8V to +5.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles (Note 9)		T_A = +85°C	10,000			Writes
		T_A = +25°C	50,000			

Note 1: All voltages are referenced to ground. Currents entering the device are specified as positive, and currents exiting the device are specified as negative.

Note 2: I_{CC} is specified with SCL = SDA = V_{CC}, and EN bit = 1. Typical values are at V_{CC} = 3.3V and T_A = +25°C.

Note 3: This is the minimum V_{CC} voltage that causes NV memory to be recalled.

Note 4: This is the time from V_{CC} > V_{POR} until initial memory recall is complete.

Note 5: Guaranteed by design.

Note 6: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard-mode timing.

Note 7: C_B = total capacitance of one bus line in pF.

Note 8: EEPROM write time begins after a STOP condition occurs.

Note 9: Guaranteed by characterization.

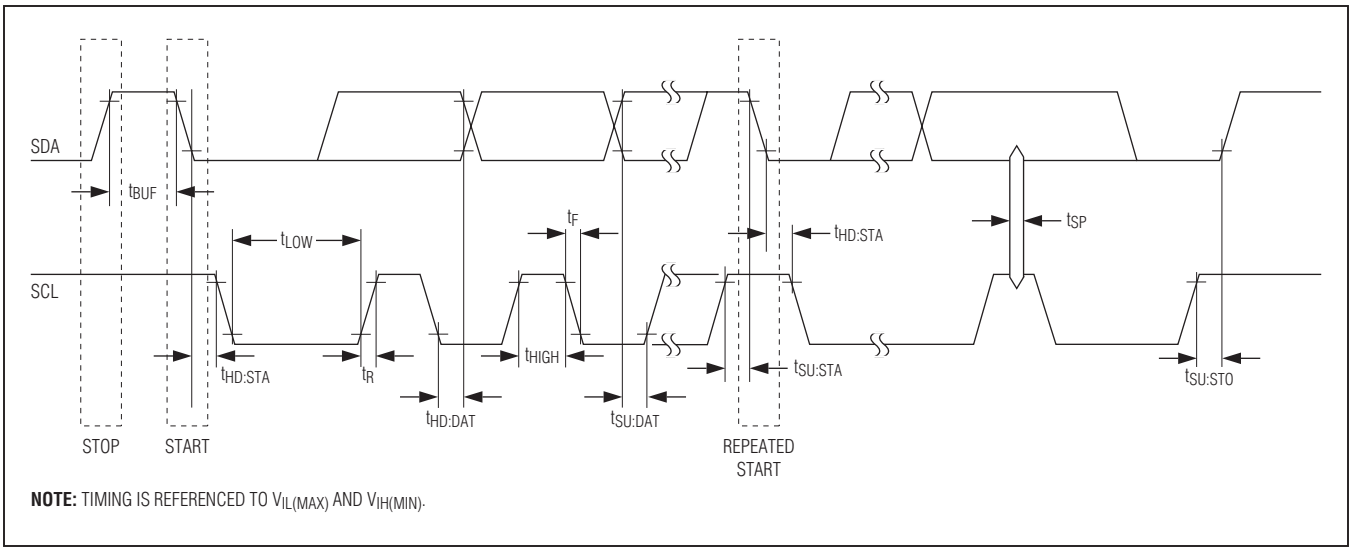
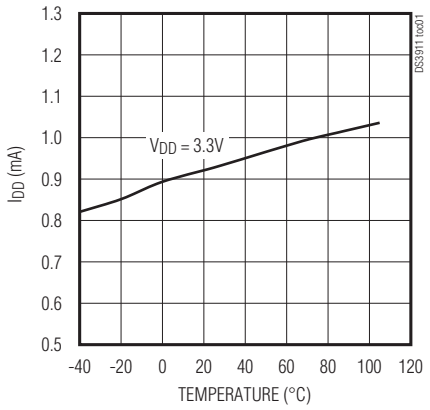


Figure 1. I²C Timing Diagram

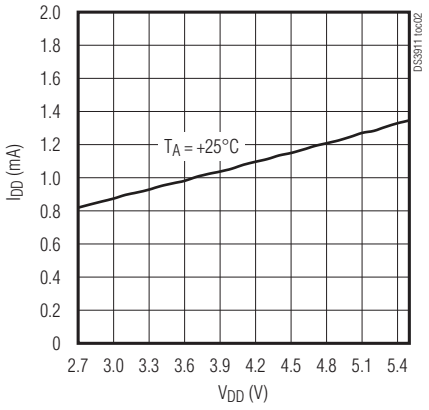
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

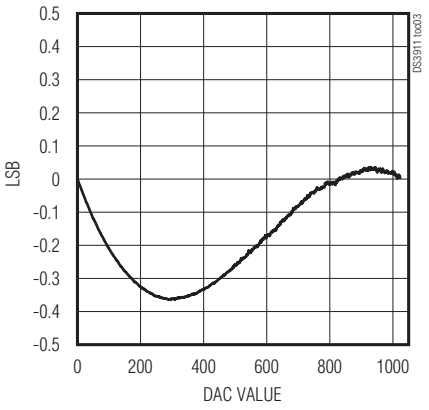
SUPPLY CURRENT vs. TEMPERATURE



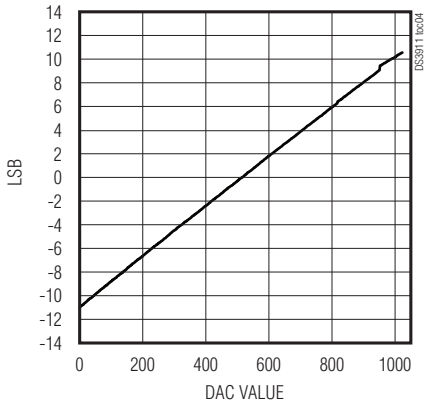
SUPPLY CURRENT vs. SUPPLY VOLTAGE



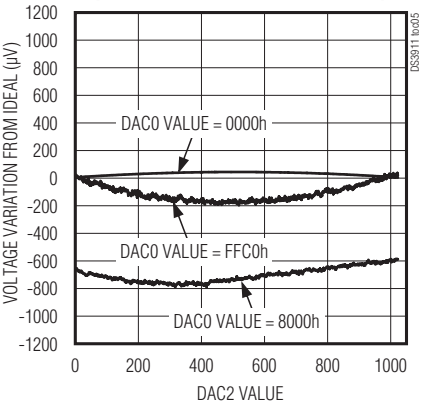
INL vs. OUTPUT CODE (VOLTAGE OUTPUT FILTER)



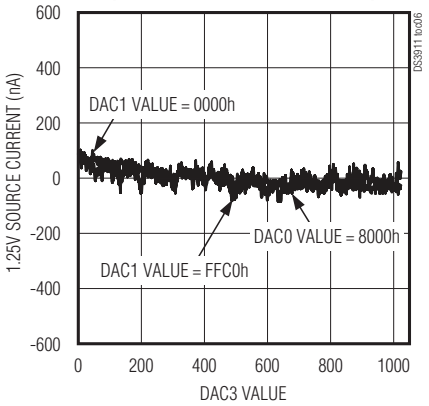
INL vs. OUTPUT CODE (CURRENT SINK FILTER)



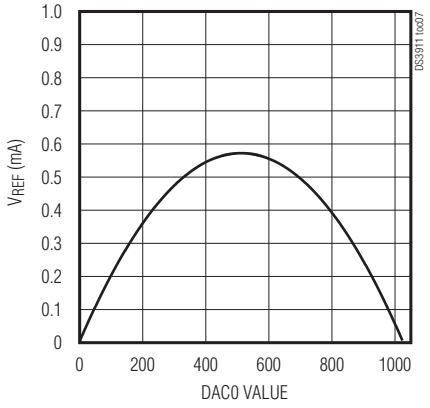
FILTERED DAC0 VOLTAGE VARIATION FROM IDEAL vs. DAC2 CODE SWEEP (BOTH VOLTAGE OUTPUT FILTERS)



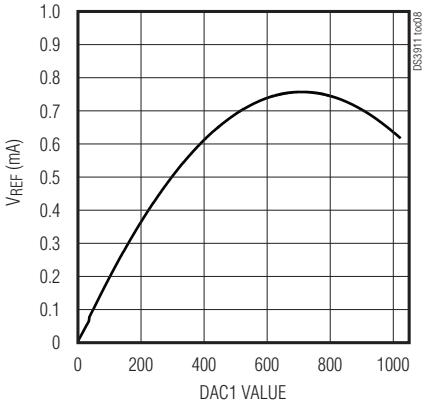
DAC1 DEVIATION FROM AVERAGE CURRENT vs. DAC3 CODE SWEEP (BOTH CURRENT SINK FILTERS)



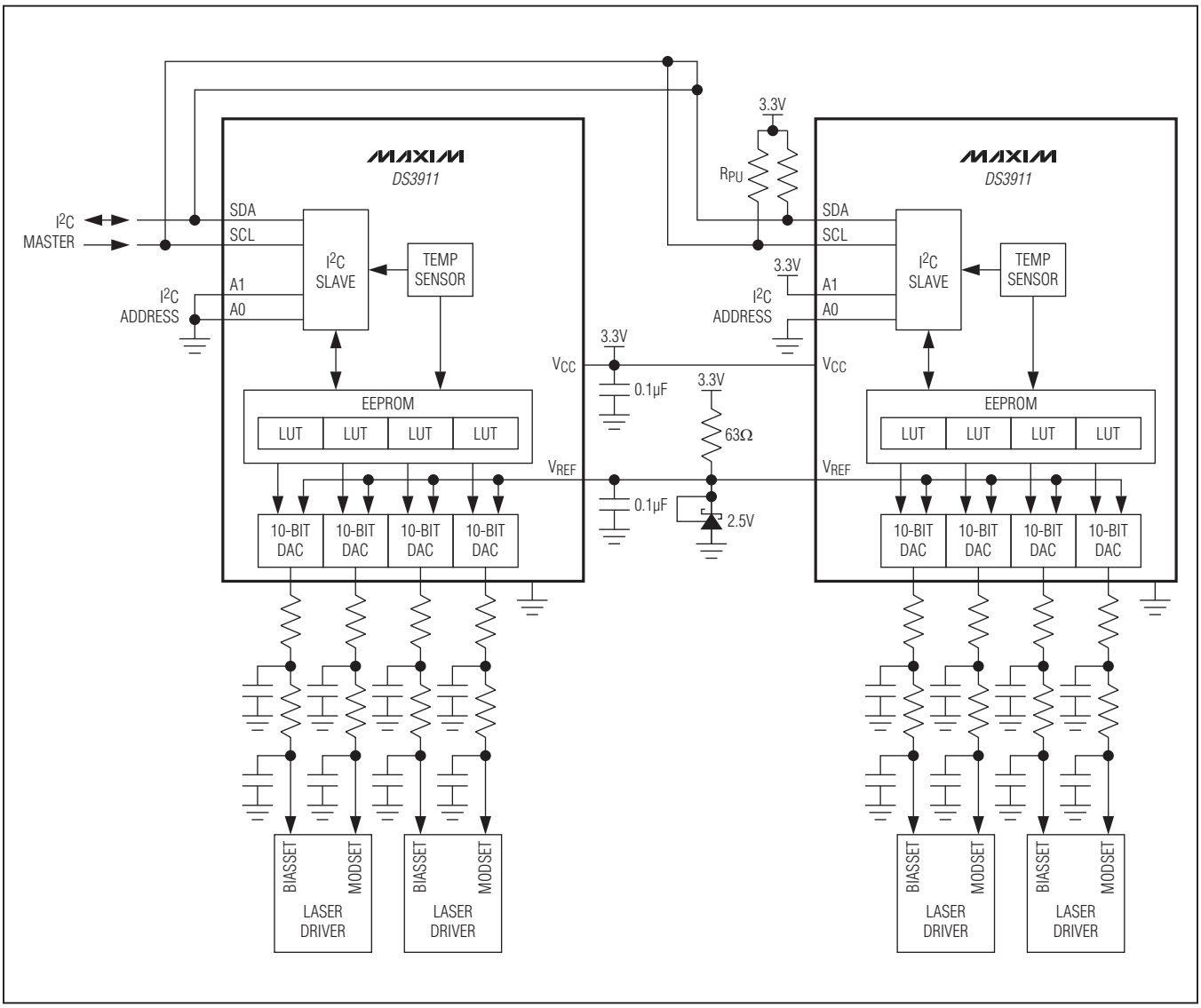
VREF CURRENT vs. DAC0 CODE SWEEP (VOLTAGE OUTPUT FILTER)



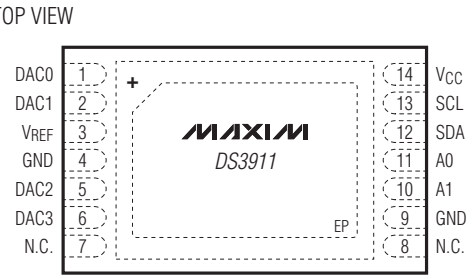
VREF CURRENT vs. DAC1 CODE SWEEP (CURRENT SINK FILTER)



Multiple Device Connection Diagram



Pin Configuration



TDFN
(3mm x 5mm)

Pin Description

PIN	NAME	TYPE	FUNCTION
1	DAC0	Output	Delta-Sigma DAC Output
2	DAC1	Output	Delta-Sigma DAC Output
3	V_{REF}	Input	DAC Reference Voltage Input
4	GND	Supply	Ground
5	DAC2	Output	Delta-Sigma DAC Output
6	DAC3	Output	Delta-Sigma DAC Output
7, 8	N.C.	—	No Internal Connection
9	GND	Supply	Ground
10	A1	Input	I²C Slave Address Input
11	A0	Input	I²C Slave Address Input
12	SDA	I/O	2-Wire Serial Data
13	SCL	Input	2-Wire Clock
14	V_{CC}	Supply	Positive Supply
—	EP	—	Exposed Pad. Connect to ground.

Detailed Description

The DS3911 operates in one of two modes: lookup table (LUT) mode or digital-to-analog converter (DAC) mode. In LUT mode, the DAC's output is controlled as a function of the temperature measured by the device's internal temperature sensor and the pulse-density modulation profile stored in the associated DAC's LUT. In DAC mode, the DAC's output is controlled by the specific DAC's DAC VALUE register (DAC0 VALUE, DAC1 VALUE, DAC2 VALUE, and DAC3 VALUE) using the I²C interface. Detailed descriptions of these modes as well as additional device features are discussed in subsequent sections.

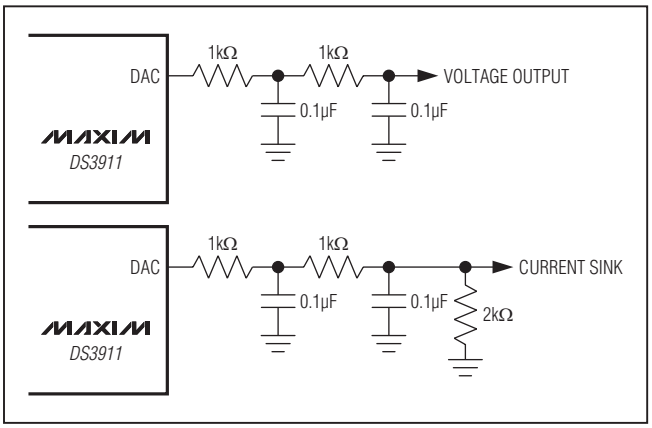


Figure 2. Recommended RC Filter for DAC Outputs

Delta-Sigma DAC Output and Control

Four delta-sigma DAC outputs are provided, DAC0 to DAC3. With the addition of an external RC filter, these outputs provide four 10-bit resolution-analog outputs with the full-scale range set by the input V_{REF} pin. Each output is either manually controlled or controlled using a temperature-indexed LUT. A delta-sigma converter produces a digital output using pulse-density modulation. It provides much lower output ripple than a standard digital PWM output, given the same clock rate and filter components.

Figure 2 shows two recommended filters. These external RC filter components are chosen to greatly reduce the output ripple while maintaining the desired response time. Using resistors smaller than the recommended values can degrade the output accuracy.

The device's delta-sigma outputs are 10 bits. For illustrative purposes, a 3-bit example is provided. Figure 3 shows each possible output of this 3-bit delta-sigma DAC.

The reference input voltage, V_{REF}, is the supply voltage for the output buffer of all DACs. The power supply connected to V_{REF} must be able to support the edge-rate requirements of the delta-sigma outputs. In a typical application, a 0.1µF capacitor should be connected between the V_{REF} and GND pins.

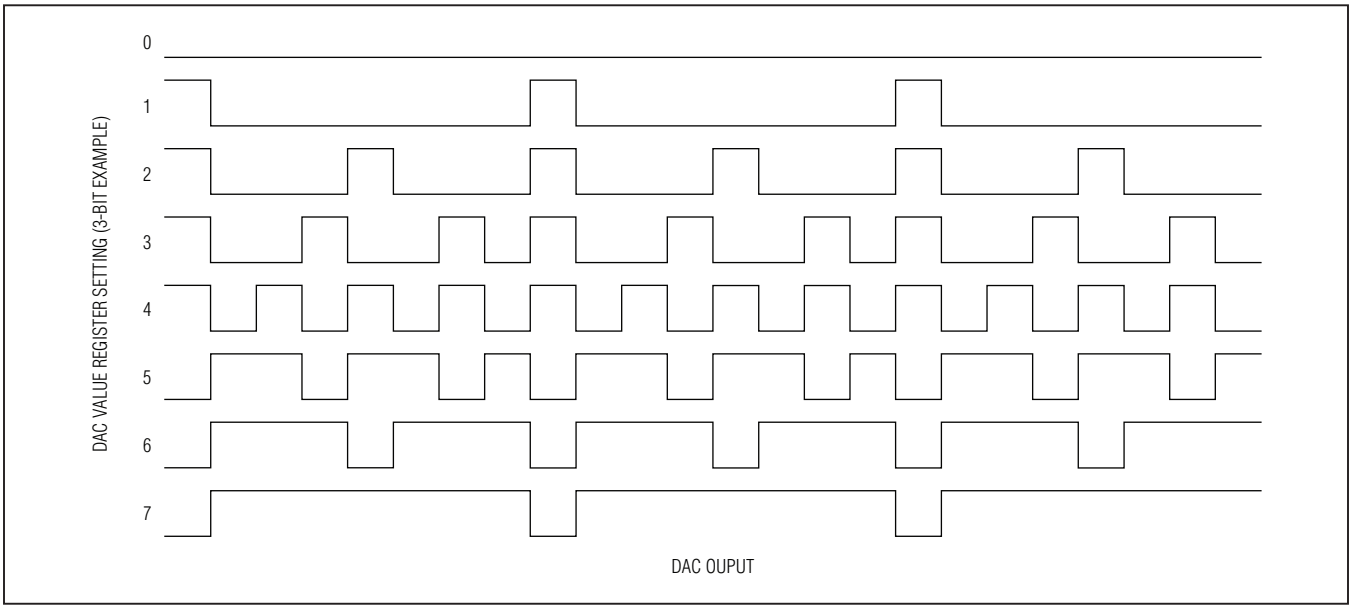


Figure 3. 3-Bit (8-Position) Delta-Sigma Example

DAC Power-On Values

Each 10-bit DAC is controlled directly by the value in its corresponding DAC VALUE register. Each DAC also has a DAC POR register that contains the power-on-reset (POR) value for the associated DAC, along with two control bits: enable (EN) and polarity (POL). See the *Lower Memory Register Descriptions* section for complete lower memory descriptions.

The DAC POR (DAC0 POR, DAC1 POR, DAC2 POR, and DAC3 POR) registers are shadowed EEPROM with functionality controlled by the shadow EEPROM bit ($\overline{SEE}$). If the $\overline{SEE}$ bit is high, the DAC POR registers function as SRAM only. If the $\overline{SEE}$ bit is low, the registers are shadowed EEPROM and EEPROM write timing, t_W, must be observed.

On power-up, the initial DAC settings are always transferred from the DAC POR registers to the corresponding DAC VALUE registers.

Manual Control Mode

On power-up, the device starts performing temperature conversions and the DAC VALUE register whose corresponding EN bit is set is updated by the LUT controller as described in the *Lookup Table Mode* section. Clearing the EN bit enables I²C writes to the corresponding DAC VALUE and disables LUT controller updates. This allows the individual DACs whose EN bit is cleared to be controlled by writing the corresponding DAC VALUE register directly.

Lookup Table Mode

The device has four nonvolatile memory tables, one for each of the four DACs. Each memory table is associated with an individual DAC as follows: Table 04h (DAC0), Table 05h (DAC1), Table 06h (DAC2), Table 07h (DAC3), and selected by setting the table select bits, TS[3:0], in the CTRL register. Each DAC memory table consists of a DAC LUT table (addresses 80h–AFh) (DAC0 LUT, DAC1 LUT, DAC2 LUT, and DAC3 LUT) and a DAC OFFSET table (addresses F8h–FFh) (DAC0 OFFSET, DAC1 OFFSET, DAC2 OFFSET, and DAC3 OFFSET). Because these four memory tables all share the same address and register mapping, the TS[3:0] bits must be used to select among them.

Each LUT address represents as little as a 2° change in temperature. Table 1 shows the full temperature-to-register mapping.

The first DAC OFFSET address corresponds to 32° of temperature. After this, every 16° of temperature converts into one DAC OFFSET address slot. Table 2 shows the full temperature-to-register mapping.

The TINDEX register points to a LUT address slot. The TINDEX register can operate in two modes, as defined by the AEN bit. When the AEN bit is cleared, I²C writes to the TINDEX register are enabled, and updates from the LUT controller are blocked. The register can be used to force DAC updates to be based on the user-selected index. The TINDEX register directly addresses the LUT

Table 1. LUT Temperature Mapping

ROW (HEX)	BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
4°C LUT								
80h	< -36°	-36°	-32°	-28°	-24°	-20°	-16°	-12°
88h	-8°	-4°	0°	+4°	+8°	+12°	+16°	+20°
90h	+24°	+28°	+32°	+36°	+40°	+44°	+48°	+52°
2°C LUT								
98h	+56°	+58°	+60°	+62°	+64°	+66°	+68°	+70°
A0h	+72°	+74°	+76°	+78°	+80°	+82°	+84°	+86°
A8h	+88°	+90°	+92°	+94°	+96°	+98°	+100°	≥ +102°

Table 2. Offset Temperature Mapping

ROW (HEX)	BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
F8h	< -8°	-8°	+8°	+24°	+40°	+56°	+72°	≥ +88°

memory locations by dropping TINDEX[7] and forcing it high. When AEN = 0, any address between 80h and FFh can be addressed. To get known results in the DAC VALUE register, TINDEX should be kept between 80h and AFh.

The device monitors the internal temperature by repeatedly polling the temperature sensor's result at a rate of t_{FRAME}. Each cycle, for the DAC whose corresponding EN bit is set, the device reads the internal temperature once, and, based on that temperature, calculates the TINDEX register. The TINDEX value corresponds directly to the LUT memory address for the given temperature ranges. The DAC OFFSET address is calculated based on the TINDEX value so only one pointer is necessary. These two locations provide the values that eventually become the 10-bit DAC input, DAC VALUE. This data that gets loaded into the DAC VALUE register is a math function of the temperature-indexed LUT value and the temperature-indexed OFFSET value, as follows:

DAC[9:0] = LUT Setting + 4 x OFFSET Setting

where the DAC[9:0] DAC control value is left-justified in the 16-bit DAC VALUE register.

DAC VALUE[15:0] = DAC[9:0] x 64

Example Calculation for DAC1:

Assumptions:

1) Temperature is 43°C.
2) DAC1 OFFSET index associated with 43°C is memory table location FCh and contains data = 2Ah.
3) DAC1 LUT index associated with 43°C is memory table location 94h and contains data = 7Bh.

DAC1 = 7Bh + 4 x 2Ah = 123h = 291

DAC1 VALUE = 291 x 64

Note: Loss of information occurs if the result of the DAC VALUE math function described above is greater than 10 bits. It is important to set the DAC VALUE and DAC OFFSET values to ensure this overflow does not occur.

The eight DAC OFFSET registers can be independently set to achieve any desired temperature coefficient (tempco) on its associated DAC. Figure 4 demonstrates

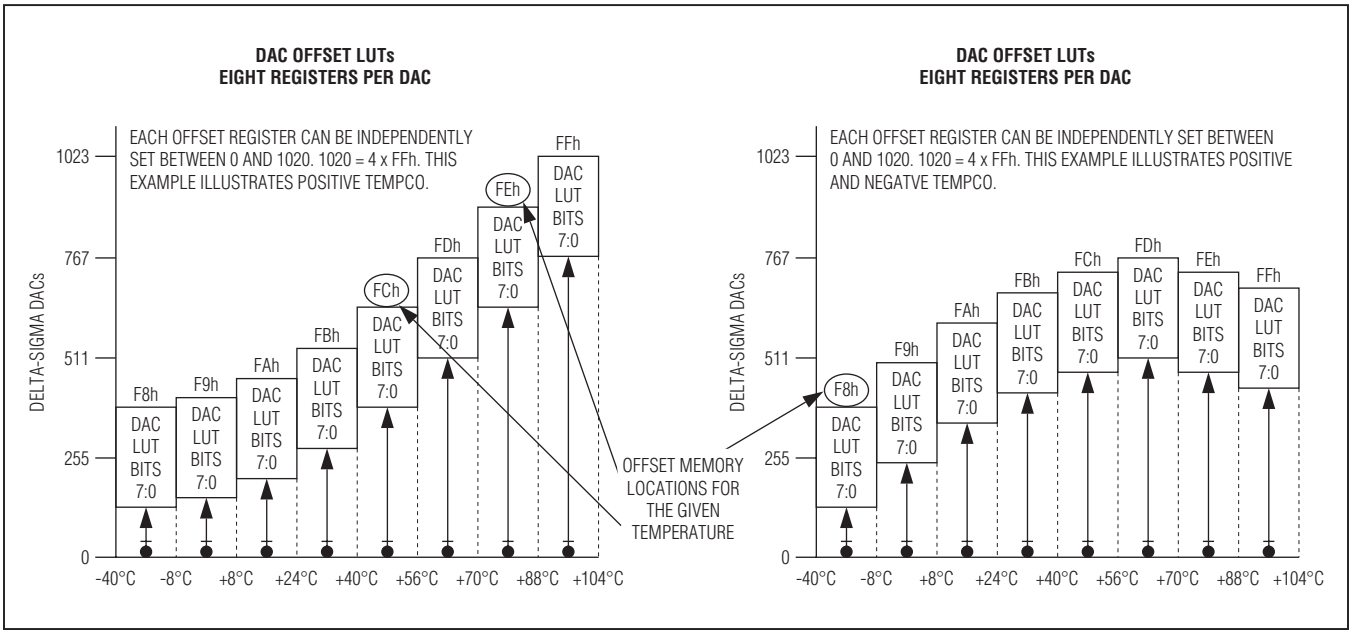


Figure 4. DAC OFFSET LUT Examples

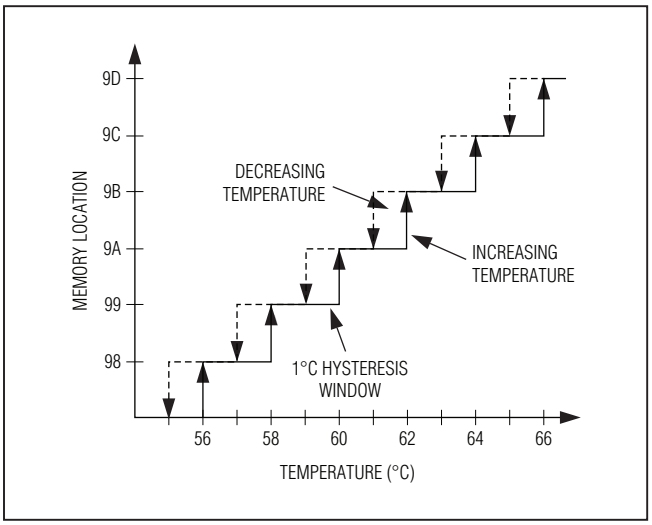


Figure 5. LUT Hysteresis

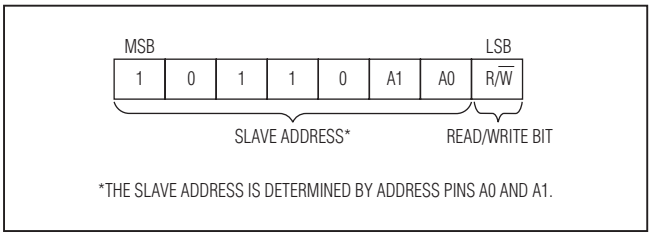


Figure 6. DS3911 Slave Address Byte

how a positive and negative tempco can be achieved by adjusting DAC OFFSET values. The DACs are updated after each temperature conversion.

The LUT features 1°C hysteresis to prevent chattering if the measured temperature falls on the boundary between two windows (Figure 5). This 1°C hysteresis is implemented in the TINDEX register value calculation by adding 1°C to temperature changes of negative slope.

Temperature Conversion and Supply Voltage Monitoring

Temperature Conversion

The device features an internal 12-bit temperature sensor that can drive the LUT and provide a measurement of the ambient temperature over I²C by reading the value stored in memory addresses 04h–05h. The sensor is functional over the entire operating temperature range, and the results are stored in signed two's-complement format with a 1/16°C resolution. See the *Lower Memory, Register 04h–05h: TEMP VALUE* section for the temperature sensor's bit weights. The DONETEMP bit located in the CTRL register indicates whether a temperature conversion has been completed since the bit was last cleared.

Supply Voltage Monitoring

The device also features an internal 13-bit supply voltage (V_{CC}) monitor. A left-justified value of the supply voltage measurement can be read over I²C at memory addresses 06h–07h. To calculate the supply voltage, simply convert the hexadecimal result into decimal and then multiply it by the LSB as shown in the *Analog Voltage Monitoring Characteristics* electrical specifications table. The DONEVCC bit located in the CTRL register indicates whether a V_{CC} conversion has been completed since the bit was last cleared.

Slave Address Byte and Address Pins

The slave address byte consists of a 7-bit slave address plus a R/$\overline{W}$ bit, as shown in Figure 6. The device's slave address is determined by the state of the A0 and A1 address pins. These pins allow up to four devices to reside on the same I²C bus. Address pins connected to GND result in a 0 in the corresponding bit position in the slave address. Conversely, address pins connected to V_{CC} result in a 1 in the corresponding bit positions. For example, the device's slave address byte is B0h when A0 and A1 are grounded. See the *I²C Serial Interface* section for more information.

I²C Serial Interface

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. See the timing diagram (Figure 1) and the *I²C AC Electrical Characteristics* table for additional information.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An acknowledge (ACK) or not-acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one (done by releasing SDA) during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data (see Figure 7). A NACK is used to terminate a read sequence, or used as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgment is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The device's slave address is determined by the state of the A0 and A1 address pins as shown in Figure 6. Address pins connected to GND result in a 0 in the corresponding bit position in the slave address. Conversely, address pins connected to V_{CC} result in a 1 in the corresponding bit positions. When the R/$\overline{W}$ bit is 0 (such as in B0h), the master is indicating it will write data to the slave. If R/$\overline{W}$ is set to 1 (B1h in this case), the master is indicating it wants to read from the slave. If an incorrect (nonmatching) slave address is written, the device assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory Address: During an I²C write operation to the device, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

See Figure 7 for I²C communication examples.

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. The master must read the slave's acknowledgement during all byte write operations.

When writing to the device, the DAC's output adjusts to the new setting once it has acknowledged the new data that is being written, and writes to the EEPROM are written following the STOP condition at the end of the write command.

Writing Multiple Bytes to a Slave: I²C write operations of multiple bytes can also be performed. During a single write sequence, up to 8 bytes in one page

can be written at one time. If more than 8 bytes are transmitted in the sequence, only the last 8 transmitted bytes are stored. After the last physical memory location in a particular page (8-byte page write), the address counter automatically wraps back to the first location in the same page for subsequent byte write operations.

Acknowledge Polling: Any time a EEPROM byte is written, the device requires the EEPROM write time (t_W) after the STOP condition to write the contents of the byte to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the device, which allows communication to continue as soon as the device is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

Reading a Single Byte from a Slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is impractical, the next method should be used to perform reads from a specified memory location.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter to a particular value. To do this, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. Recall that the master must NACK the last byte to inform the slave that no additional bytes are to be read. See Figure 7 for I²C communication examples.

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte, it must NACK to indicate the end of the transfer and generates a STOP condition. During a single read sequence of multiple

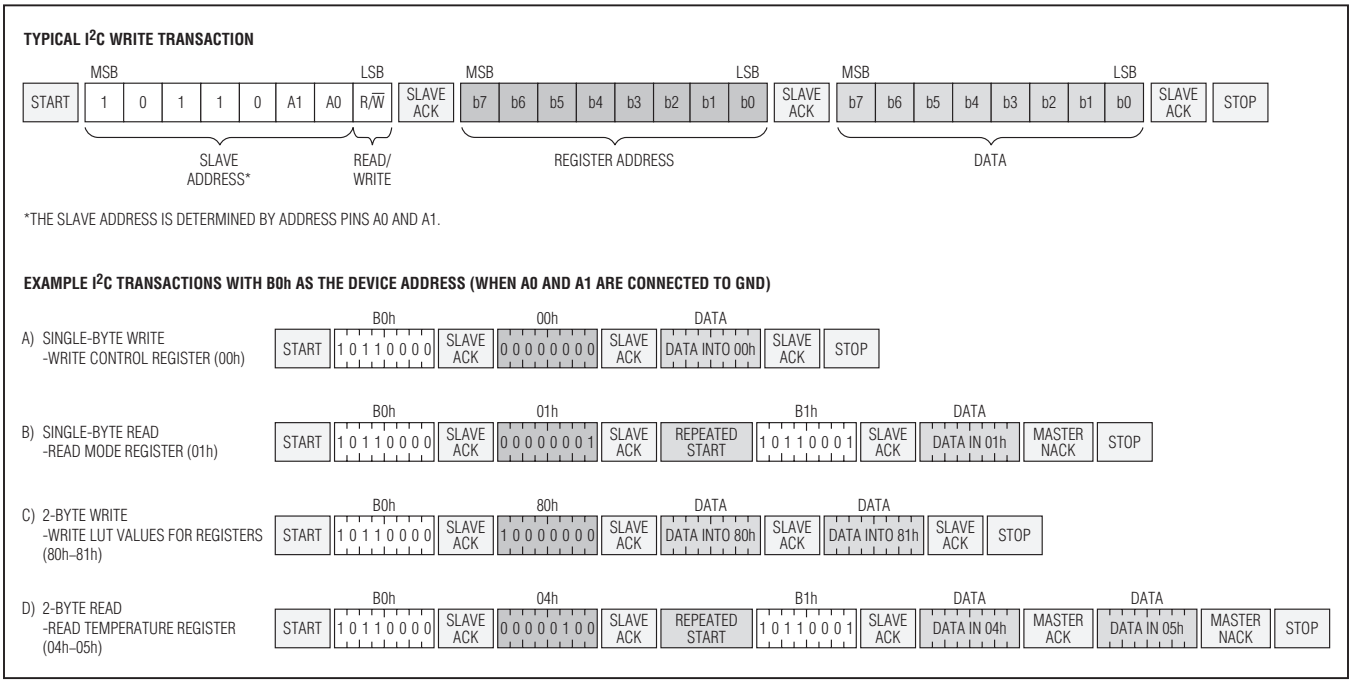


Figure 7. I²C Communication Examples

bytes, after the last address counter position of FFh is accessed, the address counter automatically wraps back to the first location, 00h. Read operations can continue indefinitely.

I²C LUT Lockout

Both the I²C port and the LUT controller have access to the LUTs. To prevent bus/data contention, the LUT controller goes into a wait state instead of accessing the LUT if the I²C port is active. Register updates and memory access are briefly described below.

- After a voltage or temperature conversion completes or the TINDEX register is calculated, the results are loaded into a shadow SRAM for the associated register by a backdoor that is not seen by the I²C port. The value is pushed forward to the SRAM cell seen by the I²C port at a later state. It is not pushed if the I²C port is active.
- After TINDEX is calculated and loaded into the shadow SRAM, the LUT controller goes into a round-robin loop where it updates the VCC VALUE, TEMP VALUE, and TINDEX registers, reads the DAC OFFSET and DAC LUT, performs the calculation, and loads the result into the DAC VALUE register. This process is where contention could occur. As such, the state machine waits until I²C is inactive before performing this process. If the I²C port were to become active for a long time period, the temperature compensation does not run.

Memory Description

The device's internal memory consists of both volatile and nonvolatile registers located in Lower Memory and four separate memory tables (Upper Memory), as shown in Figure 8.

The **Lower Memory** is addressed from 00h–7Fh. Lower Memory contains temperature reading, V_{CC} reading, status bits, control registers, table select bits, and all four DAC VALUE and DAC POR registers.

The **Upper Memory** consists of the following four memory tables. The table select bits, TS[3:0], determine which table is currently accessible through I²C at memory location 80h–FFh.

Table 04h contains a nonvolatile temperature-indexed DAC0 LUT and DAC0 OFFSET register designed to hold the pulse-density modulation profile for DAC0.

Table 05h contains a nonvolatile temperature-indexed DAC1 LUT and DAC1 OFFSET register designed to hold the pulse-density modulation profile for DAC1.

Table 06h contains a nonvolatile temperature-indexed DAC2 LUT and DAC2 OFFSET registers designed to hold the pulse-density modulation profile for DAC2.

Table 07h contains a nonvolatile temperature-indexed DAC3 LUT and DAC3 OFFSET registers designed to hold the pulse-density modulation profile for DAC3.

Shadowed EEPROM

The DAC POR memory locations are actually shadowed EEPROM and are controlled by the shadowed EEPROM bit, $\overline{SEE}$. By default, $\overline{SEE}$ is not set and these locations act as ordinary EEPROM. By setting $\overline{SEE}$ these locations function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. This also eliminates the requirement for the EEPROM write time, t_W. Because changes made with $\overline{SEE}$ enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-on value is the last value written with $\overline{SEE}$ disabled. This function can be used to speed up calibration and minimize the number of EEPROM write cycles.

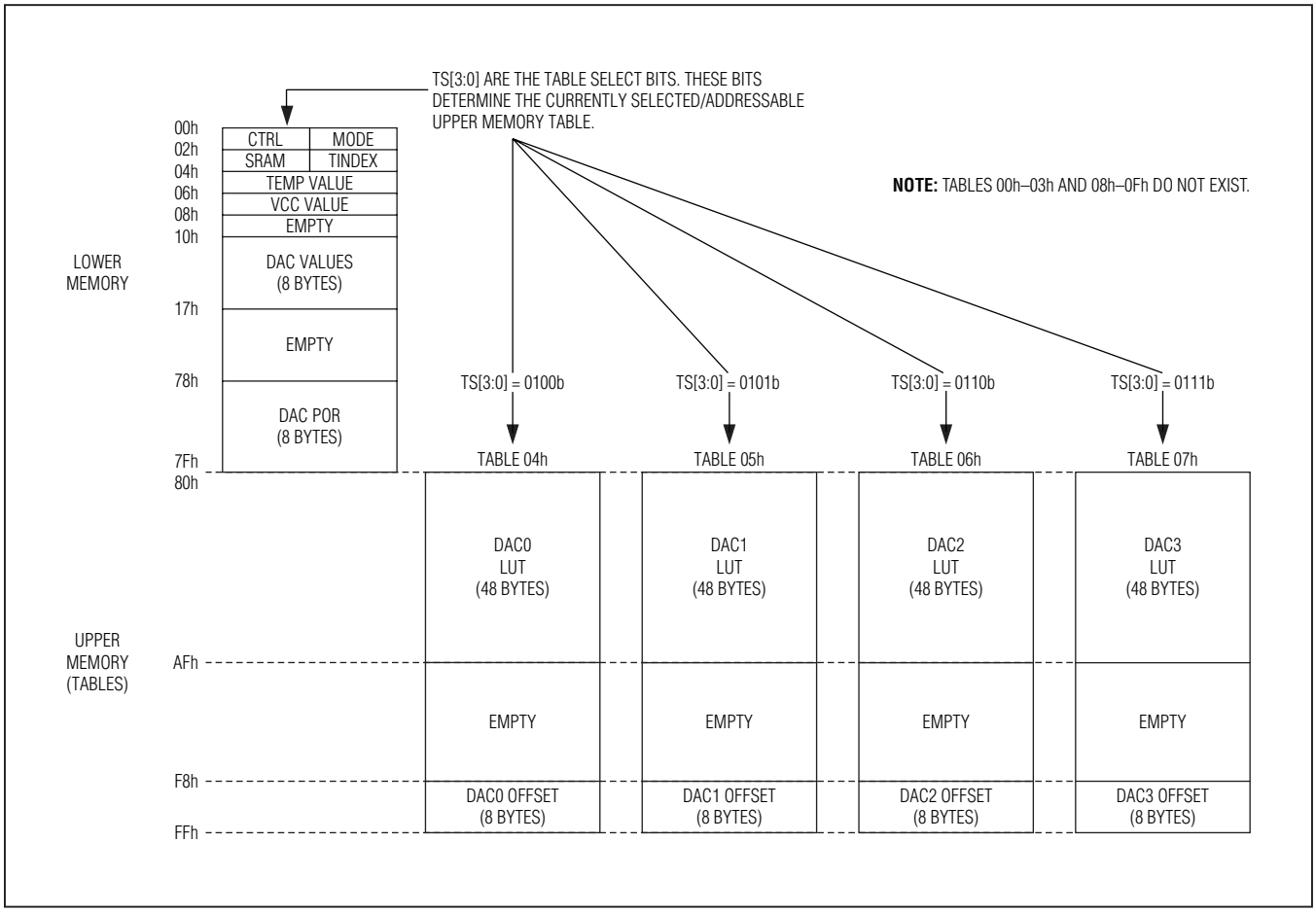


Figure 8. Memory Map

Register Description

This register map shows each byte/word (2-byte) in terms of its row and byte/word placement in the memory. The first byte in the row is located in memory at the row address (hexadecimal) in the leftmost column. Each subsequent byte/word on the row is one/two memory locations beyond the previous byte/word's address. A total of 8 bytes are present on each row. See the *Lower Memory Register Descriptions* section for more information about each of these bytes.

Lower Memory Register Map

LOWER MEMORY								
ADDR (HEX)	WORD 0		WORD 1		WORD 2		WORD 3	
	BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
00h	CTRL	MODE	SRAM	TINDEX	TEMP VALUE		VCC VALUE	
08h	—							
10h	DAC3 VALUE		DAC2 VALUE		DAC1 VALUE		DAC0 VALUE	
78h	DAC3 POR		DAC2 POR		DAC1 POR		DAC0 POR	

Lower Memory Register Descriptions

Lower Memory, Register 00h: CTRL

POWER-ON VALUE	00h
ACCESS	R/W
MEMORY TYPE	Volatile

00h	DONETEMP	DONEVCC	SRAM	SRAM	TS3	TS2	TS1	TS0
	BIT 7							BIT 0

BIT 7	**DONETEMP:** Done Temp Status 0 = Temperature conversion in progress. 1 = Temperature conversion completed since this bit was last cleared.
BIT 6	**DONEVCC:** Done V_{CC} Status 0 = V_{CC} conversion in progress. 1 = V_{CC} conversion completed since this bit was last cleared.
BITS 5:4	**SRAM:** General-Purpose SRAM. These bits have no affect on device operation.
BITS 3:0	**TS[3:0]:** Table Select. The device's memory tables are accessed by writing the desired table value in this bit field. The device only contains four addressable memory tables, 04h–07h, and therefore the values listed below are the only usable options.

TS[3:0]	TABLE SELECTED	CORRESPONDING DAC LUT
0100b	04h	0
0101b	05h	1
0110b	06h	2
0111b	07h	3

Lower Memory, Register 01h: MODE

POWER-ON VALUE	40h
ACCESS	R/W
MEMORY TYPE	Volatile

01h	$\overline{SEE}$	AEN	SRAM	SRAM	SRAM	SRAM	SRAM	SOFTTXD
	BIT 7							BIT 0

BIT 7	**$\overline{SEE}$:** Shadowed EEPROM Disable 0 = Enables EEPROM writes to the shadowed EEPROM bytes. 1 = Disables EEPROM writes to shadowed EPPROM bytes during configuration, so that the configuration of the device is not delayed by the EEPROM cycle time. Once the values are known, write this bit to a 0 and write the shadowed EEPROM locations again for data to be written to the EEPROM.
BIT 6	**AEN:** Automatic Enable 0 = The temperature-calculated index value TINDEX is writable by the user and the automatic updates of calculated indexes are disabled. This allows users to interactively test their modules by controlling the indexing for the LUTs. The recalled values from the LUTs appear in the DAC VALUE registers after the next completion of a temperature conversion. 1 = The internal temperature sensor determines the value of TINDEX.
BITS 5:1	**SRAM:** General-Purpose SRAM. These bits have no affect on device operation.
BIT 0	**SOFTTXD:** Soft Transmit Disable 0 = DACs operate normally. 1 = The DAC outputs are forced to the bit value of the POL bit, which is located in the DAC's associate DAC POR register. For example, when SOFTTXD is set and POL = 1 in the DAC0 POR register, DAC0 is forced to full-scale output, but if POL = 0, DAC0 is forced to a zero output. This applies to all four DACs.

Lower Memory, Register 02h: SRAM

POWER-ON VALUE	00h
ACCESS	R/W
MEMORY TYPE	Volatile

02h	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
	BIT 7							BIT 0

These general-purpose SRAM bits have no affect on device operation.

Lower Memory, Register 03h: TINDEX

POWER-ON VALUE	00h
ACCESS	When AEN = 1: R
ACCESS	When AEN = 0: R/W
MEMORY TYPE	Volatile

03h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The TINDEX register is the temperature indexed address pointer. The TINDEX value corresponds directly to the LUT memory address for the given temperature ranges. The DAC OFFSET address is calculated based on the TINDEX value, so only one pointer is necessary.
The pointer value is calculated based on the current temperature reading (see the below equation). The calculation uses different math depending on which LUT range (2°C or 4°C) the current temperature measurement resides in.

$$\text{TINDEX} = _{\text{temp}<56}\frac{\text{Temperature}+40}{4}+128 = _{\text{temp}\geq 56}\frac{\text{Temperature}-8}{2}+128$$

A 1°C hysteresis is implemented in the TINDEX value calculation by adding 1°C to temperature changes of negative slope.
When the AEN bit is high, the TINDEX register is read-only and the pointer is updated after the temperature and voltage conversions have completed. When the AEN bit is cleared, I²C writes to the TINDEX register are enabled and updates from the LUT controller are blocked. The register can be used to force DAC updates to be based on the user-selected index. The TINDEX register directly addresses the LUT memory locations by dropping TINDEX[7] and forcing it high. When AEN = 0, any address between 80h and FFh can be addressed. To obtain known results in the DAC VALUE register, TINDEX should be kept between 80h and AFh.
TINDEX value is clamped for temperatures below -40°C and above 102°C.

Lower Memory, Register 04h–05h: TEMP VALUE

POWER-ON VALUE	0000h
ACCESS	R
MEMORY TYPE	Volatile

04h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
05h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	0	0	0	0
	BIT 7							BIT 0

Left-justified signed two's complement direct-to-temperature measurement. The lower 4 bits always return zero. The temperature reading is clamped to -128°C and +127.9375°C.

Lower Memory, Register 06h–07h: VCC VALUE

POWER-ON VALUE	0000h
ACCESS	R
MEMORY TYPE	Volatile

06h	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}
07h	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	0	0	0
	BIT 7							BIT 0

Left-justified unsigned voltage measurement. To calculate the supply voltage, simply convert the hexadecimal result into decimal and then multiply it by the LSB as shown in the *Analog Voltage Monitoring Characteristics* electrical characteristics table. The lower 3 bits always return zero.

Lower Memory, Register 10h–11h: DAC3 VALUE
Lower Memory, Register 12h–13h: DAC2 VALUE
Lower Memory, Register 14h–15h: DAC1 VALUE
Lower Memory, Register 16h–17h: DAC0 VALUE

POWER-ON VALUE	0000h
ACCESS	When EN = 1: R
ACCESS	When EN = 0: R/W
MEMORY TYPE	Volatile

10h, 12h, 14h, 16h	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}
11h, 13h, 15h, 17h	2^{1}	2^{0}	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM
	BIT 7							BIT 0

These registers are the left- justified digital 10-bit value used for their associated DAC output. The lower 6 bits have no effect on device operation. At POR these registers are updated to the EEPROM value DAC POR. When the EN bit in DAC POR is set, this register is updated at the end of each temperature conversion, with the calculated result of values recalled from LUT and OFFSET LUT pointed to by TINDEX.

$$V_{DAC} = \frac{V_{REF}}{1024} \times \text{DAC VALUE}$$

Lower Memory, Register 78h–79h: DAC3 POR
Lower Memory, Register 7Ah–7Bh: DAC2 POR
Lower Memory, Register 7Ch–7Dh: DAC1 POR
Lower Memory, Register 7Eh–7Fh: DAC0 POR

POWER-ON VALUE	Recalled from EEPROM
ACCESS	R/W
MEMORY TYPE	Nonvolatile (SEE)

	BIT 7							BIT 0
78h, 7Ah, 7Ch, 7Eh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
79h, 7Bh, 7Dh, 7Fh	2^1	2^0	SEE	SEE	SEE	SEE	POL	EN

BITS 15:6	A left-justified, digital, 10-bit initial DAC value. During a POR these 10 bits are used to fill the corresponding DAC VALUE register.
BITS 5:2	**SEE:** These bits have no effect on device operation.
BIT 1	**POL:** Polarity Select 0 = Normal DAC mode, DAC VALUE = 3FFh results in full-scale output. 1 = Inverted DAC mode, DAC VALUE = 3FFh results in zero output.
BIT 0	**EN:** LUT Enable 0 = DAC mode: At power-on, the corresponding DAC VALUE register is loaded with the value stored in the corresponding DAC POR register. Updates from the temperature-referenced LUT and LUT OFFSET are disabled. The user can write to the DAC VALUE register to set the value for the DAC. The DAC VALUE register is R/W. 1 = LUT mode: At power-on, the corresponding DAC VALUE register is loaded with the value stored in the corresponding DAC POR register. After the first valid temperature conversion, the DAC VALUE register is loaded with the value calculated from the LUT and LUT OFFSET that correspond to the measured temperature. The DAC VALUE register is read-only.

Table 04h, Register 80h–AFh: DAC0 LUT
Table 05h, Register 80h–AFh: DAC1 LUT
Table 06h, Register 80h–AFh: DAC2 LUT
Table 07h, Register 80h–AFh: DAC3 LUT

FACTORY DEFAULT	00h
ACCESS	R/W
MEMORY TYPE	Nonvolatile

80h–AFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The DAC LUT is a set of registers assigned to hold the pulse-density modulation profile for the associated DAC. The values in this table are added to four times the corresponding value in the DAC OFFSET table to determine the set point for the associated DAC. In all four DAC tables, the DAC LUT registers are formatted the same. Beginning at -40°C, the LUT increments in 4°C steps per address until the temperature reaches 56°C, then it increments in 2°C steps until it clamps at 102°C. See the *LUT Temperature Mapping* table for full register-to-temperature mapping. Register 80h defines the -40°C to -36°C DAC LUT value, register 81h defines the -36°C to -32°C DAC LUT value, and so on.

LUT TEMPERATURE MAPPING								
ROW (HEX)	**BYTE 0**	**BYTE 1**	**BYTE 2**	**BYTE 3**	**BYTE 4**	**BYTE 5**	**BYTE 6**	**BYTE 7**
4°C LUT								
80h	< -36°	-36°	-32°	-28°	-24°	-20°	-16°	-12°
88h	-8°	-4°	0°	+4°	+8°	+12°	+16°	+20°
90h	+24°	+28°	+32°	+36°	+40°	+44°	+48°	+52°
2°C LUT								
98h	+56°	+58°	+60°	+62°	+64°	+66°	+68°	+70°
A0h	+72°	+74°	+76°	+78°	+80°	+82°	+84°	+86°
A8h	+88°	+90°	+92°	+94°	+96°	+98°	+100°	≥ +102°

Table 04h, Register F8h–FFh: DAC0 OFFSET
Table 05h, Register F8h–FFh: DAC1 OFFSET
Table 06h, Register F8h–FFh: DAC2 OFFSET
Table 07h, Register F8h–FFh: DAC3 OFFSET

FACTORY DEFAULT	00h
ACCESS	R/W
MEMORY TYPE	Nonvolatile

F8h–FFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The DAC OFFSET is a set of registers assigned to hold the pulse-density modulation profile for the associated DAC. The values in this table are multiplied by four and added to the corresponding value in the LUT table to determine the set point for the associated DAC. In all four DAC tables, the DAC OFFSET registers are formatted the same. The OFFSET registers increase in 16°C steps from -8°C to +88°C. Below -8°C the DAC OFFSET is indexed at 0xF8. See the *Offset Temperature Mapping* table for full register to temperature mapping. Register F8h defines the -40°C to -8°C DAC OFFSET value, register F9h defines the -8°C to +8°C DAC OFFSET value, and so on.

OFFSET TEMPERATURE MAPPING								
ROW (HEX)	**BYTE 0**	**BYTE 1**	**BYTE 2**	**BYTE 3**	**BYTE 4**	**BYTE 5**	**BYTE 6**	**BYTE 7**
F8h	< -8°	-8°	+8°	+24°	+40°	+56°	+72°	≥ +88°

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS3911, decouple the power supply with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications. Likewise, a decoupling capacitor should be placed from V_{REF} to GND.

SDA and SCL Pullup Resistors

SDA is an I/O with an open-collector output that requires a pullup resistor to realize high-logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I²C AC Electrical Characteristics* table are within specification. A typical value for the pullup resistors is 4.7kΩ.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3911T+	-40°C to +100°C	14 TDFN-EP*
DS3911T+T	-40°C to +100°C	14 TDFN-EP*

Note: *Contact the factory about CSBGA version availability.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TDFN-EP	T1435N+1	21-0253	90-0246

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—