



Low-Voltage, Quad, SPDT, CMOS Analog Switch

MAX394

General Description

The MAX394 is a precision, low-voltage, quad, single-pole/double-throw (SPDT) analog switch. The four independent switches operate with bipolar supplies ranging from $\pm 2.7V$ to $\pm 8V$, or with a single supply of $+2.7V$ to $+15V$. The MAX394 offers low on-resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the analog signal range ($\Delta 4\Omega$ max). It also offers break-before-make switching (10ns typical), with turn-off times less than 75ns and turn-on times less than 130ns. The MAX394 is ideal for portable operation since quiescent current runs less than $1\mu A$ with all inputs high or low.

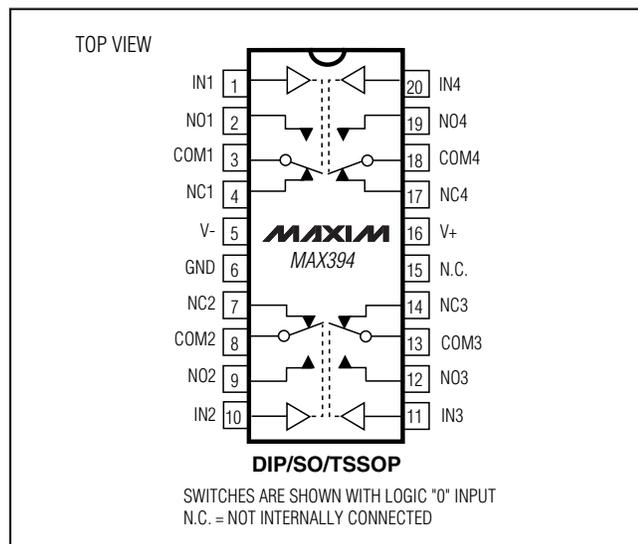
This monolithic, quad switch is fabricated with Maxim's low voltage silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption ($10\mu W$), and electrostatic discharge (ESD) greater than 2000V.

Logic inputs are TTL and CMOS compatible and guaranteed over a $+0.8V$ to $+2.4V$ range for supply voltages up to $+8V$. When supplies exceed $+8V$, the inputs are typically $+0.8V$ to $+4V$. Logic inputs and switched analog signals can range anywhere between the supply voltages without damage.

Applications

Test Equipment	Portable Instruments
Communications Systems	Audio Signal Routing
PBX, PABX	Set-Top Boxes
Heads-Up Displays	

Pin Configuration



Features

- ◆ Low On-Resistance, $< 17\Omega$ Typical (35Ω max)
- ◆ Guaranteed Matched On-Resistance Between Channels, $< 2\Omega$
- ◆ Guaranteed Flat On-Resistance over Analog Signal Range, $\Delta 4\Omega$ Max
- ◆ Guaranteed Charge Injection $< 10pC$
- ◆ Guaranteed Off-Channel Leakage $< 2.5nA$ at $+85^\circ C$
- ◆ ESD Guaranteed $> 2000V$ per Method 3015.7
- ◆ Single-Supply Operation ($+2.7V$ to $+15V$)
Bipolar-Supply Operation ($\pm 2.7V$ to $\pm 8V$)
- ◆ TTL/CMOS-Logic Compatibility
- ◆ Rail-to-Rail Analog Signal Handling Capability
- ◆ Pin Compatible with MAX333, MAX333A

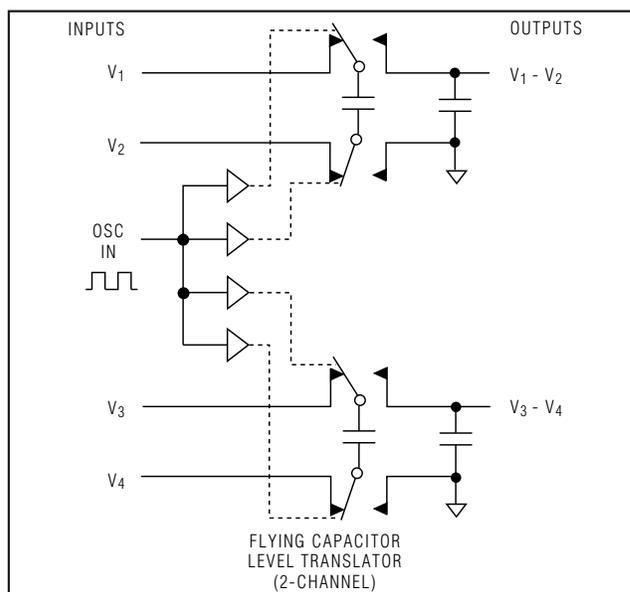
Ordering Information

PART	TEMPERATURE	PIN-PACKAGE
MAX394CPP	$0^\circ C$ to $+70^\circ C$	20 Plastic DIP
MAX394CWP	$0^\circ C$ to $+70^\circ C$	20 Wide SO
MAX394C/D	$0^\circ C$ to $+70^\circ C$	Dice*
MAX394EPP	$-40^\circ C$ to $+85^\circ C$	20 Plastic DIP
MAX394EWP	$-40^\circ C$ to $+85^\circ C$	20 Wide SO
MAX394EUP	$-40^\circ C$ to $+85^\circ C$	20 TSSOP
MAX394MJP	$-55^\circ C$ to $+85^\circ C$	20 CERDIP**
MAX394MWP/PR	$-55^\circ C$ to $+125^\circ C$	20 Wide SO**
MAX394MWP/PR-T	$-55^\circ C$ to $+125^\circ C$	20 Wide SO**

*Contact factory for dice specifications.

**Contact factory for availability.

Typical Operating Circuit



Low-Voltage, Quad, SPDT, CMOS Analog Switch

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND

V+-0.3V to +17V
V-+0.3V to -17V
V+ to V--0.3V to +17V
COM_, NO_, NC_, IN_ (Note 1)(V- - 2V) to (V+ + 2V) or 30mA, whichever occurs first

Continuous Current, Any Pin.....30mA

Peak Current, Any Pin
(pulsed at 1ms, 10% duty cycle max)100mA

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)

Plastic DIP (derate 10.53mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$)842mW
Narrow SO (derate 8.70mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$)696mW
CERDIP (derate 10.00mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$)800mW
TSSOP (derate 11.00mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$)879mW

Operating Temperature Ranges

MAX394C_P0 $^\circ\text{C}$ to +70 $^\circ\text{C}$
MAX394E_P-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
MAX394MJP-55 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Storage Temperature Range-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (soldering, 10s)+300 $^\circ\text{C}$

Note 1: Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 5V \pm 10%, V- = -5V \pm 10%, GND = 0V, $V_{\text{INH}} = 2.4\text{V}$, $V_{\text{INL}} = 0.8\text{V}$, $T_A = T_{\text{MIN}}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP. RANGE	MIN	TYP (Note 2)	MAX	UNITS	
SWITCH								
Analog Signal Range	V_{COM} , V_{NO} , V_{NC}	(Note 3)		V-		V+	V	
On-Resistance	R_{ON}	$V_+ = 4.5\text{V}$, $V_- = -4.5\text{V}$, V_{NC} or $V_{\text{NO}} = \pm 3.5\text{V}$, $I_{\text{COM}} = 10\text{mA}$, $V_{\text{INH}} = 2.4\text{V}$, $V_{\text{INL}} = 0.8\text{V}$	$T_A = +25^\circ\text{C}$	C, E	20	35	Ω	
			$T_A = T_{\text{MIN}}$ to T_{MAX}	M	20	30		
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V_{NC} or $V_{\text{NO}} = \pm 3\text{V}$, $I_{\text{COM}} = 10\text{mA}$, $V_+ = 5\text{V}$, $V_- = -5\text{V}$	$T_A = +25^\circ\text{C}$	C, E, M	0.5	2	Ω	
			$T_A = T_{\text{MIN}}$ to T_{MAX}	C, E, M		4		
On-Resistance Flatness (Note 4)	$R_{\text{FLAT(ON)}}$	V_{NC} or $V_{\text{NO}} = 3\text{V}$, 0V, -3V; $I_{\text{COM}} = 10\text{mA}$, $V_+ = 5\text{V}$; $V_- = -5\text{V}$	$T_A = +25^\circ\text{C}$	C, E, M		4	Ω	
			$T_A = T_{\text{MIN}}$ to T_{MAX}	C, E, M		6		
NC or NO Off-Leakage Current (Note 5)	$I_{\text{NC(OFF)}}$ or $I_{\text{NO(OFF)}}$	$V_{\text{COM}} = \pm 4.5\text{V}$, V_{NC} or $V_{\text{NO}} = \pm 4.5\text{V}$, $V_+ = 5.5\text{V}$, $V_- = -5.5\text{V}$	$T_A = +25^\circ\text{C}$	C, E	-0.2	-0.01	+0.2	nA
				M	-0.1	-0.01	+0.1	
			$T_A = T_{\text{MIN}}$ to T_{MAX}	C, E	-2.5		+2.5	
				M	-20		+20	
COM Leakage Current (Note 5)	$I_{\text{COM(ON)}}$	$V_{\text{COM}} = \pm 4.5\text{V}$, V_{NC} or $V_{\text{NO}} = \pm 4.5\text{V}$, $V_+ = 5.5\text{V}$, $V_- = -5.5\text{V}$	$T_A = +25^\circ\text{C}$	C, E	-0.4	-0.04	+0.4	nA
				M	-0.2	-0.04	+0.2	
			$T_A = T_{\text{MIN}}$ to T_{MAX}	C, E	-5.0		+5.0	
				M	-20		+20	

Low-Voltage, Quad, SPDT, CMOS Analog Switch

MAX394

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 5V ±10%, V- = -5V ±10%, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT							
Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4V, all others = 0.8V		-1.0	+0.005	+1.0	μA
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8V, all others = 2.4V		-1.0	+0.005	+1.0	μA
Logic High Input Voltage	V _{A_H}		T _A = T _{MIN} to T _{MAX}	2.4			V
Logic Low Input Voltage	V _{A_L}		T _A = T _{MIN} to T _{MAX}			0.8	V
DYNAMIC							
Turn-On Time	t _{ON}	V _{COM} = 3V, Figure 2	T _A = +25°C	82	130		ns
			T _A = T _{MIN} to T _{MAX}		175		
Turn-Off Time	t _{OFF}	V _{COM} = 3V, Figure 2	T _A = +25°C	57	75		ns
			T _A = T _{MIN} to T _{MAX}		100		
Break-Before-Make Time Delay (Note 3)	t _D	Figure 5	T _A = +25°C	2	10		ns
Charge Injection (Note 3)	V _{CTE}	C _L = 1.0nF, V _{GEN} = 0V, R _{GEN} = 0Ω, Figure 6	T _A = +25°C		5	10	pC
Off-Isolation (Note 6)	V _{ISO}	R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 3	T _A = +25°C		66		dBm
Crosstalk (Note 7)	V _{CT}	R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 8	T _A = +25°C		88		dBm
Off-Capacitance	C _{OFF}	f = 1MHz, Figure 3	T _A = +25°C		12		pF
COM Off-Capacitance	C _{COM(OFF)}	f = 1MHz, Figure 3	T _A = +25°C		12		pF
Channel On-Capacitance	C _{COM(ON)}	f = 1MHz, Figure 4	T _A = +25°C		39		pF
SUPPLY							
Power-Supply Range				±2.4		±8	V
Positive Supply Current	I ₊	All channels on or off, V+ = 5.5V, V- = -5.5V, V _{IN} = 0V or V+		-1.0	+0.06	+1.0	μA
Negative Supply Current	I ₋	All channels on or off, V+ = 5.5V, V- = -5.5V, V _{IN} = 0V or V+		-1.0	-0.01	+1.0	μA

Low-Voltage, Quad, SPDT, CMOS Analog Switch

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = 5V ±10%, V- = 0V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP. RANGE	MIN	TYP (Note 2)	MAX	UNITS	
SWITCH								
Analog Signal Range	VCOM, VNO, VNC	(Note 3)		0V		V+	V	
On-Resistance	RON	V+ = 5.0V, V- = 0V, VNC or VNO = 3.5V, ICOM = 1.0mA, VINH = 2.4V, VINL = 0.8V	TA = +25°C	C, E	25	65	Ω	
			TA = TMIN to TMAX	M		60		
On-Resistance Match Between Channels (Note 4)	ΔRON	VNC or VNO = 3V, ICOM = 1.0mA, V+ = 5V	TA = +25°C	C, E, M	0.5	2	Ω	
			TA = TMIN to TMAX	C, E, M		4		
On-Resistance Flatness (Note 4)	RFLAT(ON)	VNC or VNO = 3V, 2V, 1V; ICOM = 1.0mA; V+ = 5V; V- = 0V	TA = +25°C	C, E, M		6	Ω	
			TA = TMIN to TMAX	C, E, M		8		
NC or NO Off-Leakage Current (Note 8)	INC(OFF) or INO(OFF)	VCOM = 0V, VNC or VNO = 4.5V, V+ = 5.5V, V- = 0V	TA = +25°C	C, E	-0.2	-0.01	+0.2	nA
			TA = TMIN to TMAX	M	-0.1	-0.01	+0.1	
				C, E	-2.5		+2.5	
COM Leakage Current (Note 8)	ICOM(ON)	VCOM = 4.5V, VNC or VNO = 4.5V, V+ = 5.5V, V- = 0V	TA = +25°C	C, E	-0.4	-0.04	+0.4	nA
			TA = TMIN to TMAX	M	-0.2	-0.04	+0.2	
				C, E	-5.0		+5.0	
				M	-20		+20	
DIGITAL LOGIC INPUT								
Input Current with Input Voltage High	IINH	VIN = 2.4V, all others = 0.8V		-1.0	+0.005	+1.0	μA	
Input Current with Input Voltage Low	IINL	VIN = 0.8V, all others = 2.4V		-1.0	+0.005	+1.0	μA	

Low-Voltage, Quad, SPDT, CMOS Analog Switch

MAX394

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V- = 0V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC						
Turn-On Time (Note 3)	tON	VCOM = 3V, Figure 2	TA = +25°C	160	250	ns
			TA = TMIN to TMAX		300	
Turn-Off Time (Note 3)	tOFF	VCOM = 3V, Figure 2	TA = +25°C	60	125	ns
			TA = TMIN to TMAX		175	
Break-Before-Make Time Delay (Note 3)	tD		TA = +25°C	5	20	ns
Charge Injection (Note 3)	VCTE	CL = 1.0nF, VGEN = 0V, RGEN = 0Ω	TA = +25°C	3	5	pC
SUPPLY						
Power-Supply Range	V+		2.4		16	V
Positive Supply Current	I+	All channels on or off, VIN = 0V or V+, V+ = 5.5V, V- = 0V	-1.0	+0.01	+1.0	μA
Negative Supply Current	I-	All channels on or off, VIN = 0V or V+, V+ = 5.5V, V- = 0V	-1.0	-0.01	+1.0	μA

ELECTRICAL CHARACTERISTICS—Single +3.3V Supply

(V+ = 3.0V to 3.6V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP. RANGE	MIN	TYP (Note 2)	MAX	UNITS	
SWITCH								
Analog Signal Range	VCOM, VNO, VNC	(Note 3)		0		V+	V	
On-Resistance	RON	V+ = 3V, V- = 0V, VNC or VNO = 1.5V, ICOM = 1.0mA, VINH = 2.4V, VINL = 0.8V	TA = +25°C	C, E	75	185	Ω	
			TA = TMIN to TMAX	M		175		
NC or NO Off-Leakage Current (Note 8)	IN(OFF) or INO(OFF)	VCOM = 0V, VNC or VNO = 3V, V+ = 3.6V, V- = 0V	TA = +25°C	C, E	-0.2	-0.01	+0.2	nA
			TA = TMIN to TMAX	M	-0.1	-0.01	+0.1	
COM Leakage Current (Note 8)	ICOM(ON)	VCOM = 3V, VNC or VNO = 3V, V+ = 3.6V, V- = 0V	TA = +25°C	C, E	-0.4	-0.04	+0.4	nA
			TA = TMIN to TMAX	M	-0.2	-0.04	+0.2	
				C, E	-5.0		+5.0	
				M	-20.0		+20.0	

Low-Voltage, Quad, SPDT, CMOS Analog Switch

ELECTRICAL CHARACTERISTICS—Single +3.3V Supply (continued)

(V+ = 3.0V to 3.6V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT							
Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4V, all others = 0.8V		-1.0	+0.005	+1.0	μA
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8V, all others = 2.4V		-1.0	+0.005	+1.0	μA
DYNAMIC							
Turn-On Time (Note 3)	t _{ON}	V _{COM} = 1.5V, Figure 2	T _A = +25°C			400	ns
Turn-Off Time (Note 3)	t _{OFF}	V _{COM} = 1.5V, Figure 2	T _A = +25°C			150	ns
Break-Before-Make Delay (Note 3)	t _D	Figure 5	T _A = +25°C	5	20		ns
Charge Injection (Note 3)	V _{CTE}	C _L = 1.0nF, V _{GEN} = 0V, R _{GEN} = 0Ω, Figure 6	T _A = +25°C		1	5	pC
SUPPLY							
Power-Supply Range	V+			2.7		16	V
Positive Supply Current	I+	All channels on or off, V _{IN} = 0V or V+, V+ = 3.6V, V- = 0V		-1.0	+0.01	+1.0	μA
Negative Supply Current	I-	All channels on or off, V _{IN} = 0V or V+, V+ = 3.6V, V- = 0V		-1.0	-0.01	+1.0	μA

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = \Delta R_{ON}(\max) - \Delta R_{ON}(\min)$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 5: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temperature.

Note 6: See Figure 6. Off-isolation = $20\log_{10} V_{COM}/V_{NC}$ or V_{NO} , V_{COM} = output, V_{NC} or V_{NO} = input to off switch.

Note 7: Between any two switches. See Figure 3.

Note 8: Leakage testing at single supply is guaranteed by testing with dual supplies.

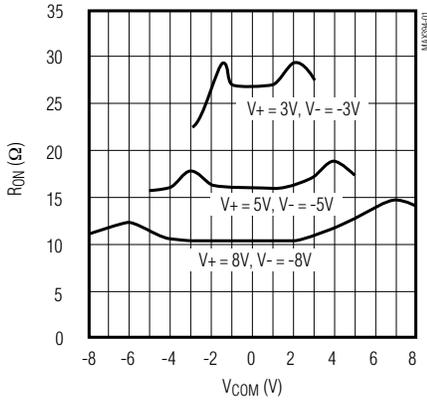
Low-Voltage, Quad, SPDT, CMOS Analog Switch

MAX394

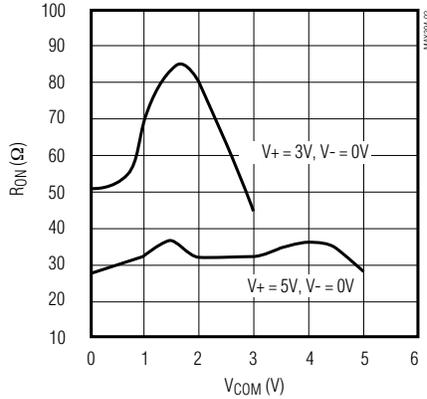
Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

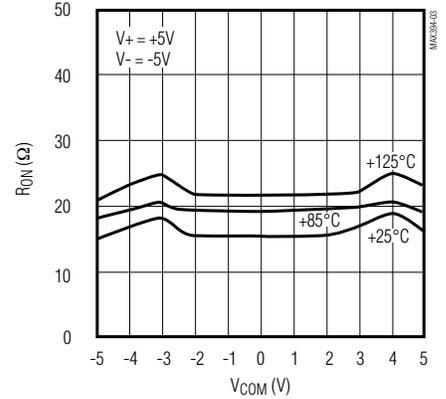
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



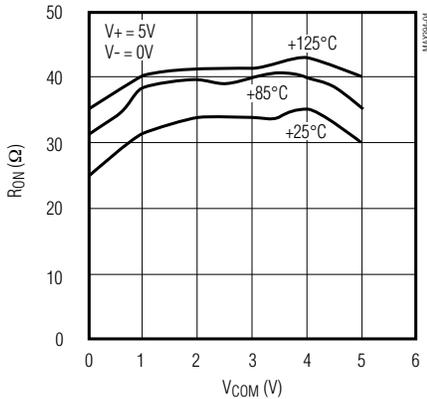
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



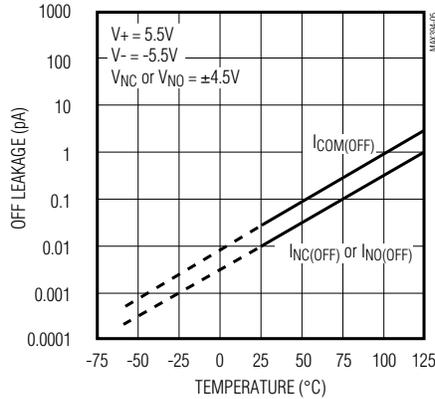
ON-RESISTANCE vs. V_{COM} OVER TEMPERATURE (DUAL SUPPLIES)



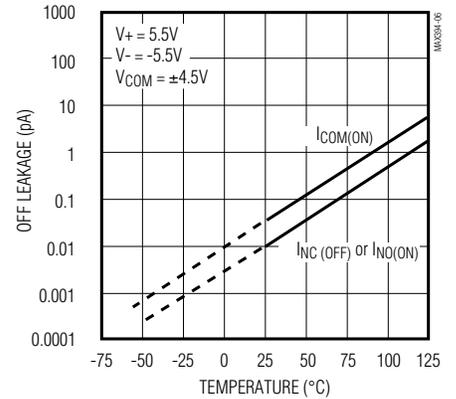
ON-RESISTANCE vs. V_{COM} OVER TEMPERATURE (SINGLE SUPPLY)



OFF-LEAKAGE CURRENT vs. TEMPERATURE



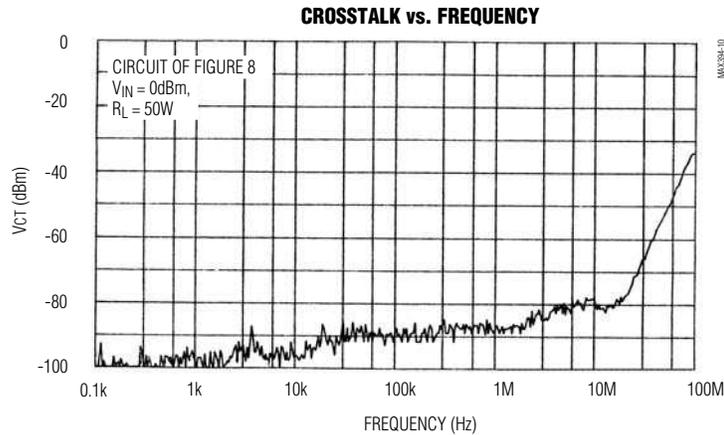
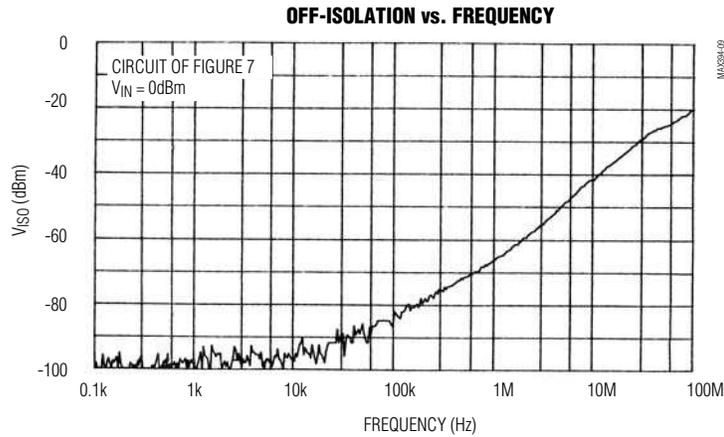
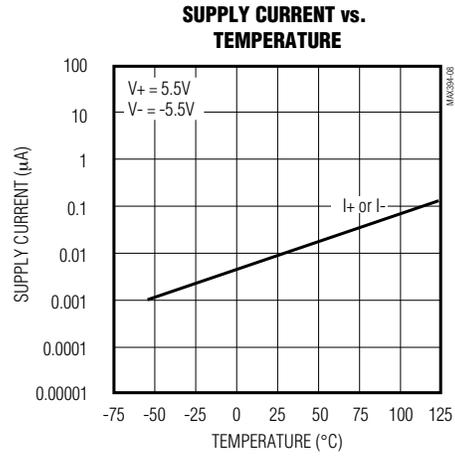
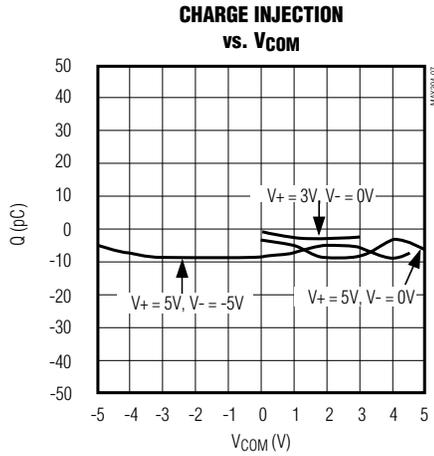
ON-LEAKAGE CURRENT vs. TEMPERATURE



Low-Voltage, Quad, SPDT, CMOS Analog Switch

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted).



Low-Voltage, Quad, SPDT, CMOS Analog Switch

MAX394

Pin Description

PIN	NAME	FUNCTION
1, 10, 11, 20	IN1-IN4	Logic-Level Inputs
2, 9, 12, 19	NO1-NO4	Normally Open Switches
3, 8, 13, 18	COM1-COM4	Common Switch Poles
4, 7, 14, 17	NC1-NC4	Normally Closed Switches
5	V-	Negative Power Supply
6	GND	Ground
15	N.C.	Not Internally Connected
16	V+	Positive Power Supply

Applications Information

Operation with Supply Voltages Other than $\pm 5V$

The MAX394 switch operates with $\pm 2.7V$ to $\pm 8V$ bipolar supplies and a $+2.7V$ to $+15V$ single supply. In either case, analog signals ranging from $V+$ to $V-$ can be switched. The *Typical Operating Characteristics* graphs show the typical on-resistance variation with analog signal and supply voltage. The usual on-resistance temperature coefficient is $0.5\%/^{\circ}C$ (typ).

Power-Supply Sequencing and Overvoltage Protection

Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the device. Proper power-supply sequencing is recommended for all CMOS devices. Always apply $V+$, followed by $V-$ (when using split supplies) before applying analog signals or logic inputs, especially if the analog or logic signals are not current-limited. If this sequencing is not possible and if the analog or logic inputs are not current-limited to less than

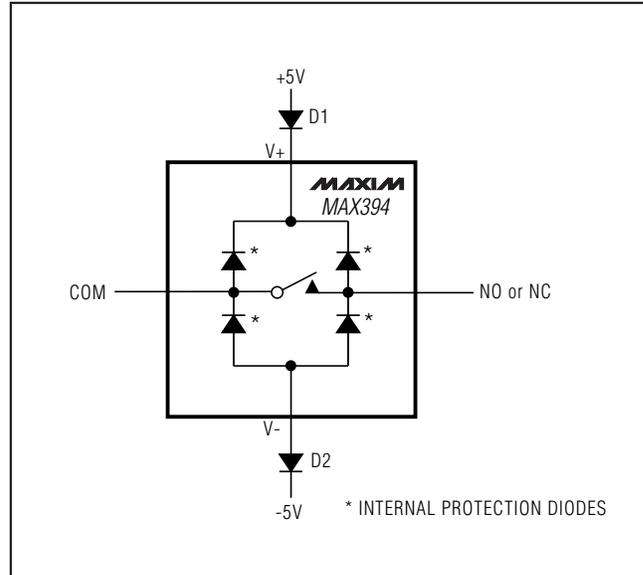


Figure 1. Overvoltage Protection Using Blocking Diodes

30mA, add a single diode (D1) for single-supply operation (Figure 1). If using dual supplies or if the analog signal can dip below ground in single-supply operation, add two small signal diodes (D1, D2), as shown in Figure 1. Adding protection diodes reduces the analog signal range to a diode drop above $V-$ for D2. Leakage is not affected by adding the diodes. On-resistance increases by a small amount at low supply voltages. Maximum supply voltage ($V-$ to $V+$) must not exceed $17V$.

Adding diodes D1 and D2 also protects against some overvoltage situations. With the circuit of Figure 1, if the supply voltage is below the absolute maximum rating and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result. For example, with $\pm 5V$ supplies, analog signals up to $\pm 8.5V$ will not damage the circuit of Figure 1. If only a single fault signal is present, the fault voltage can go to $+12V$ or $-12V$ without damage.

Low-Voltage, Quad, SPDT, CMOS Analog Switch

Test Circuits/Timing Diagrams

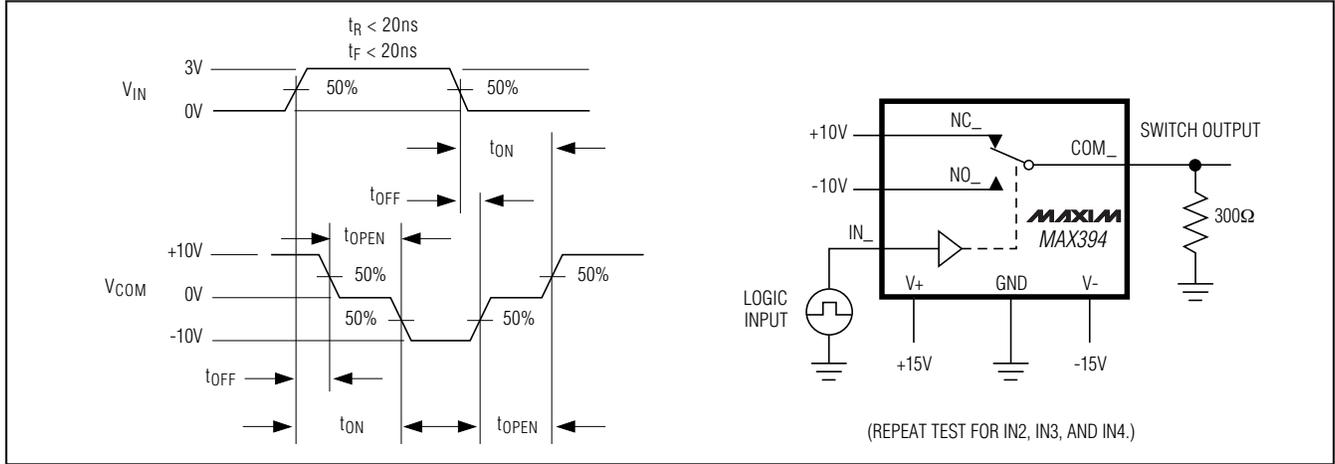


Figure 2. Switching-Time Test Circuit

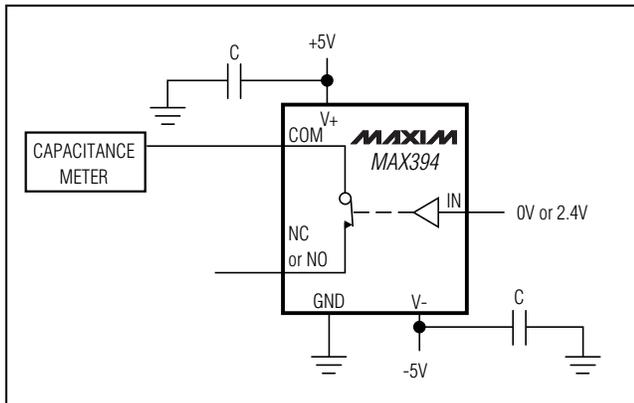


Figure 3. Channel Off-Capacitance

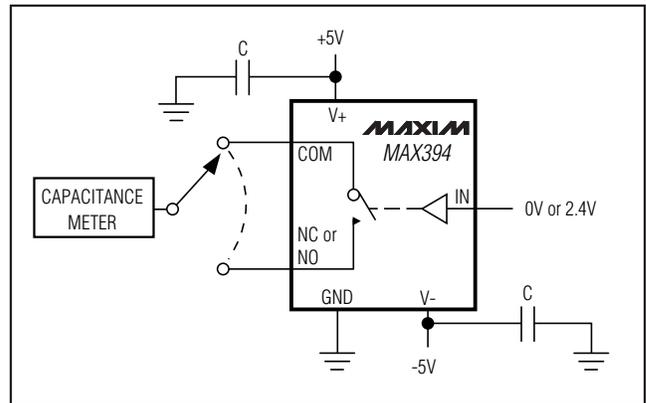


Figure 4. Channel On-Capacitance

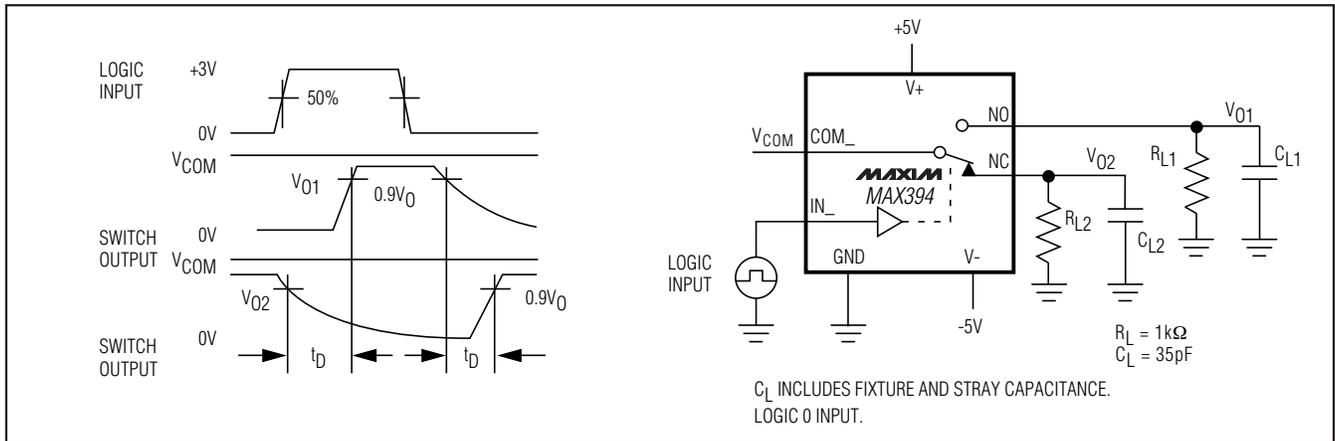


Figure 5. Break-Before-Make Delay

Low-Voltage, Quad, SPDT, CMOS Analog Switch

Test Circuits/Timing Diagrams (continued)

MAX394

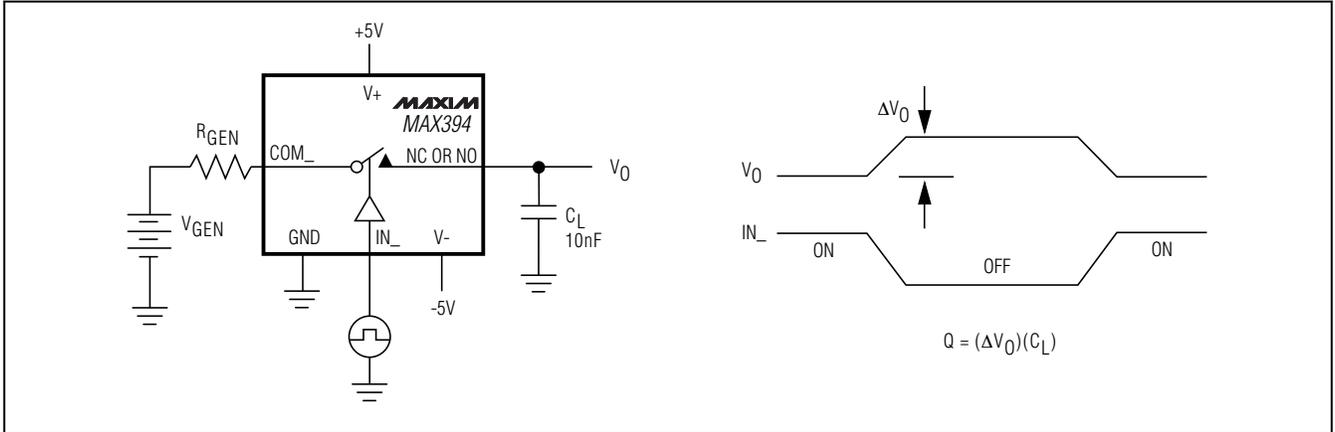


Figure 6. Charge Injection

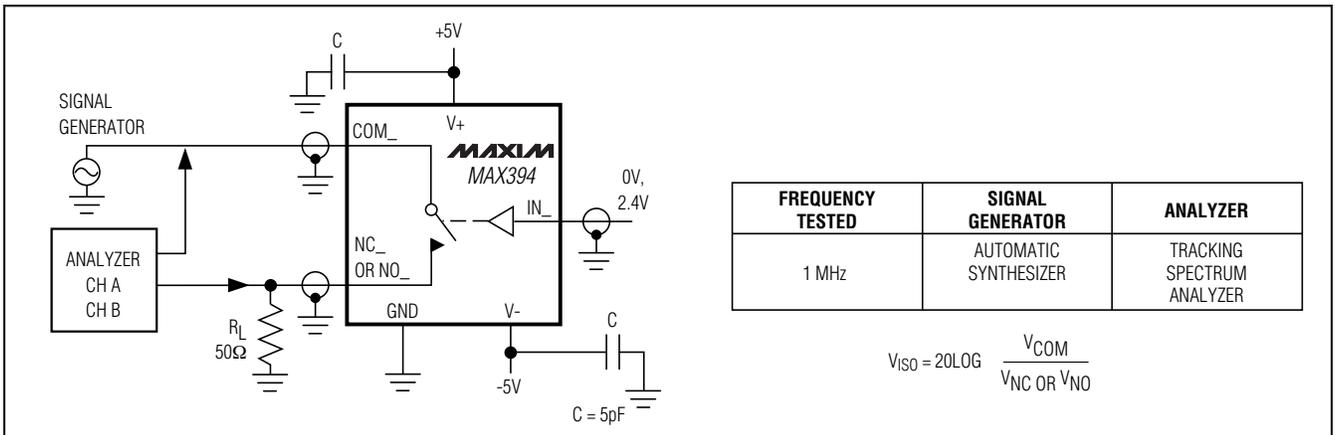


Figure 7. Off Isolation

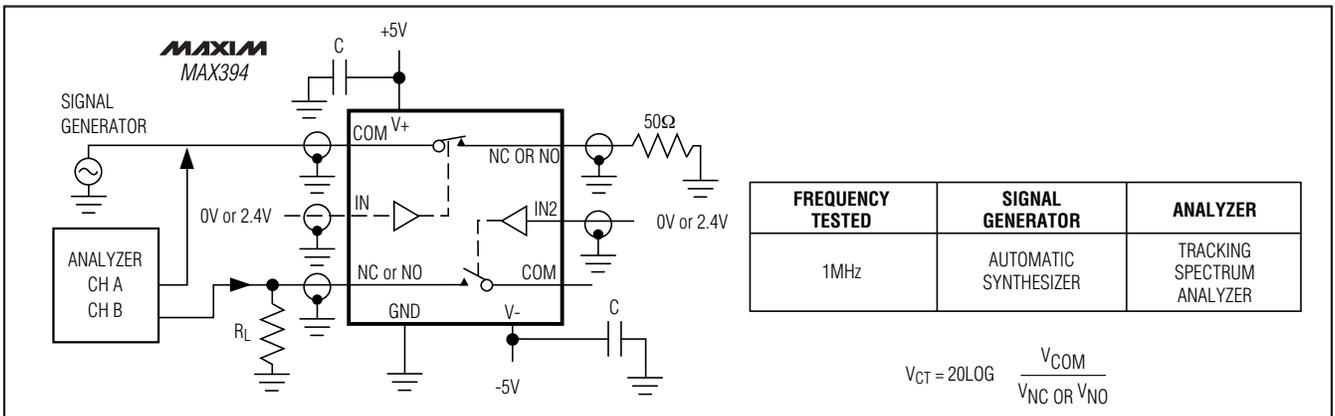
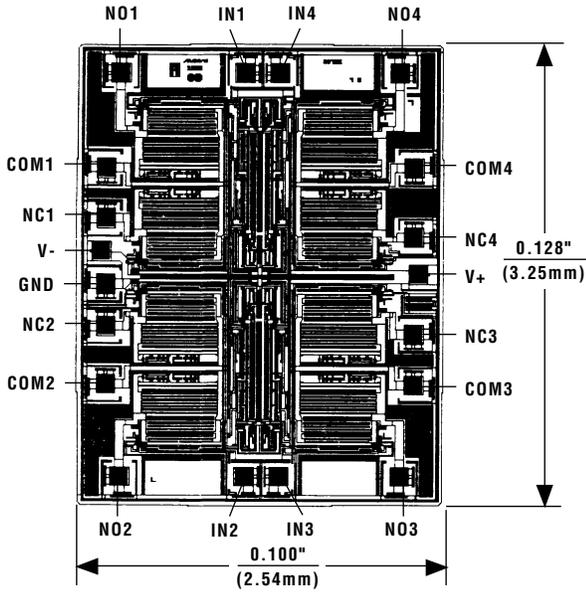


Figure 8. Crosstalk Test Circuit

Low-Voltage, Quad, SPDT, CMOS Analog Switch

Chip Topography



SUBSTRATE IS CONNECTED TO V+
 TRANSISTOR COUNT: 137

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 Plastic DIP	P20-4	21-0043
20 Wide SO	W26-1	21-0042
20 TSSOP	U20-2	21-0066
20 CERDIP	J20-2	21-0335

Low-Voltage, Quad, SPDT, CMOS Analog Switch

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	9/08	Added information for rugged plastic product	1

MAX394

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 _____ 13