19-4148; Rev 2; 8/10

EVALUATION KIT AVAILABLE

2.5/5.0/8.0Gbps PCIe Passive Switches

General Description

The MAX4889B/MAX4889C high-speed passive switches route PCI Express® (PCIe) data between two possible destinations in desktop or notebook PCs. The MAX4889B/MAX4889C are quad double-pole/double-throw (4 x DPDT) switches ideal for switching four half lanes of PCIe data between two destinations. The MAX4889B/MAX4889C feature a single digital control input (SEL) to switch signal paths.

The MAX4889C is intended for use in systems (e.g., SAS) where both the input and output are capacitively coupled, and provides a 10µA (typ) source current and a 60kΩ (typ) internal biasing resistor to GND at the _OUT_ terminals.

The MAX4889B/MAX4889C are fully specified to operate from a single +3.3V (typ) power supply. Both devices are available in an industry-standard 3.5mm x 9.0mm, 42-pin TQFN package. These devices operate over the -40°C to +85°C extended temperature range.

Applications

Desktop PCs

Notebook PCs

Servers

Video Graphics Cards—SLI®
(Scaled Link Interface) and CrossFire™

PCI Express is a registered service mark of PCI-SIG Corporation.

SLI is a registered trademark of NVIDIA Corporation.

CrossFire is a trademark of ATI Technologies, Inc.

Features

- ♦ **Single +3.3V Power-Supply Voltage**
- ♦ **Support PCIe Gen I, Gen II, and Gen III Data Rates**
- ♦ **Supports SAS I, SAS II, and SAS 6.0Gbps (MAX4889C)**
- ♦ **Superior Return Loss**
  Better than -10dB (typ) at 5.0GHz
- ♦ **Small 3.5mm x 9.0mm, 42-Pin TQFN Package**
- ♦ **Industry-Standard Pinouts**

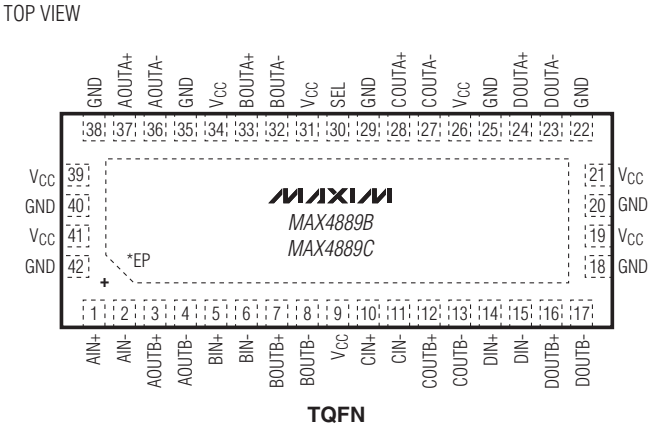
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4889BETO+	-40°C to +85°C	42 TQFN-EP*
MAX4889CETO+	-40°C to +85°C	42 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit appears at end of data sheet.

Pin Configuration



TQFN

*CONNECT EXPOSED PAD TO GROUND.

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
V_{CC} .....-0.3V to +4V
SEL, _IN_, _OUTA_, _OUTB_ (Note 1) .....-0.3V to (V_{CC} + 0.3V)
Continuous Current (AIN_ to AOUTA_/AOUTB_, BIN_ to BOUTA_/BOUTB_, CIN_ to COUTA_/COUTB_, DIN_ to DOUTA_/DOUTB_) .....±70mA
Peak Current (AIN_ to AOUTA_/AOUTB_, BIN_ to BOUTA_/BOUTB_, CIN_ to COUTA_/COUTB_, DIN_ to DOUTA_/DOUTB_)
(pulsed at 1ms, 10% duty cycle).....±70mA
Continuous Current (SEL).....±10mA
Peak Current (SEL)
(pulsed at 1ms, 10% duty cycle).....±10mA

Continuous Power Dissipation (T_A = +70°C) for multilayer board:
42-Pin TQFN (derate 35.7mW/°C above +70°C) 2857mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Package Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 2) .....28.0°C/W
Package Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2) .....2.0°C/W
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Signals on SEL, _IN_, _OUTA_, _OUTB_ exceeding V_{CC} or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE						
Analog Signal Range	_IN_, _OUTA_, _OUTB_		-0.3		V_{CC} - 1.8	V
On-Resistance	R_{ON}	V_{CC} = +3.0V, $I_{IN\_}$ = 15mA, $V_{OUTA\_}$, $V_{OUTB\_}$ = 0V, 1.2V		6.4	8.4	Ω
On-Resistance Match Between Pairs of Same Channel	ΔR_{ON}	V_{CC} = +3.0V, $I_{IN\_}$ = 15mA, $V_{OUTA\_}$, $V_{OUTB\_}$ = 0V (Notes 4, 5)		0.1	0.5	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = +3.0V, $I_{IN\_}$ = 15mA, $V_{OUTA\_}$, $V_{OUTB\_}$ = 0V (Notes 4, 5)		0.2		Ω
On-Resistance Flatness	$R_{FLAT (ON)}$	V_{CC} = +3.0V, $I_{IN\_}$ = 15mA, $V_{OUTA\_}$, $V_{OUTB\_}$ = 0V, 1.2V (Notes 5, 6)		0.3		Ω
OUTA or _OUTB_ Off-Leakage Current	$I_{OUTA\_ (OFF)}$, $I_{OUTB\_ (OFF)}$	V_{CC} = +3.6V, $V_{IN\_}$ = 0V, 1.2V, $V_{OUTA\_}$ or $V_{OUTB\_}$ = 1.2V, 0V (MAX4889B)	-1		+1	µA
_IN_ On-Leakage Current	$I_{IN\_ (ON)}$	V_{CC} = +3.6V, $V_{IN\_}$ = 0V, 1.2V, $V_{OUTA\_}$ or $V_{OUTB\_}$ = $V_{IN\_}$ or unconnected (MAX4889B)	-1		+1	µA
Output Short-Circuit Current		All other ports are unconnected (MAX4889C)	5		15	µA
Output Open-Circuit Voltage		All other ports are unconnected (MAX4889C)	0.2	0.6	0.9	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE						
SEL-to-Switch Turn-On Time	t_{ON_SEL}	Z_S = Z_L = 50Ω		80		ns
SEL-to-Switch Turn-Off Time	t_{OFF_SEL}	Z_S = Z_L = 50Ω, Figure 1		15		ns
Propagation Delay	t_{PD}	Z_S = Z_L = 50Ω, Figure 2		50		ps
Output Skew Between Pairs	t_{SKEW1}	Z_S = Z_L = 50Ω, Figure 2		50		ps
Output Skew Between Same Pair	t_{SKEW2}	Z_S = Z_L = 50Ω, Figure 2		10		ps
Differential Return Loss (Note 5)	S_{DD11}	0Hz < f ≤ 2.8GHz	-14			dB
		2.8GHz < f ≤ 5.0GHz	-8			
		f > 5.0GHz	-3			
Differential Insertion Loss (Note 5)	S_{DD21}	See Table 1				dB
Differential Crosstalk (Note 5)	S_{DDCTK}	0Hz < f ≤ 2.5GHz		-40		dB
		2.5GHz < f ≤ 5.0GHz		-30		
		f > 5.0GHz		-25		
Differential Off-Isolation (Note 5)	S_{DD21_OFF}	0Hz < f ≤ 2.5GHz		-15		dB
		2.5GHz < f ≤ 5.0GHz		-12		
		f > 5.0GHz		-12		
CONTROL INPUT (SEL)						
Input Logic High	V_{IH}		1.4			V
Input Logic Low	V_{IL}				0.6	V
Input Logic Hysteresis	V_{HYST}			130		mV
POWER SUPPLY						
Power-Supply Range	V_{CC}		3.0		3.6	V
V_{CC} Supply Current	I_{CC}	V_{SEL} = 0V or V_{CC}			1	mA

Note 3: All units are 100% production tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design and characterization and are not production tested.

Note 4: $\Delta R_{ON} = R_{ON\ (MAX)} - R_{ON\ (MIN)}$.

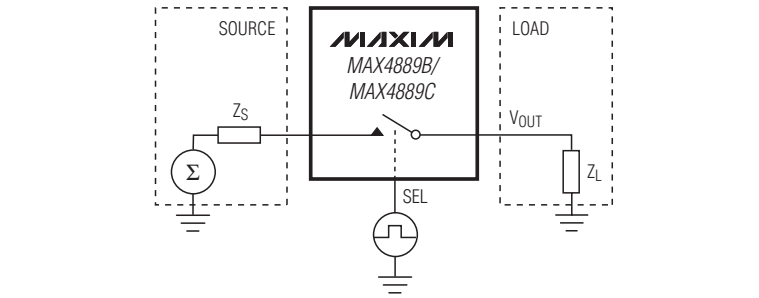
Note 5: Guaranteed by design, not production tested.

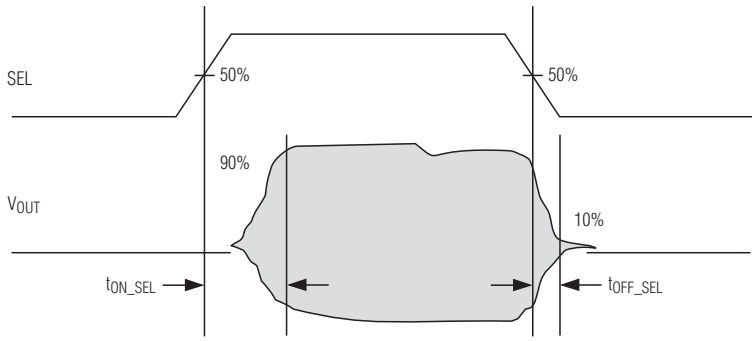
Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Table 1. Insertion Loss Mask

FREQUENCY RANGE (GHz)	MAXIMUM INSERTION LOSS (dB)
0–2.5	$\frac{14}{25} \times f_{GHz} + 0.6$
2.5–5	$\frac{6}{5} \times f_{GHz} - 1.0$
5 or greater	$\frac{8}{5} \times f_{GHz} - 3.0$

Test Circuits/Timing Diagrams





THE FREQUENCY OF THE SIGNAL SHOULD BE ABOVE THE HIGHPASS FILTER CORNER OF THE COUPLING CAPACITORS.

Figure 1. Switching Time

Test Circuits/Timing Diagrams (continued)

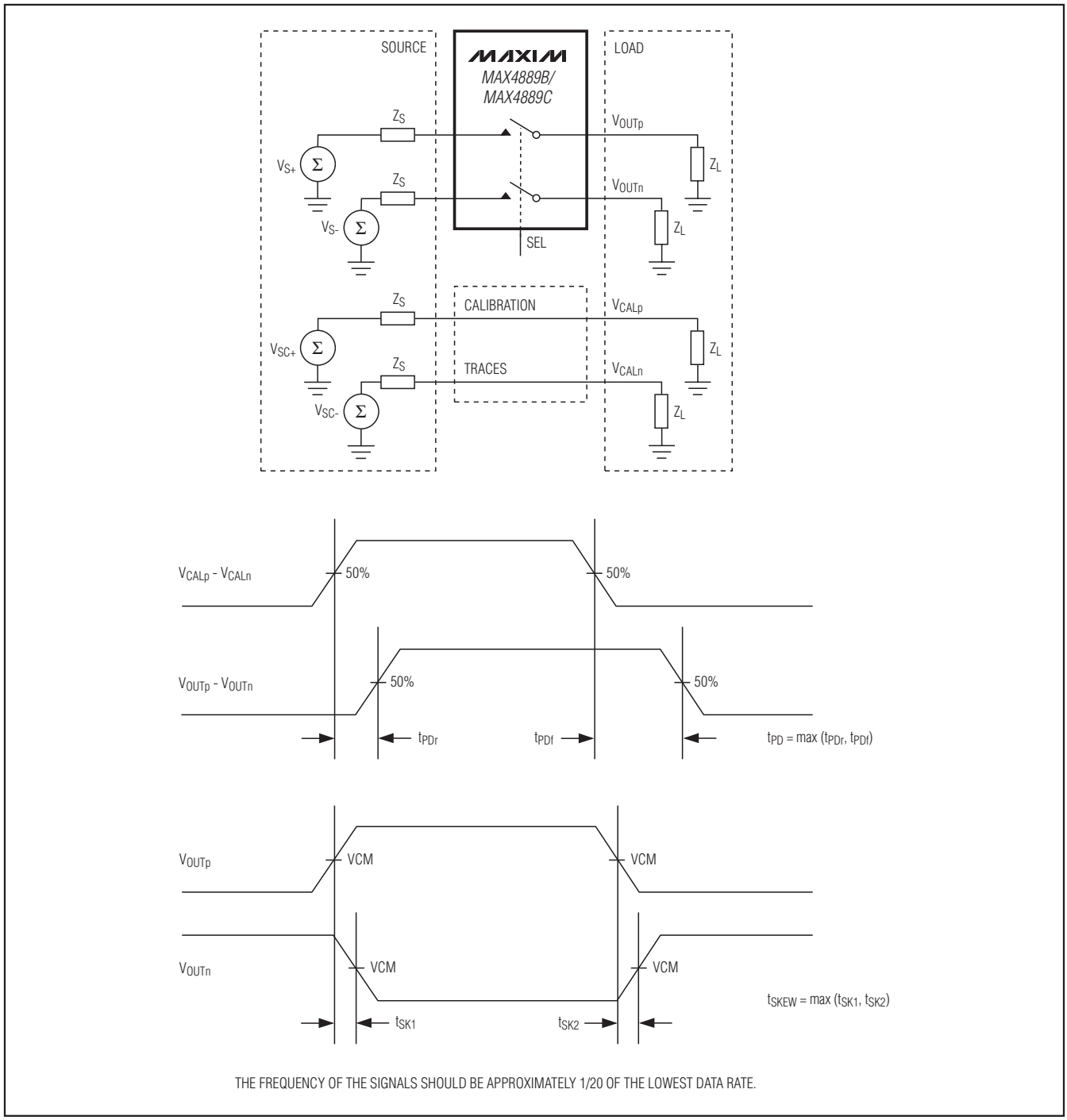


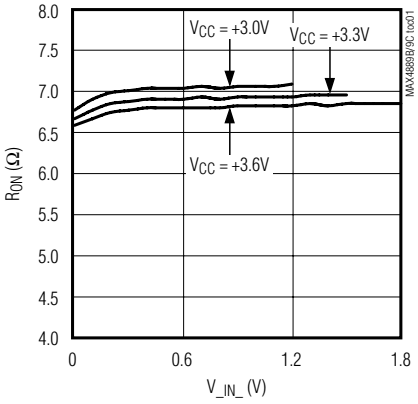
Figure 2. Propagation Delay and Output Skew

2.5/5.0/8.0Gbps PCIe Passive Switches

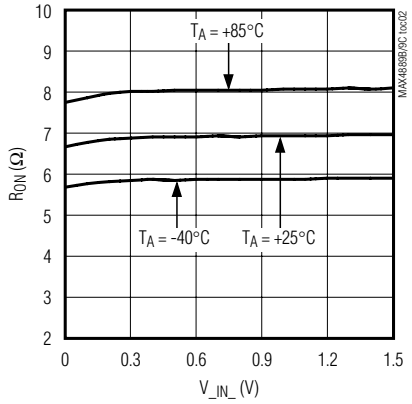
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

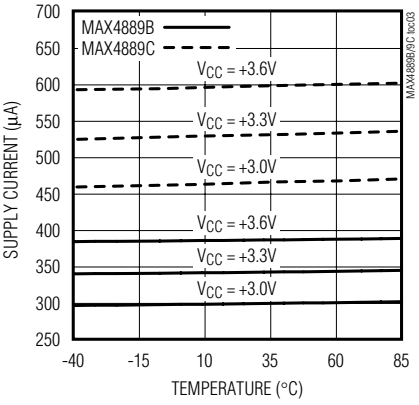
ON-RESISTANCE vs. V_IN_



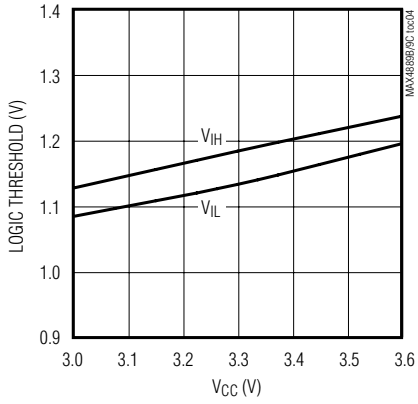
ON-RESISTANCE vs. V_IN_



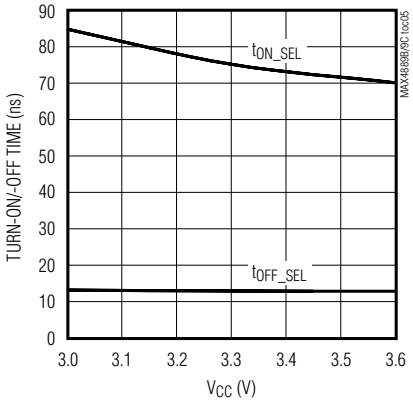
SUPPLY CURRENT vs. TEMPERATURE



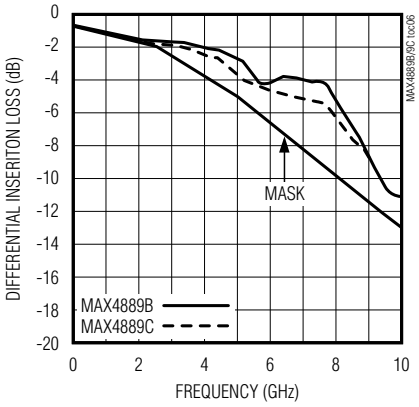
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



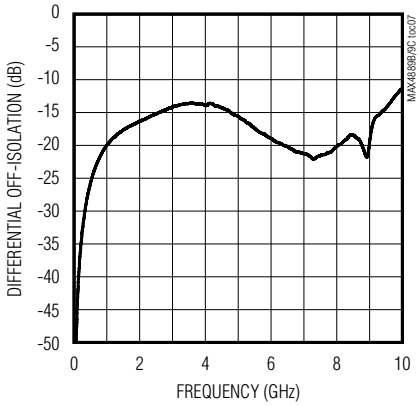
TURN-ON/-OFF TIME vs. SUPPLY VOLTAGE



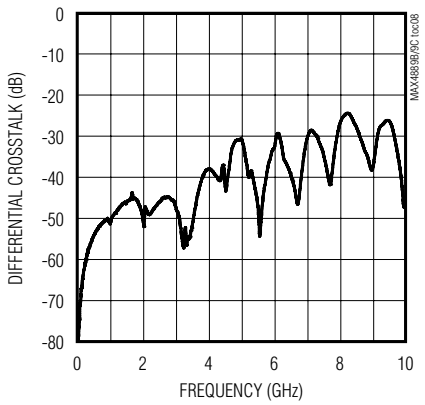
DIFFERENTIAL INSERTION LOSS vs. FREQUENCY



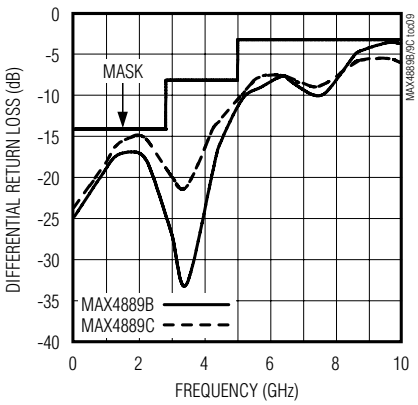
DIFFERENTIAL OFF-ISOLATION vs. FREQUENCY



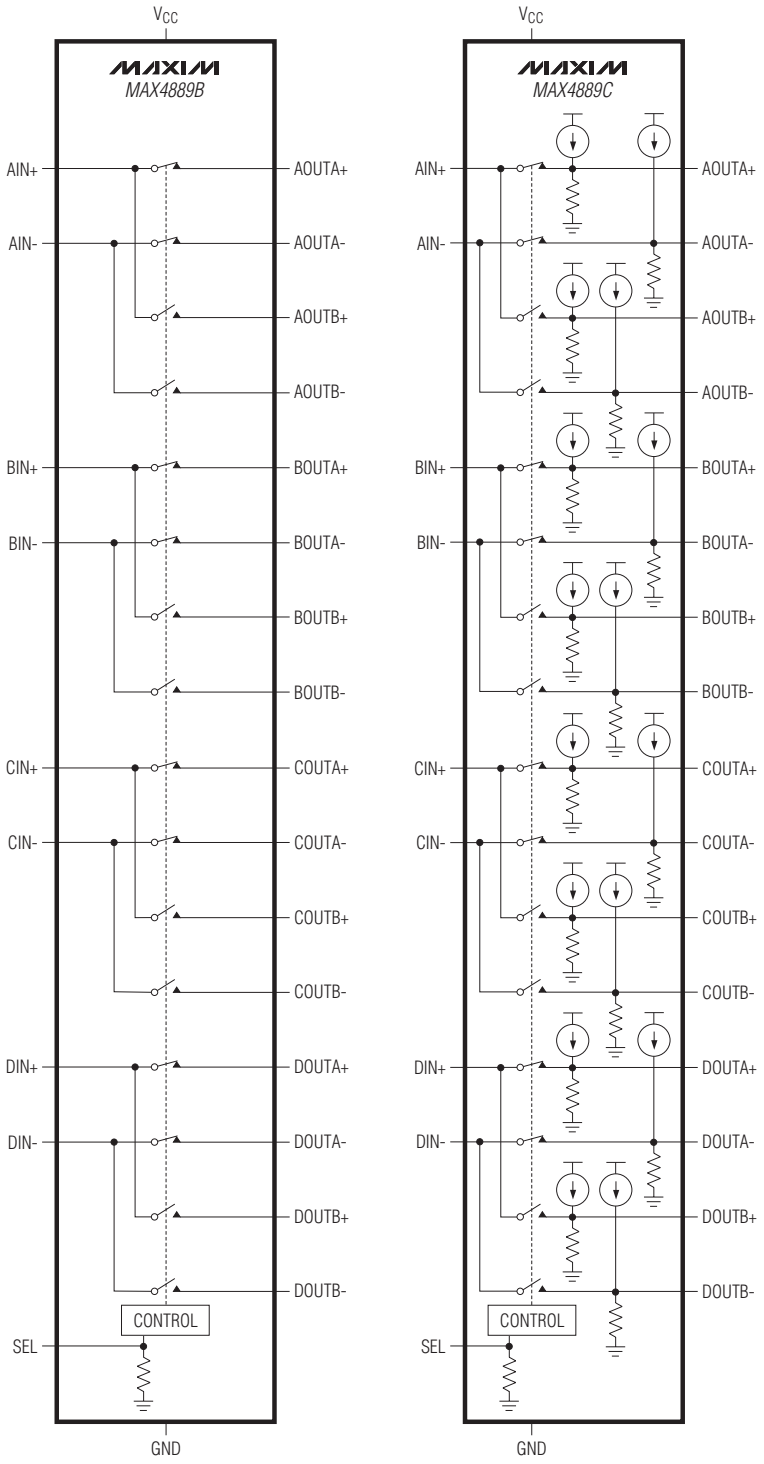
DIFFERENTIAL CROSSTALK vs. FREQUENCY



DIFFERENTIAL RETURN LOSS vs. FREQUENCY



Functional Diagram/Truth Table



SEL	_IN_ TO _OUTA_	_IN_ TO _OUTB_
0 (DEFAULT)	ON	OFF
1	OFF	ON

Pin Description

PIN	NAME	FUNCTION
MAX4889B/ MAX4889C		
1	AIN+	Analog Switch 1. Common Positive Terminal.
2	AIN-	Analog Switch 1. Common Negative Terminal.
3	AOUTB+	Analog Switch 1. Normally Open Positive Terminal.
4	AOUTB-	Analog Switch 1. Normally Open Negative Terminal.
5	BIN+	Analog Switch 2. Common Positive Terminal.
6	BIN-	Analog Switch 2. Common Negative Terminal.
7	BOUTB+	Analog Switch 2. Normally Open Positive Terminal.
8	BOUTB-	Analog Switch 2. Normally Open Negative Terminal.
9, 19, 21, 26, 31, 34, 39, 41	V_{CC}	Positive Supply Voltage Input. Connect V_{CC} to a 3.0V to 3.6V supply voltage. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor placed as close as possible to the device. See the *Board Layout* section.
10	CIN+	Analog Switch 3. Common Positive Terminal.
11	CIN-	Analog Switch 3. Common Negative Terminal.
12	COUTB+	Analog Switch 3. Normally Open Positive Terminal.
13	COUTB-	Analog Switch 3. Normally Open Negative Terminal.
14	DIN+	Analog Switch 4. Common Positive Terminal.
15	DIN-	Analog Switch 4. Common Negative Terminal.
16	DOUTB+	Analog Switch 4. Normally Open Positive Terminal.
17	DOUTB-	Analog Switch 4. Normally Open Negative Terminal.
18, 20, 22, 25, 29, 35, 38, 40, 42	GND	Ground
23	DOUTA-	Analog Switch 4. Normally Closed Negative Terminal.
24	DOUTA+	Analog Switch 4. Normally Closed Positive Terminal.
27	COUTA-	Analog Switch 3. Normally Closed Negative Terminal.
28	COUTA+	Analog Switch 3. Normally Closed Positive Terminal.
30	SEL	Control Signal Input. SEL has a 70kΩ (typ) pulldown resistor to GND.
32	BOUTA -	Analog Switch 2. Normally Closed Negative Terminal.
33	BOUTA+	Analog Switch 2. Normally Closed Positive Terminal.
36	AOUTA-	Analog Switch 1. Normally Closed Negative Terminal.
37	AOUTA+	Analog Switch 1. Normally Closed Positive Terminal.
—	EP	Exposed Pad. Connect EP to GND.

Detailed Description

The MAX4889B high-speed passive switch routes PCI Express (PCIe) data or other high-speed signals with amplitude of ≤ 1.2V_{P-P} differential, and common-mode voltage close to 0V between two possible destinations. The MAX4889B is ideal for routing PCIe signals to change system configuration. For example, in a graphics application, four MAX4889B devices create two sets of eight lanes from a single 16-lane bus. The MAX4889C feature a 10µA (typ) source current and a 60kΩ (typ) internal biasing resistor to GND at the _OUT_ terminals. The MAX4889C is ideal for dual capacitively coupled applications such as SAS and SATA. The MAX4889B/MAX4889C feature a single digital control input (SEL) to switch signal paths. SEL has a 70kΩ (typ) pulldown resistor to GND.

The MAX4889B/MAX4889C are fully specified to operate from a single 3.0V to 3.6V power supply.

Digital Control Input (SEL)

The MAX4889B/MAX4889C provide a single digital control input (SEL) to select the signal path between the _IN_ and _OUT_ channels. The truth tables for the MAX4889B/MAX4889C are illustrated in the *Functional Diagram/Truth Table*. SEL has a 70kΩ (typ) pulldown resistor to GND.

Analog Signal Levels

The MAX4889B/MAX4889C accept standard PCIe signals to a maximum of (V_{CC} - 1.8V). Signals on the _IN+ channels are routed to either the _OUTA+ or _OUTB+ channels. Signals on the _IN- channels are routed to either the _OUTA- or _OUTB- channels. The MAX4889B/MAX4889C are bidirectional switches, allowing _IN_ and _OUT_ to be used as either inputs or outputs.

Applications Information

PCIe Switching

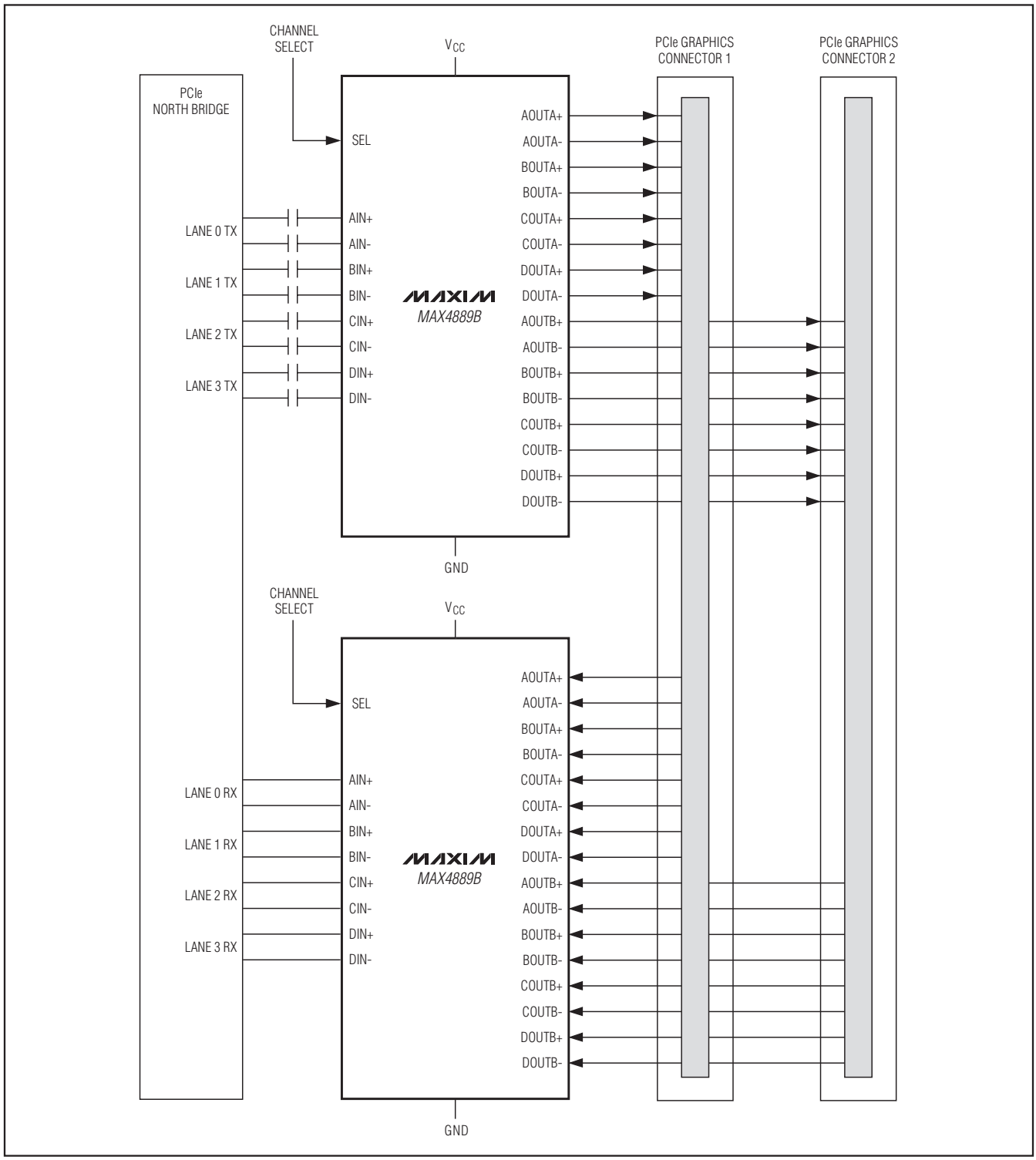
The MAX4889B/MAX4889C primary applications are aimed at reallocating PCIe lanes (see the *Typical Operating Circuit: Video Graphics Cards*). For example, in graphics applications, several manufacturers have found that it is possible to improve performance by a factor of nearly two by splitting a single 16-lane PCIe bus into two 8-lane buses. Two of the more prominent examples are SLI (Scaled Link Interface) and CrossFire. Four MAX4889Bs permit a computer motherboard to operate properly with a single 16-lane graphics card, which can later be upgraded to dual cards.

Board Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep controlled-impedance PCB traces as short as possible or follow impedance layouts per the PCIe specification. Ensure that power-supply bypass capacitors are placed as close as possible to the device. Multiple bypass capacitors are recommended. Connect all grounds and the exposed pad to large ground planes.

2.5/5.0/8.0Gbps PCIe Passive Switches

Typical Operating Circuit: Video Graphics Cards



Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
42 TQFN	T423590M+1	21-0181	90-0079

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	8/10	Added 8.0Gbps PCIe passive switch to the title; added Gen III to the data rates in the *Features* section; changed the return loss in the *Features* section to -10dB (typ) at 5.0GHz	All