MAX44260/MAX44261
1.8V 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps

General Description

The MAX44260/MAX44261 offer a unique combination of high speed, precision, low noise, and low-voltage operation making them ideally suited for a large number of signal processing functions such as filtering and amplification of signals in portable and industrial equipment.

The amplifiers feature an input offset of less than 50µV and a high-gain bandwidth product of 15MHz while maintaining a low 1.8V supply rail. The devices' rail-to-rail input/outputs and low noise guarantee maximum dynamic range in demanding applications such as 12- to 14-bit SAR ADC drivers. Unlike traditional rail-to-rail input structures, input crossover distortion is absent due to an optimized input stage with an ultra-quiet charge pump.

The MAX44260 includes a fast-power-on shutdown mode for further power savings. The MAX44261 offers a unique on-demand calibration pin where the user can invoke self-trimming of the input offset voltage.

The family of parts operates from a supply range of 1.8V to 5.5V over the -40°C to +125°C temperature range and can operate down to 1.7V over the 0°C to +70°C temperature range. The MAX44260/MAX44261 are available in small, 6-pin SC70 packages. The MAX44260 is also available in a 1mm x 1.5mm thin µDFN (ultra-thin LGA) package.

***Ordering Information* appears at end of data sheet.**

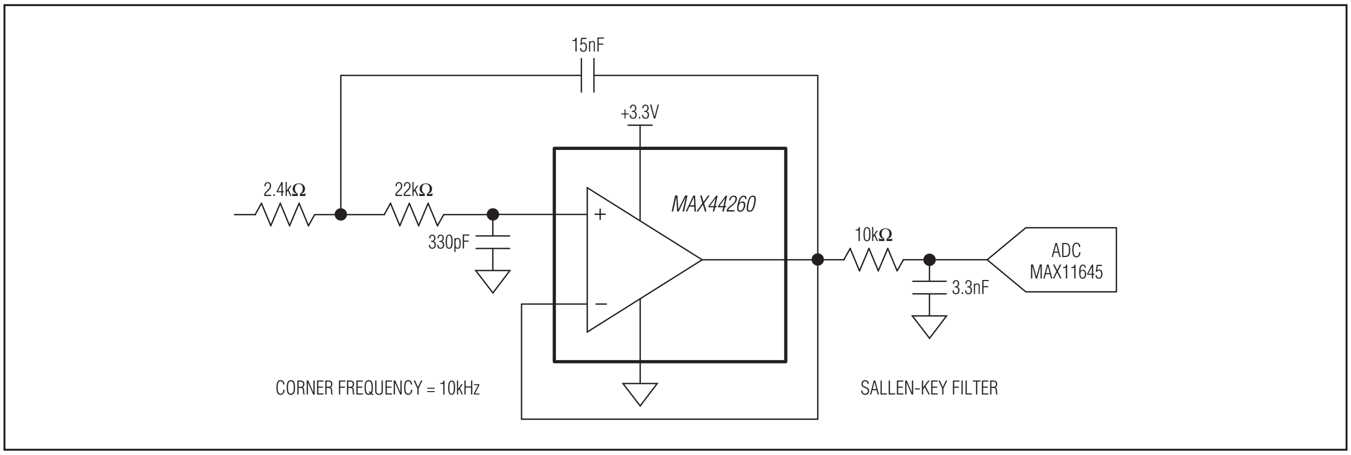
Features

- **Low 1.8V Supply Rail Over the -40°C to +125°C Range**
  1.7V Supply Rail Over the 0°C to +70°C Range
- **15MHz Unity-Gain Bandwidth**
- **Low 12.7nV/√Hz Input Voltage-Noise Density**
- **Low 1.2fA/√Hz Input Current-Noise Density**
- **Low 50µV (max) V_{OS} at +25°C**
- **On-Demand V_{OS} Self-Calibration (MAX44261)**
- **500fA Low Input Bias Current**
- **750µA Quiescent Current per Amplifier**
- **< 1µA Supply Current in Shutdown**
- **Small, 2mm x 2mm SC70 and 1mm x 1.5mm Thin µDFN (MAX44260) Packages**
- **Low 110dB Total Harmonic Distortion**

Applications

Notebooks
3G/4G Handsets
Portable Media Players
Portable Medical Instruments
Battery-Operated Devices
Analog-to-Digital Converter Buffers
Transimpedance Amplifiers
General-Purpose Signal Processing

Typical Application Circuit



For related parts and recommended products to use with this part, refer to: ***www.maxim-ic.com/MAX44260.related***

ABSOLUTE MAXIMUM RATINGS

IN+, IN-, OUT ....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
V_{DD} to V_{SS}...-0.3V to +6V
$\overline{SHDN}$, $\overline{CAL}$ ....-0.3V to +6V
Output to Short-Circuit Ground Duration 10s
Continuous Input Current into Any Pin........................... ±20mA
Continuous Power Dissipation (T_A = +70°C)
SC70 (derate 3.1mW/°C above +70°C)......................245mW
6-Pin Thin µDFN (Ultra-Thin LGA)
(derate 2.1mW/°C above +70°C)............................110.2mW
Operating Temperature Range........................ -40°C to +125°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

SC70
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 326.5°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....115°C/W
Thin µDFN (Ultra-Thin LGA)
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 470°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, $V_{\overline{CAL}}$ = $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Input Voltage Range	V_{IN+} V_{IN-}	Guaranteed by CMRR test	-0.1		V_{DD} + 0.1	V
Input Offset Voltage	V_{OS}	T_A = +25°C		10	50	µV
		T_A = -40°C to +125°C after calibration			100	
		T_A = -40°C to +125°C			500	
Input Offset Voltage Drift	V_{OS} - TC			0.8	5	µV/°C
Input Bias Current (Note 3)	I_B	T_A = +25°C		0.01	0.5	pA
		T_A = -40°C to +85°C			10	
		T_A = -40°C to +125°C			100	
Input Capacitance	C_{IN}			0.4		pF
Common-Mode Rejection Ratio	CMRR	V_{CM} = -0.1V to (V_{DD} + 0.1V)	75	90		dB
Open-Loop Gain	A_{OL}	0.4V ≤ V_{OUT} ≤ V_{DD} - 0.4V, R_{OUT} = 10kΩ	100	115		dB
		0.4V ≤ V_{OUT} ≤ V_{DD} - 0.4V, R_{OUT} = 600Ω	91	100		
		0.4V ≤ V_{OUT} ≤ V_{DD} - 0.4V, R_{OUT} = 32Ω		80		
Output Short-Circuit Current	I_{SC}	To V_{DD} or V_{SS}		50		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, $V_{\overline{CAL}}$ = $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

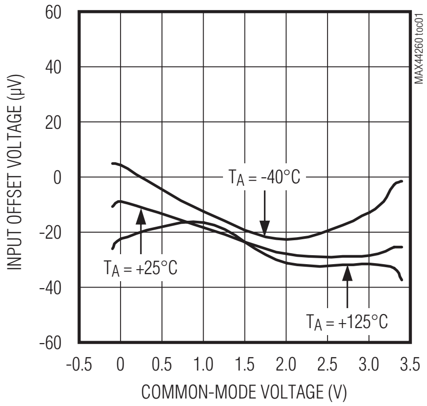
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing	V_{OL} - V_{SS}	R_{OUT} = 10kΩ			20	mV
		R_{OUT} = 600Ω			50	
		R_{OUT} = 32Ω		400	700	
	V_{DD} - V_{OH}	R_{OUT} = 10kΩ			10	
		R_{OUT} = 600Ω			40	
		R_{OUT} = 32Ω		400	800	
AC CHARACTERISTICS						
Input Voltage-Noise Density	e_n	f = 10kHz		12.7		nV/√Hz
Input Current-Noise Density	i_n	f = 10kHz		1.2		fA/√Hz
Gain-Bandwidth Product	GBWP			15		MHz
Slew Rate	SR			7		V/µs
Settling Time		V_{OUT} = $2V_{P-P}$, V_{DD} = 3.3V, A_V = 1V/V, C_L = 30pF (load), settle to 0.01%		1.7		µs
Capacitive Loading	C_{LOAD}	No sustained oscillation		300		pF
Total Harmonic Distortion	THD	f = 10kHz, V_O = $2V_{P-P}$, A_V = 1, R_{OUT} = 10kΩ		-110		dB
Output Transient Recovery Time		ΔV_{OUT} = 0.2V, V_{DD} = 3.3V, A_V = 1V/V; R_S = 20Ω, C_L = 1nF (load)		1		µs
POWER-SUPPLY CHARACTERISTICS						
Power-Supply Range	V_{DD}	Guaranteed by PSRR	1.8		5.5	V
		T_A = 0°C to +70°C	1.7		5.5	
Power-Supply Rejection Ratio	PSRR	V_{CM} = V_{DD}/2	82	95		dB
Quiescent Current	I_{DD}			750	1200	µA
Shutdown Supply Current	$I_{\overline{SHDN}}$	MAX44260/MAX44261 only			1	µA
Shutdown Input Low	V_{IL}				0.5	V
Shutdown Input High	V_{IH}		1.3			V
Output Leakage Current in Shutdown	$I_{\overline{SHDN}}$			100		pA
Shutdown Input Bias Current	I_{IL}/I_{IH}	MAX44260			1	µA
		MAX44261			0.1	
Shutdown Turn-On Time	$t_{\overline{SHDN}}$	T_A = +25°C (Note 3)		14.4	18.9	µs
		T_A = -40°C to +125°C (Note 3)			26.7	
Turn-On Time	t_{ON}	T_A = +25°C (Note 3)		9.7	15.2	ms
		T_A = -40°C to +125°C (Note 3)			18.4	

Note 2: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 3: Guaranteed by design.

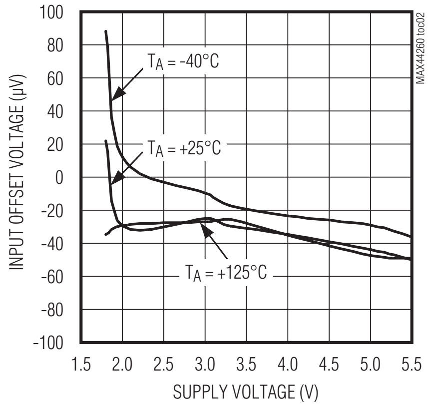
Typical Operating Characteristics

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, $V_{\overline{CAL}}$ = $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted. All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.)

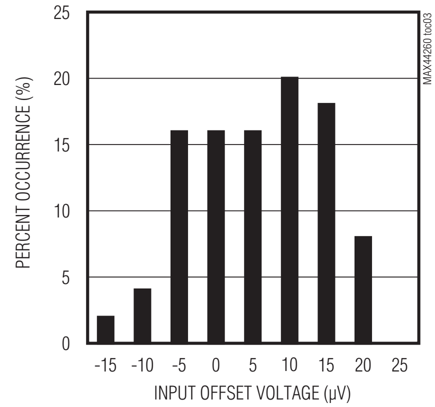
INPUT OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



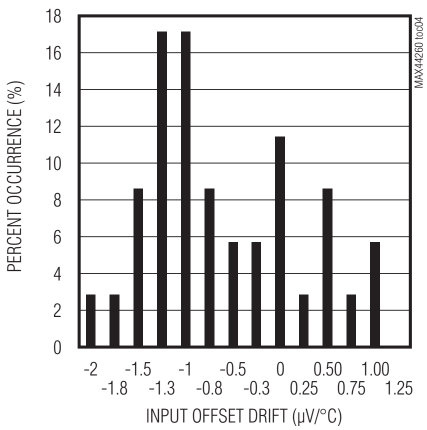
INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



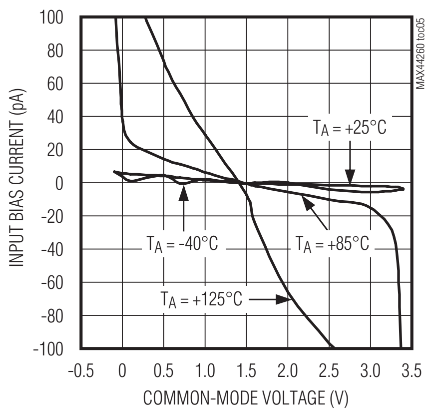
INPUT V_{OS} HISTOGRAM



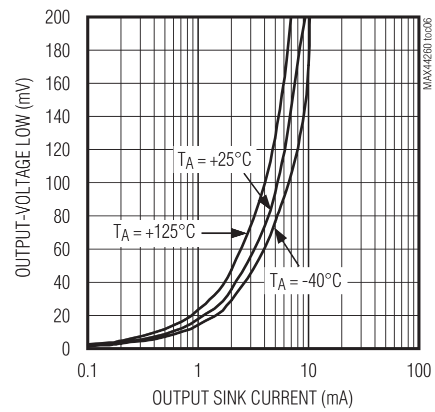
INPUT OFFSET DRIFT HISTOGRAM



INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



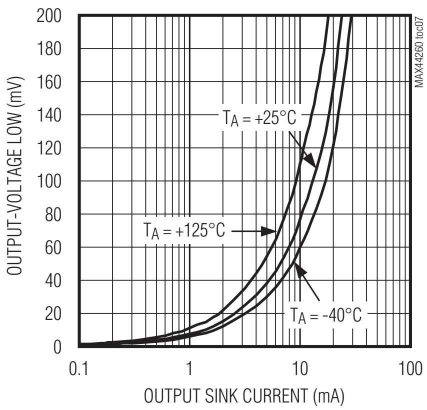
OUTPUT-VOLTAGE LOW vs. OUTPUT SINK CURRENT (V_{OL} - V_{EE}, V_{CC} = 1.8V)



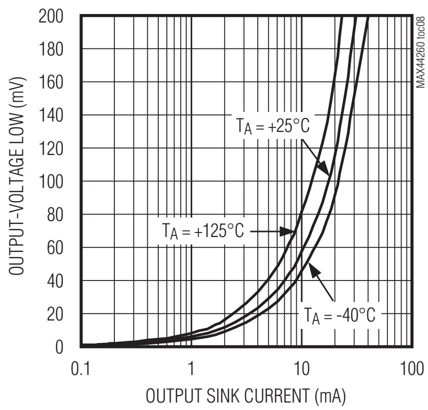
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, $V_{\overline{CAL}}$ = $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted. All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.)

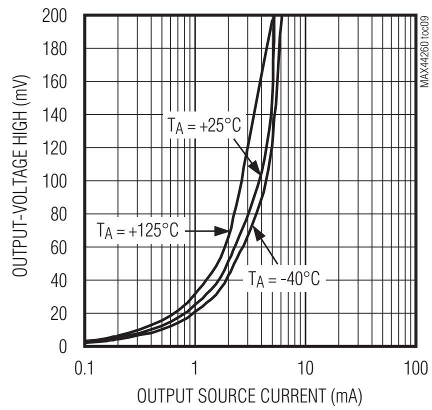
OUTPUT-VOLTAGE LOW vs. OUTPUT SINK CURRENT (V_{OL} - V_{EE}, V_{CC} = 3.3V)



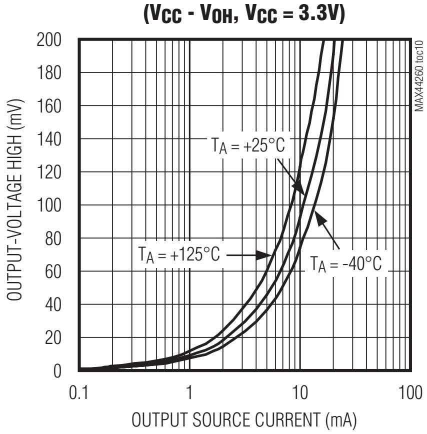
OUTPUT-VOLTAGE LOW vs. OUTPUT SINK CURRENT (V_{OL} - V_{EE}, V_{CC} = 5V)



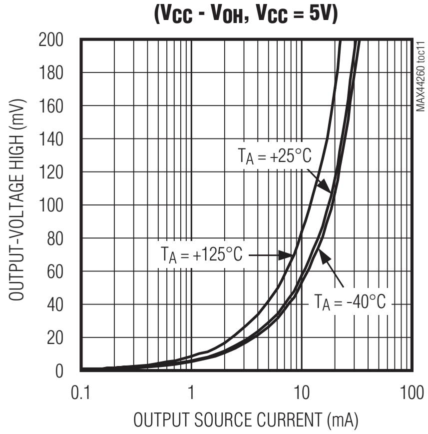
OUTPUT-VOLTAGE HIGH vs. OUTPUT SOURCE CURRENT (V_{CC} - V_{OH}, V_{CC} = 1.8V)



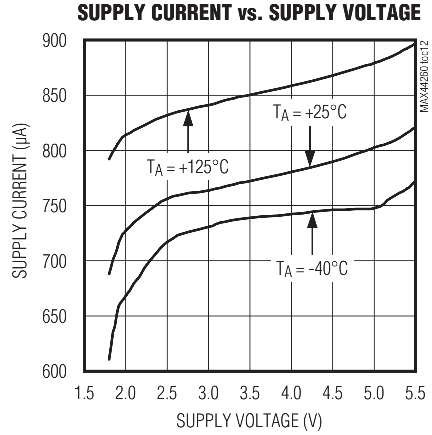
OUTPUT-VOLTAGE HIGH vs. OUTPUT SOURCE CURRENT (V_{CC} - V_{OH}, V_{CC} = 3.3V)



OUTPUT-VOLTAGE HIGH vs. OUTPUT SOURCE CURRENT (V_{CC} - V_{OH}, V_{CC} = 5V)



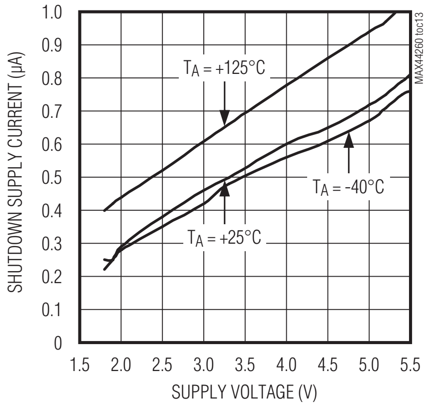
SUPPLY CURRENT vs. SUPPLY VOLTAGE



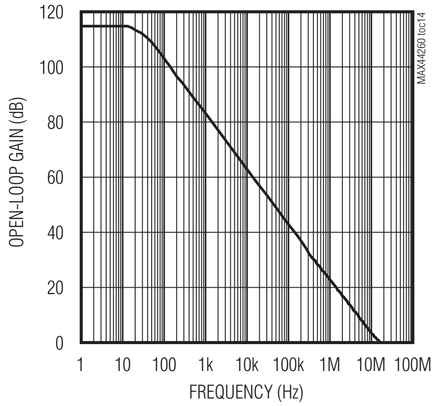
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, $V_{\overline{CAL}}$ = $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted. All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.)

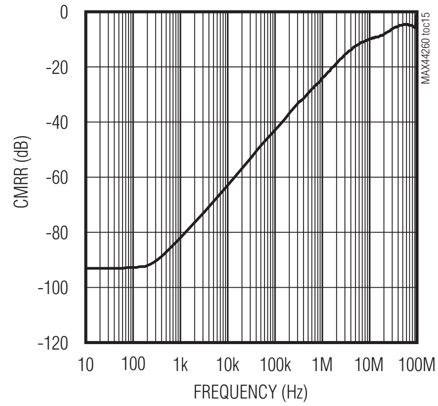
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE ($V_{\overline{SHDN}}$ = V_{EE})



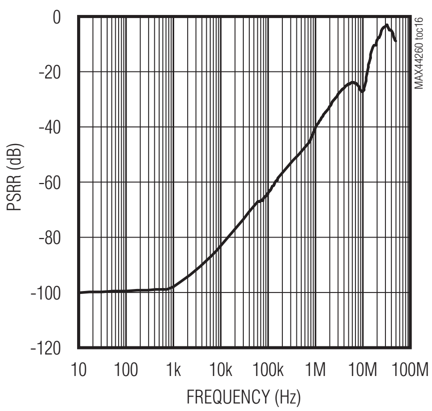
OPEN-LOOP GAIN vs. FREQUENCY



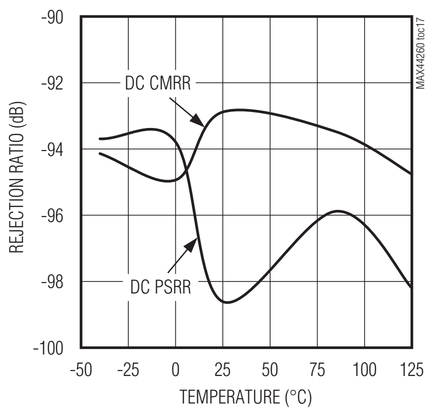
COMMON-MODE REJECTION RATIO vs. FREQUENCY



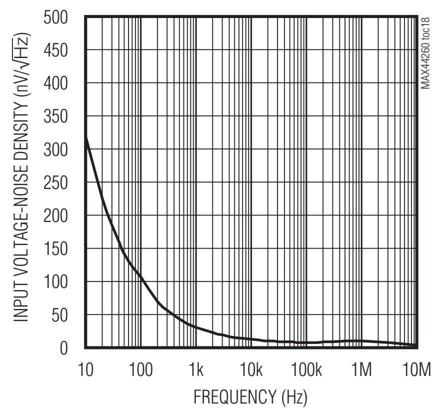
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



DC CMRR AND PSRR vs. TEMPERATURE



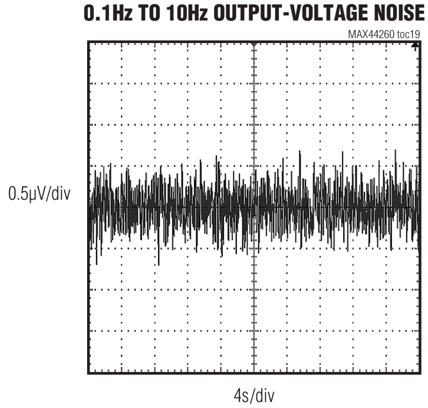
INPUT VOLTAGE-NOISE DENSITY vs. FREQUENCY



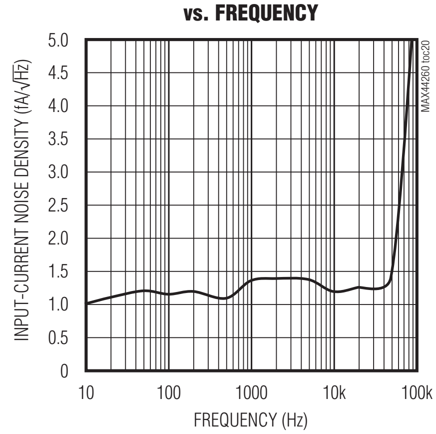
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, $V_{\overline{CAL}}$ = $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted. All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.)

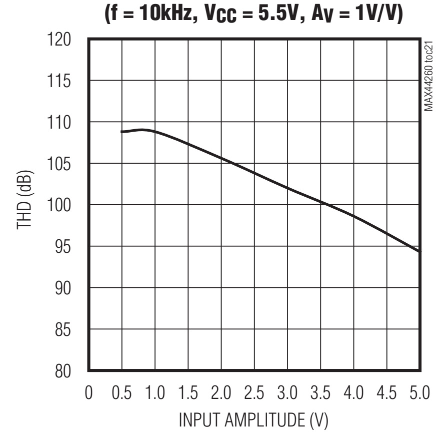
0.1Hz TO 10Hz OUTPUT-VOLTAGE NOISE



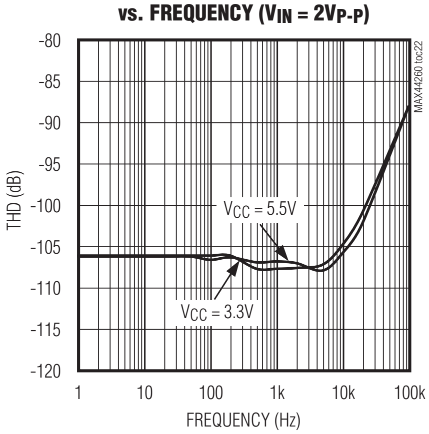
INPUT CURRENT-NOISE DENSITY vs. FREQUENCY



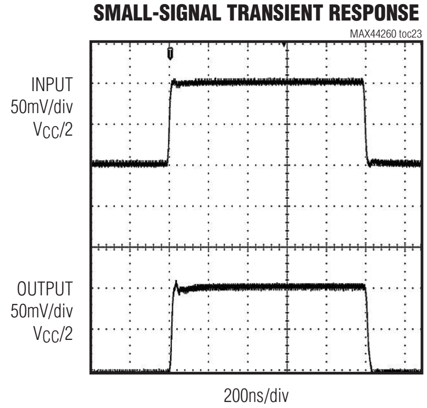
TOTAL HARMONIC DISTORTION vs. INPUT AMPLITUDE (f = 10kHz, V_{CC} = 5.5V, A_V = 1V/V)



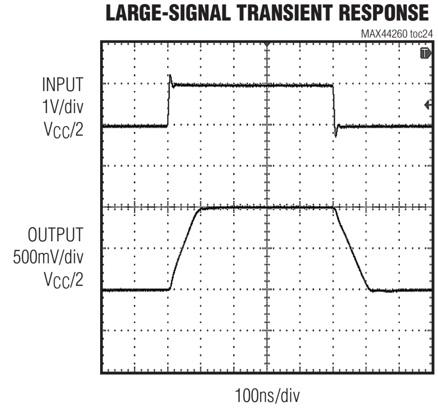
TOTAL HARMONIC DISTORTION vs. FREQUENCY (V_{IN} = $2V_{P-P}$)



SMALL-SIGNAL TRANSIENT RESPONSE

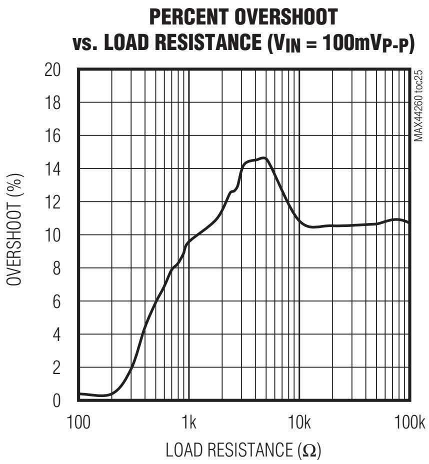


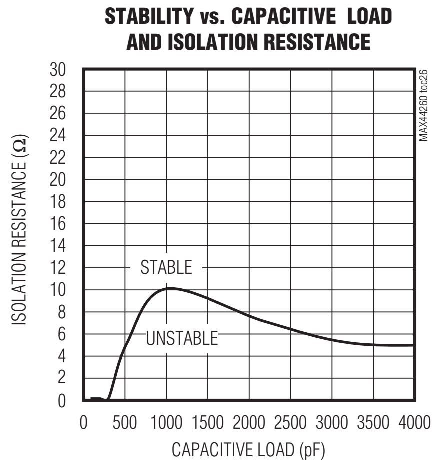
LARGE-SIGNAL TRANSIENT RESPONSE

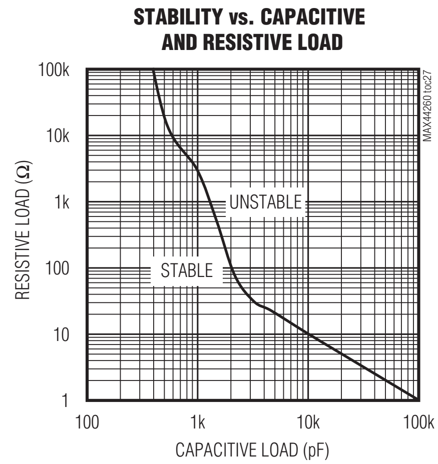


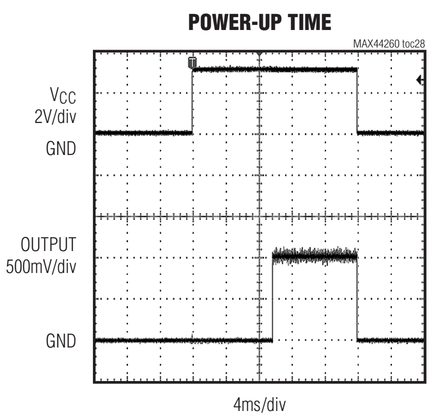
Typical Operating Characteristics (continued)

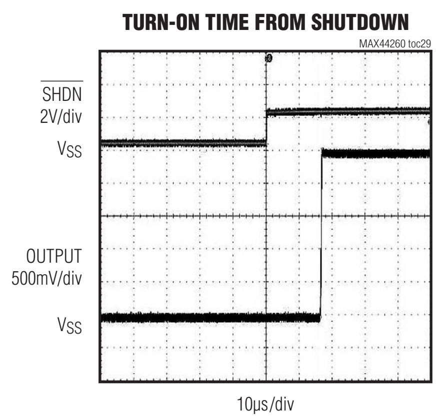
(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = $V_{DD}/2$, R_L = 10kΩ to $V_{DD}/2$, $V_{\overline{CAL}}$ = $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted. All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.)



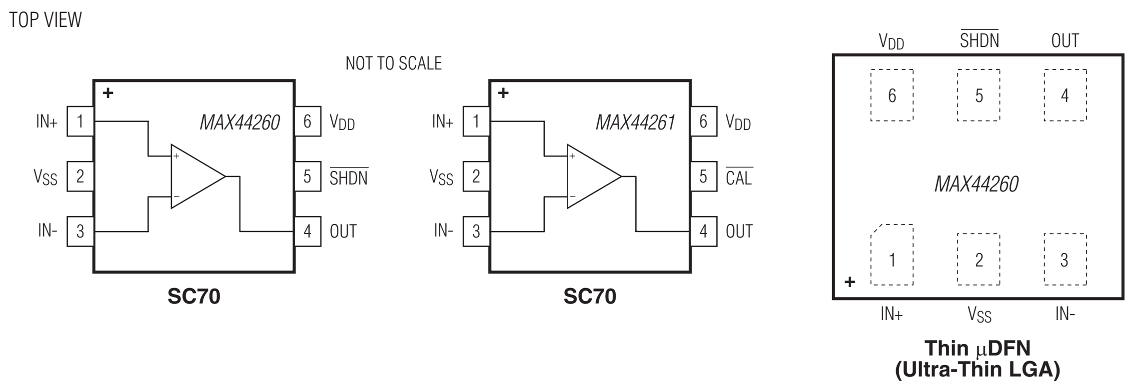








Pin Configurations



Pin Description

PIN		NAME	FUNCTION
MAX44260	MAX44261		
1	1	IN+	Positive Input
2	2	V_{SS}	Negative Power Supply. Bypass with a 0.1µF capacitor to ground.
3	3	IN-	Negative Input
4	4	OUT	Output
—	5	$\overline{CAL}$	Active-Low Calibrate Input
5	—	$\overline{SHDN}$	Active-Low Shutdown
6	6	V_{DD}	Positive Power Supply. Bypass with a 0.1µF capacitor to ground.

Detailed Description

The MAX44260/MAX44261 are high-speed low-power op amps ideal for signal processing applications due to the device's high precision and low-noise CMOS inputs. The devices self-calibrate on power-up to eliminate effects of temperature and power-supply variation.

The MAX44260 also features a low-power shutdown mode that greatly reduces quiescent current while the device is not operational and recovers in 30µs.

The MAX44261 features a user-selectable self-calibration input that shuts down the device and allows it to be recalibrated at any time. The calibration routine takes 10ms.

Crossover Distortion

These op amps feature a low-noise integrated charge pump that creates an internal voltage rail 1V above V_{DD}, which is used to power the input differential pair of PMOS transistors as shown in Figure 1. Such a unique architecture eliminates crossover distortion common in traditional CMOS input architecture (Figure 2), especially when used in a noninverting configuration, such as for Sallen-Key filters.

The charge pump's operating frequency lies well above the unity-gain frequency of the amplifier. Thanks to its high-frequency operation and ultra-quiet circuitry, the charge pump generates little noise, does not require external components, and is entirely transparent to the user.

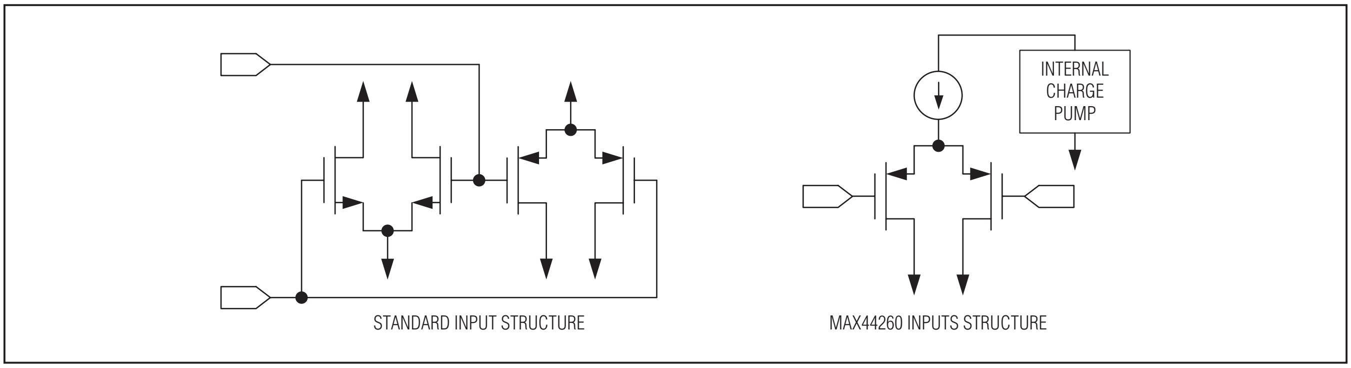


Figure 1. Comparing the Input Structure of the MAX44260 to Standard Op-Amp Inputs

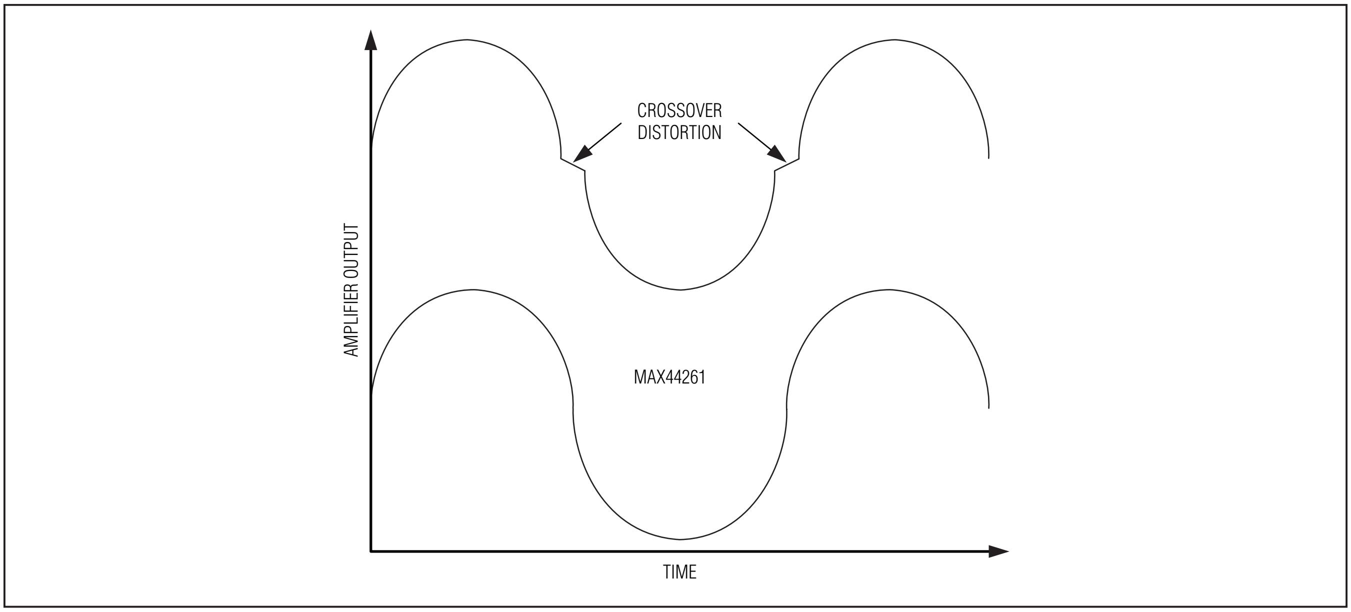


Figure 2. Crossover Distortion of Typical Amplifiers

Applications Information

Power-Up Autotrim

The ICs feature an automatic trim that self-calibrates the V_{OS} of these devices to less than 50μV of input offset voltage on power-up. This self-calibration feature allows the device to eliminate input offset voltage effects due to power supply and operating temperature variation simply by cycling its power. The autotrim sequence takes approximately 10ms to complete and is triggered by an internal power-on-reset (POR) circuitry. During this time, the inputs and outputs are put into high impedance and left unconnected. The MAX44261 can also be forced into a self-calibration cycle by pulling the $\overline{CAL}$ input low for 1μs. This input also puts the part into shutdown mode.

Shutdown Operation

The MAX44260 features an active-low shutdown mode that puts both inputs and outputs into high impedance and substantially lowers the quiescent current to less than 1μA. Putting the output into high impedance allows multiple outputs to be multiplexed onto a single output line without the additional external buffers. The device does not self-calibrate when exiting shutdown mode and retains its power-up trim settings. Figure 3 shows that the device also recovers from shutdown in under 30μs.

The MAX44261 features a recalibrate input that acts the same as the shutdown mode of the MAX44260. However, when the input is pulled low, the device goes through a self-calibration sequence again (Figure 3).

The shutdown logic levels of the devices are independent of supply, allowing the shutdown feature of the device to operate off of a 1.8V or 3.3V microcontroller, regardless of supply voltage.

Rail-to-Rail Input/Output

The input voltage range of the ICs extends 100mV above V_{DD} and below V_{SS}. The wide input common-mode voltage range allows the op amp to be used as a buffer and as a differential amplifier in a wide-variety of signal processing applications. Output voltage high/low is designed to be only 50mV above V_{SS} and below V_{DD} allowing maximum dynamic range in single-supply applications. The high output current and capacitance drive capability of the devices make them ideal as an ADC driver and a line driver.

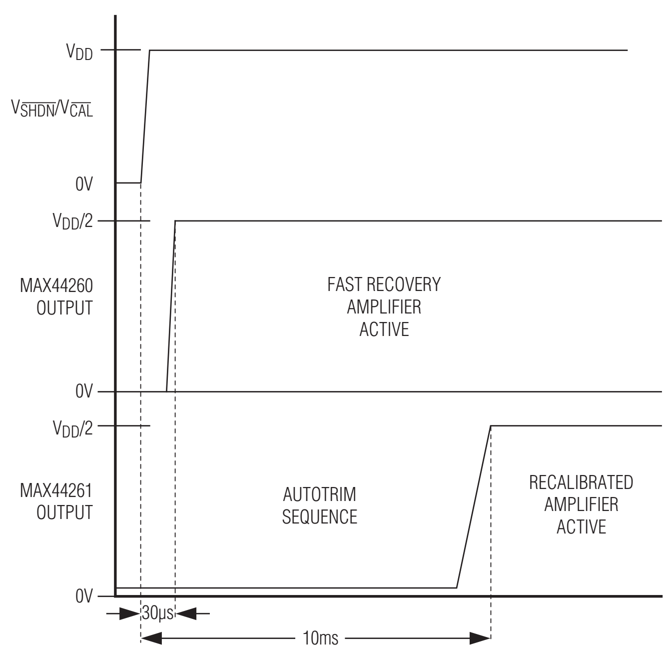


Figure 3. $\overline{CAL}$ vs. $\overline{SHDN}$ Input Operation

Input Bias Current

The ICs feature a high-impedance CMOS input stage and a specialized ESD structure that allows low-input bias current operation at low-input, common-mode voltages. Low-input bias current is useful when interfacing with high-ohmic sensors. It is also beneficial for designing transimpedance amplifiers for photodiode sensors. This makes these devices ideal for ground-referenced medical and industrial sensor applications.

Active Filters

The MAX44260/MAX44261 are ideal for a wide variety of active filter circuits that make use of their wide bandwidth, rail-to-rail input/output stages and high-impedance CMOS inputs. The *Typical Application Circuit* shows an example Sallen-Key active filter circuit with a corner frequency of 10kHz. At low frequencies, the amplifier behaves like a simple low-distortion noninverting buffer, while its high bandwidth gives excellent stopband attenuation above its corner frequency. See the *Typical Application Circuit*.

Driver for Interfacing with the MAX11645 ADC

The ICs' tiny size and low noise makes them a good fit for driving 12- to 16-bit resolution ADCs in space-constrained applications. The *Typical Application Circuit* shows the MAX44260 amplifier output connected to a lowpass filter driving the MAX11645 ADC. The MAX11645 is part of a family of 3V and 5V, 12-bit and 10-bit, 2-channel ADCs.

The MAX11645 offers sample rates up to 94ksps and measures two single-ended inputs or one differential input. These ADCs dissipate 670μA at the maximum sampling rate, but just 6μA at 1ksps and 0.5μA in shutdown. Offered in the ultra-tiny, 1.9mm x 2.2mm WLP and μMAX-8 packages, the MAX11645 ADCs are an ideal fit to pair with the MAX44260/MAX44261 amplifiers in portable applications.

Where higher resolution is required, refer to the MAX1069 (14-bit) and MAX1169 (16-bit) ADC families.

Chip Information

PROCESS: BiCMOS

Ordering Information

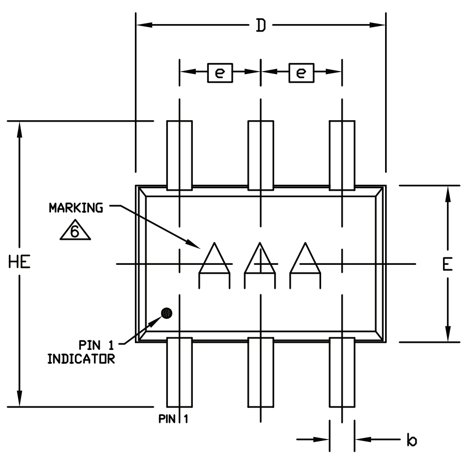
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX44260AXT+	-40°C to +125°C	6 SC70	+AEB
MAX44260AYT+	-40°C to +125°C	6 Thin μDFN (Ultra-Thin LGA)	+AY
MAX44261AXT+	-40°C to +125°C	6 SC70	+AEC

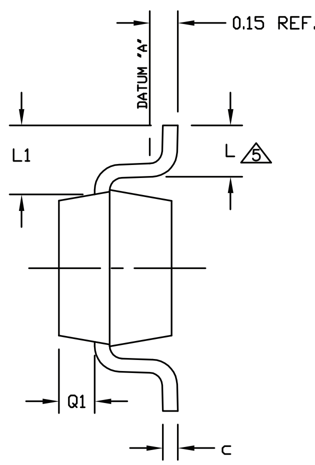
+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

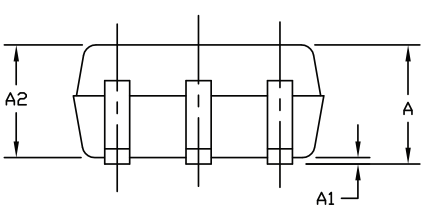
PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 SC70	X6SN+1	21-0077	90-0189
6 Thin µDFN (Ultra-Thin LGA)	Y61A1+1	21-0190	90-0233





COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.85	2.00	2.15
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	2.00	2.20	2.35
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODES	X6SN-1		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM 'A' AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
8. ALL DIMENSIONS COMPLY TO JEDEC MO-203.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

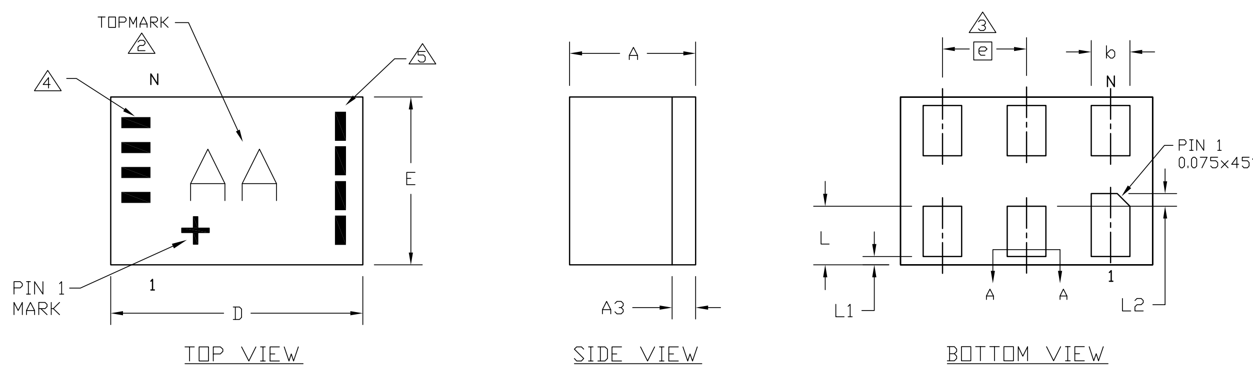


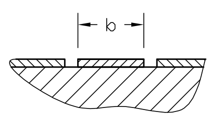
TITLE: PACKAGE OUTLINE, 6L SC70			
APPROVAL	DOCUMENT CONTROL NO. 21-0077	REV. H	1/1

-DRAWING NOT TO SCALE-

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.





SECTION A-A

SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A3	0.15 REF		
D	1.45	1.50	1.55
E	0.95	1.00	1.05
L	0.30	0.35	0.40
L1	0.00	--	0.08
L2	0.05	--	0.10
b	0.15	0.20	0.25
e	0.50 BSC.		
Pkg. Code	Y61A1-1, Y61A1-2		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY. PACKAGE USES 2 CHARACTER PRODUCT CODE.
3. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
4. CALENDAR YEAR BINARY DATE CODE (REFER TO PG. 2 TABLE 1 FOR TRANSLATION).
5. 6 WEEKLY DATE BINARY CODE (REFER TO PG. 2 TABLE 2 FOR TRANSLATION).
6. MEETS JEDEC MO-252 VARIATION WAAD.
7. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC# 10-0131.
8. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE
6L ULTRA THIN LGA, 1.5x1.0x0.5mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0190	C	1/2

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

TABLE 1 Translation Table for Calendar Year Code

Calendar Year	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
	□	□	□	■	□	□	■	□	■	■
	□	□	■	□	□	■	□	■	□	□
	□	■	□	□	■	□	□	■	■	■
	■	□	□	□	■	■	■	□	□	□

Legend: ■ Marked with bar □ Blank space - no bar required

TABLE 2 Translation Table for Payweek Binary Coding

Payweek	06-11	12-17	18-23	24-29	30-35	36-41	42-47	48-51	52-05
	□	□	□	■	□	□	■	□	■
	□	□	■	□	□	■	□	■	□
	□	■	□	□	■	□	□	■	■
	■	□	□	□	■	■	■	□	□

Legend: ■ Marked with bar □ Blank space - no bar required

TITLE:
PACKAGE OUTLINE
6L ULTRA THIN LGA, 1.5x1.0x0.5mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0190	C	2/2

-DRAWING NOT TO SCALE-

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	8/11	Added thin µDFN (ultra-thin LGA) package and updated slew rate and TOC 29	1, 2, 3, 8, 9, 12
2	10/11	Removed future product information from data sheet	12
3	2/12	Revised *Electrical Characteristics* and the *Power-Up Autotrim* section	2, 3, 11
4	7/12	Revised *Electrical Characteristics* and *Typical Operating Characteristics*	3, 6