

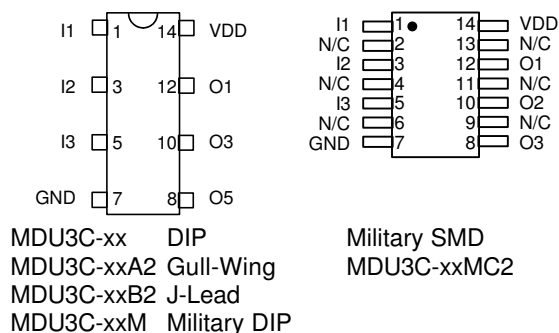
TRIPLE, HCMOS-INTERFACED FIXED DELAY LINE (SERIES MDU3C)



FEATURES

- Three independent delay lines
- Fits standard 14-pin DIP socket
- Low profile
- Auto-insertable
- Input & outputs fully CMOS interfaced & buffered
- 10 T²L fan-out capability

PACKAGES



FUNCTIONAL DESCRIPTION

The MDU3C-series device is a 3-in-1 digitally buffered delay line. The signal inputs (I1-I3) are reproduced at the outputs (O1-O3), shifted in time by an amount determined by the device dash number (See Table). The delay lines function completely independently of each other.

PIN DESCRIPTIONS

I1-I3	Signal Inputs
O1-O3	Signal Outputs
VDD	+5 Volts
GND	Ground

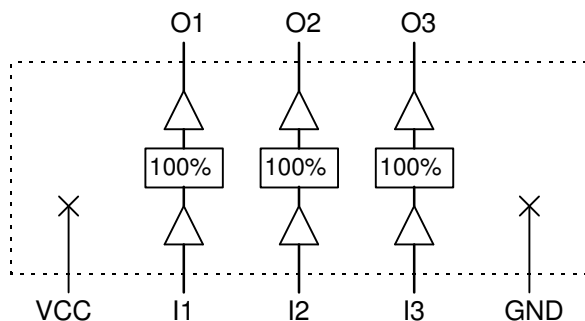
SERIES SPECIFICATIONS

- **Minimum input pulse width:** 100% of total delay
- **Output rise time:** 8ns typical
- **Supply voltage:** 5VDC \pm 5%
- **Supply current:** I_{CCL} = 40 μ a typical
 I_{CCH} = 60ma typical
- **Operating temperature:** 0° to 70° C
- **Temp. coefficient of total delay:** 300 PPM/°C

DASH NUMBER SPECIFICATIONS

Part Number	Delay Per Line (ns)
MDU3C-10	10 \pm 2.0
MDU3C-15	15 \pm 2.0
MDU3C-20	20 \pm 2.0
MDU3C-25	25 \pm 2.0
MDU3C-30	30 \pm 2.0
MDU3C-40	40 \pm 2.0
MDU3C-50	50 \pm 2.5
MDU3C-60	60 \pm 3.0
MDU3C-75	75 \pm 3.7
MDU3C-100	100 \pm 5.0

NOTE: Any dash number between 10 and 100 not shown is also available.



Functional block diagram

APPLICATION NOTES

HIGH FREQUENCY RESPONSE

The MDU3C tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 100% of the total delay and periods as small as 200% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data

Delay Devices if your application requires device testing at a specific input condition.

POWER SUPPLY BYPASSING

The MDU3C relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1uf capacitor from VDD to GND, located as close as possible to the VDD pin, is recommended. A wide VDD trace and a clean ground plane should be used.

DEVICE SPECIFICATIONS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

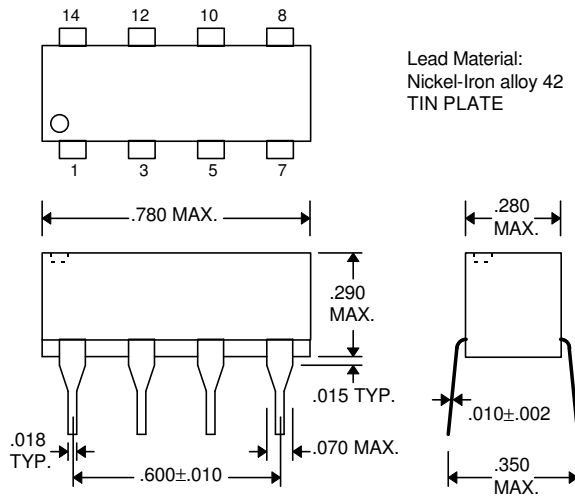
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V _{DD}	-0.3	7.0	V	
Input Pin Voltage	V _{IN}	-0.3	V _{DD} +0.3	V	
Storage Temperature	T _{STRG}	-55	150	C	
Lead Temperature	T _{LEAD}		300	C	10 sec

TABLE 2: DC ELECTRICAL CHARACTERISTICS

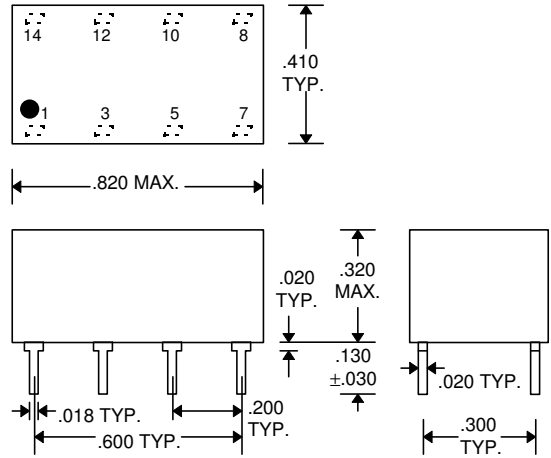
(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	V _{OH}	3.98	4.4		V	V _{DD} = 5.0, I _{OH} = MAX V _{IH} = MIN, V _{IL} = MAX
Low Level Output Voltage	V _{OL}		0.15	0.26	V	V _{DD} = 5.0, I _{OL} = MAX V _{IH} = MIN, V _{IL} = MAX
High Level Output Current	I _{OH}			-4.0	mA	
Low Level Output Current	I _{OL}			4.0	mA	
High Level Input Voltage	V _{IH}	3.15			V	
Low Level Input Voltage	V _{IL}			1.35	V	
Input Current	I _{IH}			0.10	μA	V _{DD} = 5.0

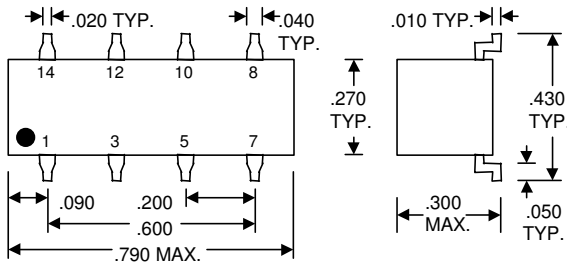
PACKAGE DIMENSIONS



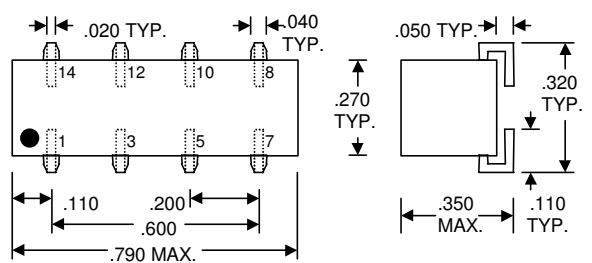
MDU3C-xx (Commercial DIP)



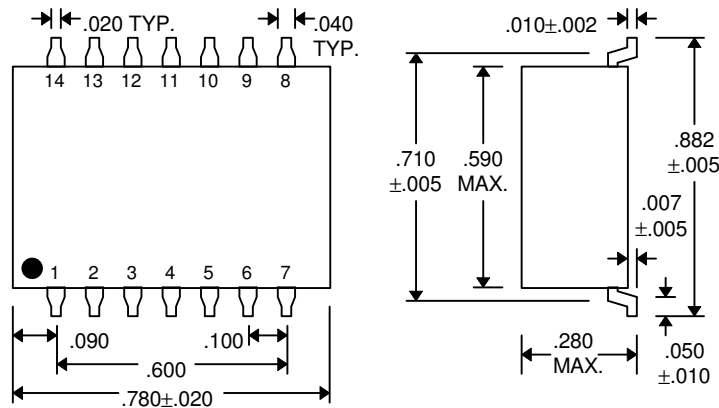
MDU3C-xxM (Military DIP)



MDU3C-xxA2 (Commercial Gull-Wing)



MDU3C-xxB2 (Commercial J-Lead)



MDU3C-xxMC2 (Military SMD)

DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

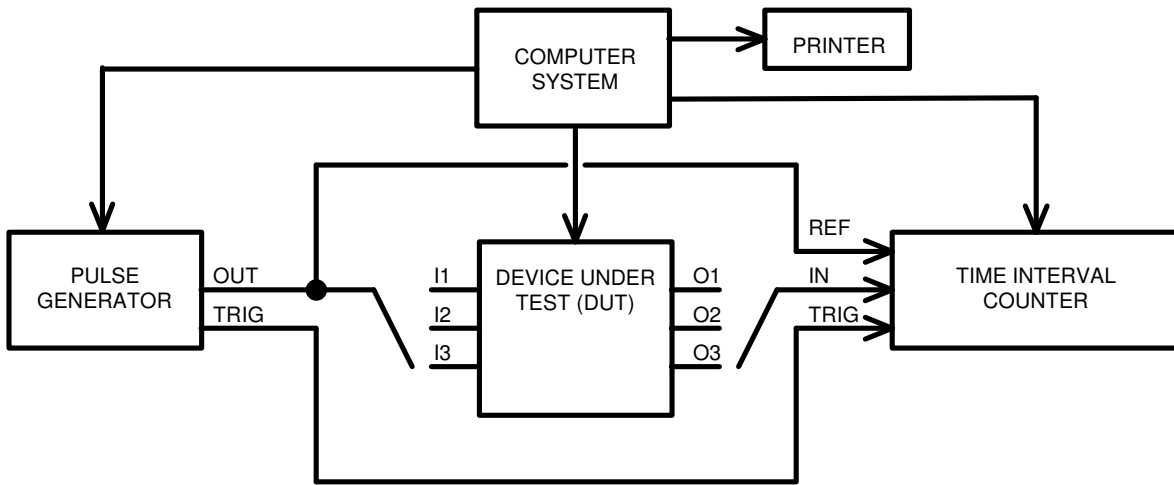
INPUT:

Ambient Temperature: $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$
Supply Voltage (VDD): $5.0\text{V} \pm 0.1\text{V}$
Input Pulse: High = $5.0\text{V} \pm 0.1\text{V}$
 Low = $0.0\text{V} \pm 0.1\text{V}$
Source Impedance: 50Ω Max.
Rise/Fall Time: 5.0 ns Max. (measured between 0.5V and 4.5V)
Pulse Width: $\text{PW}_{\text{IN}} = 1.5 \times \text{Total Delay}$
Period: $\text{PER}_{\text{IN}} = 10 \times \text{Total Delay}$

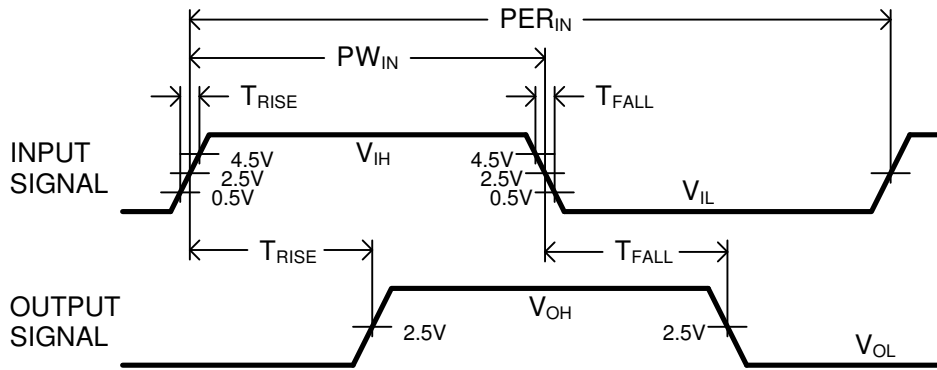
OUTPUT:

Load: 1 FAST-TTL Gate
C_{load}: $5\text{pf} \pm 10\%$
Threshold: 2.5V (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing