

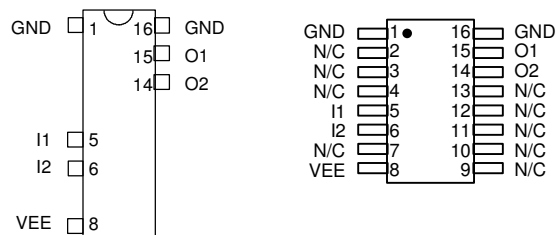
DUAL, ECL-INTERFACED FIXED DELAY LINE (SERIES MDU12H)



FEATURES

- Two independent delay lines
- Fits standard 16-pin DIP socket
- Auto-insertable
- Input & outputs fully 10KH-ECL interfaced & buffered

PACKAGES



MDU12H-xx DIP MDU12H-xxC3 SMD
MDU12H-xxM Military DIP MDU12H-xxMC3 Mil SMD

FUNCTIONAL DESCRIPTION

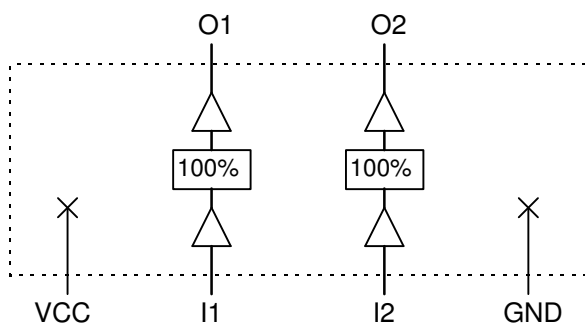
The MDU12H-series device is a 2-in-1 digitally buffered delay line. The signal inputs (I1-I2) are reproduced at the outputs (O1-O2), shifted in time by an amount determined by the device dash number (See Table). The delay lines function completely independently of each other.

PIN DESCRIPTIONS

I1-I2 Signal Inputs
O1-O2 Signal Outputs
VEE -5 Volts
GND Ground

SERIES SPECIFICATIONS

- **Minimum input pulse width:** 50% of total delay
- **Output rise time:** 2ns typical
- **Supply voltage:** -5VDC \pm 5%
- **Power dissipation:** 200mw typical (no load)
- **Operating temperature:** -30° to 85° C
- **Temp. coefficient of total delay:** 100 PPM/°C



Functional block diagram

DASH NUMBER SPECIFICATIONS

Part Number	Delay Per Line (ns)
MDU12H-3	3 \pm 1.0
MDU12H-4	4 \pm 1.0
MDU12H-5	5 \pm 1.0
MDU12H-10	10 \pm 1.0
MDU12H-15	15 \pm 1.0
MDU12H-20	20 \pm 1.0
MDU12H-25	25 \pm 2.0
MDU12H-30	30 \pm 2.0
MDU12H-35	35 \pm 2.0
MDU12H-40	40 \pm 2.0
MDU12H-45	45 \pm 2.2
MDU12H-50	50 \pm 2.5
MDU12H-60	60 \pm 3.0
MDU12H-75	75 \pm 3.7
MDU12H-100	100 \pm 5.0
MDU12H-125	125 \pm 6.2
MDU12H-150	150 \pm 7.5
MDU12H-200	200 \pm 10.0
MDU12H-250	250 \pm 12.5

* Total delay is referenced to first tap output
Input to first tap = 1.5ns \pm 1ns

NOTE: Any dash number between 3 and 50 not shown is also available.

APPLICATION NOTES

HIGH FREQUENCY RESPONSE

The MDU12H tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 50% of the total delay and periods as small as 100% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data

Delay Devices if your application requires device testing at a specific input condition.

POWER SUPPLY BYPASSING

The MDU12H relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1 μ f capacitor from VEE to GND, located as close as possible to the VEE pin, is recommended. A wide VEE trace and a clean ground plane should be used.

DEVICE SPECIFICATIONS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

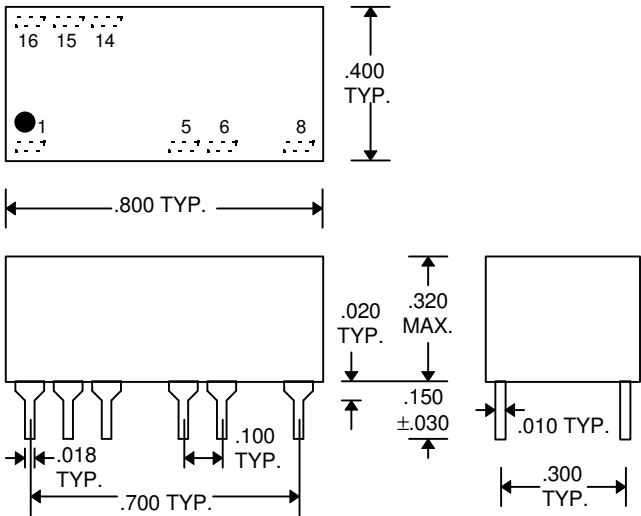
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V _{EE}	-7.0	0.3	V	
Input Pin Voltage	V _{IN}	V _{EE} - 0.3	0.3	V	
Storage Temperature	T _{STRG}	-55	150	C	
Lead Temperature	T _{LEAD}		300	C	10 sec

TABLE 2: DC ELECTRICAL CHARACTERISTICS

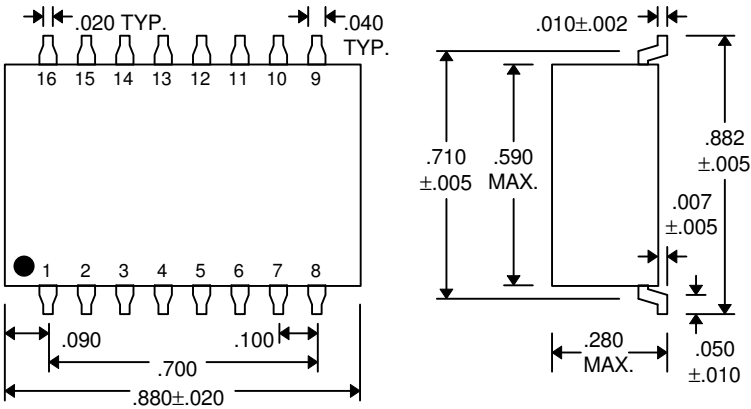
(0C to 75C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	V _{OH}	-1.020		-0.735	V	V _{IH} = MAX, 50 Ω to -2V
Low Level Output Voltage	V _{OL}	-1.950		-1.600	V	V _{IL} = MIN, 50 Ω to -2V
High Level Input Voltage	V _{IH}			-1.070	V	
Low Level Input Voltage	V _{IL}	-1.480			V	
High Level Input Current	I _{IH}			475	μ A	V _{IH} = MAX
Low Level Input Current	I _{IL}	0.5			μ A	V _{IL} = MIN

PACKAGE DIMENSIONS



MDU12H-xx (Commercial DIP)
MDU12H-xxM (Military DIP)



MDU12H-xxC3 (Commercial SMD)
MDU12H-xxMC3 (Military SMD)

DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:

Ambient Temperature: $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$

Supply Voltage (Vcc): $-5.0\text{V} \pm 0.1\text{V}$

Input Pulse: Standard 10KH ECL levels

Source Impedance: 50Ω Max.

Rise/Fall Time: 2.0 ns Max. (measured between 20% and 80%)

Pulse Width: $PW_{IN} = 1.5 \times \text{Total Delay}$

Period: $PER_{IN} = 10 \times \text{Total Delay}$

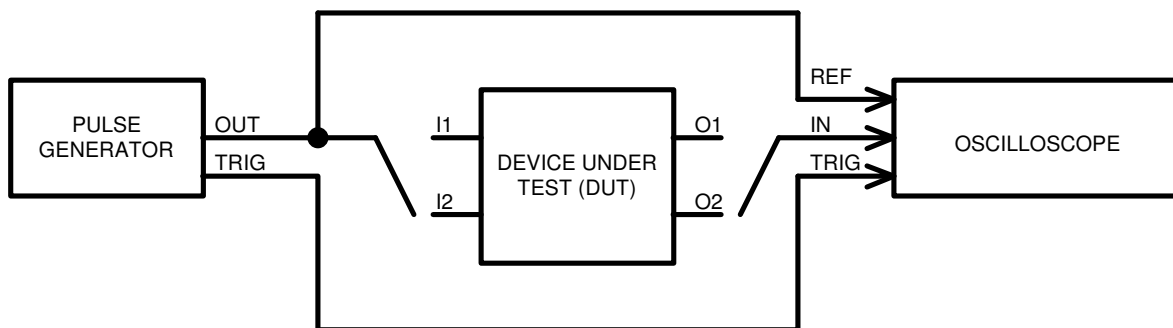
OUTPUT:

Load: 50Ω to -2V

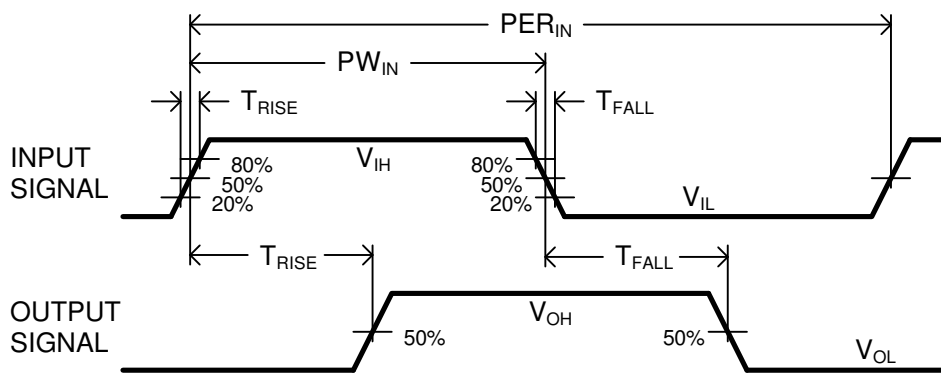
C_{load}: $5\text{pf} \pm 10\%$

Threshold: $(V_{OH} + V_{OL}) / 2$
(Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing