SY87724L

3.3V AnyRate® MUX/DEMUX Up to 2.7GHz

General Description

The SY87724L is a complete serial data multiplexer and demultiplexer, capable of operating at up to 2.7GHz. The device provides for muxing and demuxing to 4, 5, 8, or 10 bit wide buses.

The SY87724L can accept a synchronous code group or octet boundary input, and uses this input for parallel data alignment.

The SY87724L is manufactured in Micrel's high performance ASSET2™ silicon bipolar process.

Micrel provides a complete protocol transparent solution with the AnyRate® SY87721L CDR/CMU SY87729L, and the SY87724L integrated MUX/DEMUX.

Datasheets and support documentation can be found on Micrel's web site at www.micrel.com.

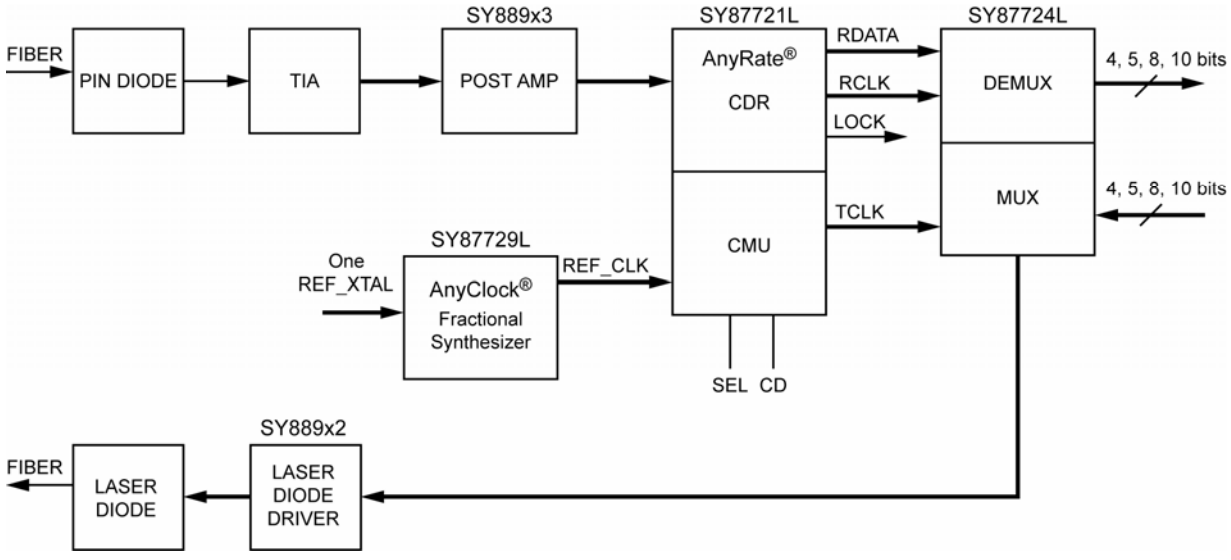
Features

- Protocol transparent MUX/DEMUX operation up to 2.7GHz
- Programmable to 4, 5, 8, or 10 bit parallel interfaces
- Differential clock and serial inputs/outputs
- Easily controlled by framer logic
- Synchronous frame boundary indication
- HSPC (High Speed PECL-Compatible) inputs and outputs
- 3.3V power supply
- Available in 80-pin EPAD-TQFP

Applications

- OC-3, OC-12, OC-48, ATM, InfiniBand
- Gigabit Ethernet
- Fibre Channel, 2X Fibre Channel
- SMPTE-259 and 292
- Proprietary optical transport
- ITU G. 975 Solutions

System Block Diagram



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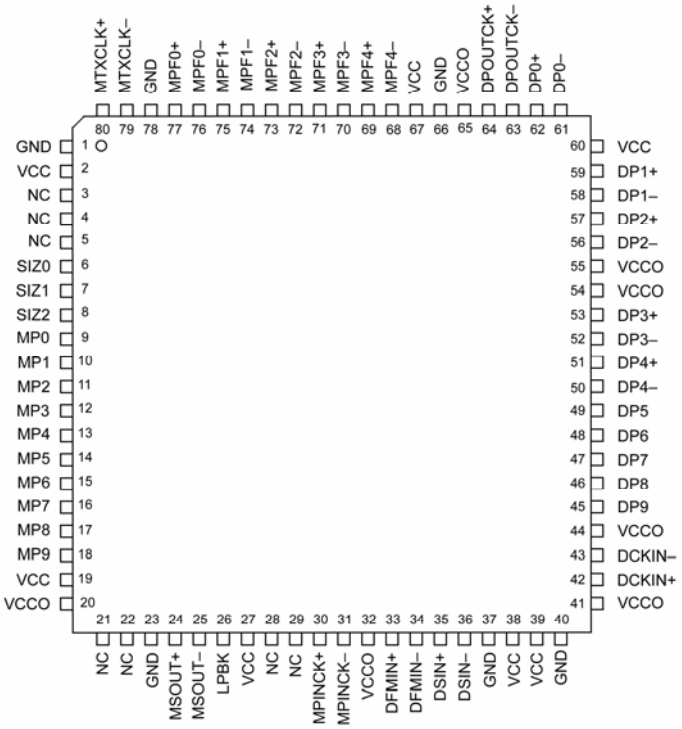
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish	Status
SY87724LHEI	H80-2	Industrial	SY87724LHEI	Sn-Pb	Active
SY87724LHEY	H80-2	Industrial	SY87724LHEY with Pb-Free bar line indicator	Matte-Sn Pb-Free	Active
SY87724LHI	H80-1	Industrial	SY87724LHI	Sn-Pb	Discontinued
SY87724LHY	H80-1	Industrial	SY87724LHY with Pb-Free bar line indicator	Matte-Sn Pb-Free	Discontinued
SY87724LHG	H80-1	Industrial	SY87724LHG with Pb-Free bar line indicator	NiPdAu Pb-Free	Discontinued

Note:

1. Other Voltage available. Contact Micrel for details.

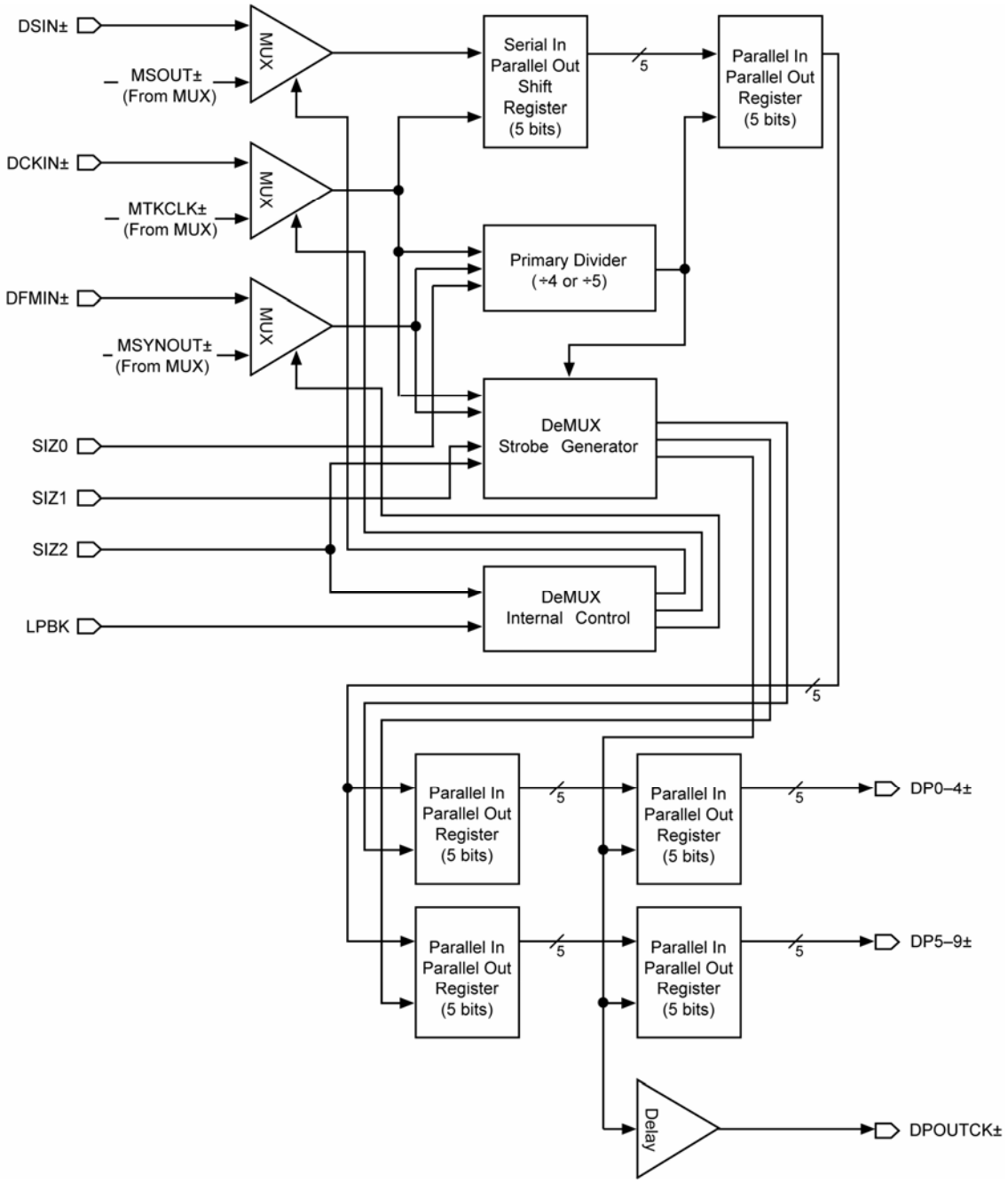
Pin Configuration



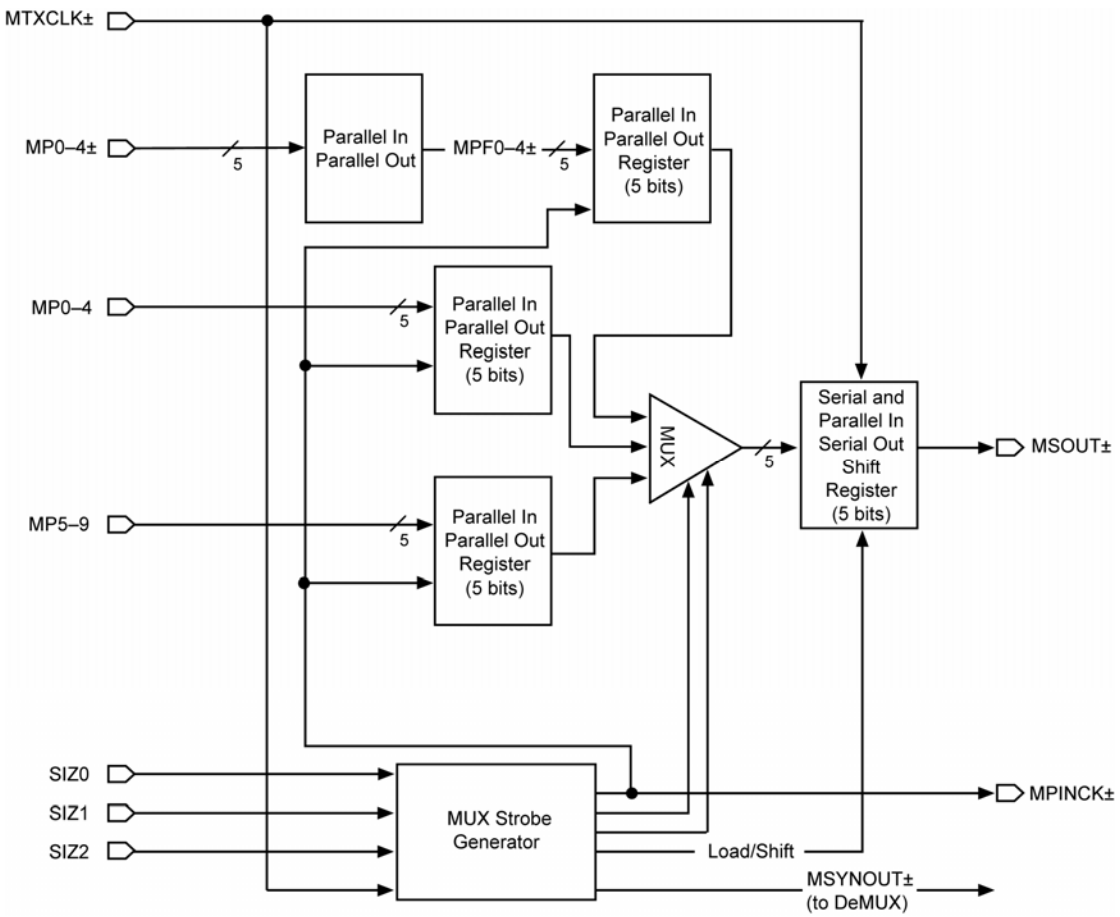
80-Pin EPAD-TQFP (H80-2)

Functional Block Diagram

DEMUX



MUX


MTXCLK±
MP0–4±
5
Parallel In Parallel Out
MPF0–4±
5
Parallel In Parallel Out Register (5 bits)
MP0–4
5
Parallel In Parallel Out Register (5 bits)
MP5–9
5
Parallel In Parallel Out Register (5 bits)
MUX
5
Serial and Parallel In Serial Out Shift Register (5 bits)
MSOUT±
SIZ0
SIZ1
SIZ2
MUX Strobe Generator
MPINCK±
Load/Shift
MSYNOUT± (to DeMUX)

Pin Description

COMMON

LPBK – TTL Input

This pin defines whether a device exhibits local loopback or not, as per the following table. Loopback internally connects MUX serial out to demux serial in, thus the user may expect MUX side parallel data to appear on the demux parallel output pins.

LPBK	Functioning
0	Loopback
1	Normal

Table 1. LPBK Input Pin Function

SIZ0, SIZ1, SIZ2 – TTL Input

These three signals determine the width of the parallel output, as well as the width of parallel input. The following table describes the parallel width options.

Width	SIZ0	SIZ1	SIZ2[1]
4	0	0	0
5	1	0	0
8	0	1	0
10	1	1	0
Undefined	X	X	1

Table 2. SIZ0, SIZ1, SIZ2 Input Truth Table

Note:

1. Pin 8 (SIZ2) should always be tied to a TTL logic level LOW.

DEMUX

DSIN± – Differential HSPC Input

This is the serial input to the SY87724L demux. It accepts the serial data and converts it to parallel data. It is ignored during loopback.

DCKIN± – Differential HSPC Input

This is the bit rate clock that feeds serial data into the demux shift register. This signal also feeds the demux strobe generator and primary divider, except during loopback.

DFMIN± – Differential HSPC Input

This is the frame alignment input signal. This signal resets the primary divider, as well as the strobe generator. This effectively sets the alignment for the parallel data being demuxed. Usually, DFMIN± asserts one DCKIN± before a parallel word boundary, and continues to assert one clock before every boundary. However, DFMIN± need only occur once for proper operation. Should DFMIN± assert at other than a previously set boundary, the DPOUTCK± signal will always occur later than would be expected. That is, there will never be a short DPOUTCK± pulse.

DP0± through DP4± – Differential PECL Output

These signals may be used as either differential, or single-ended. When converting to 4 or 5 bits, speed issues may encourage the use of these signals differentially. When converting to wider than 5 bits, these signals are to be used single-ended. Please refer to the applications section for further details.

DP5 through DP9 – PECL Output

These are the rest of the parallel output bits, to be used when converting to wider than 5 bits. Which bits are valid depends on the values of SIZ0, SIZ1, and SIZ2. Please refer to the table in the applications section for further details.

DPOUTCK± – Differential HSPC Output

This signal is used to strobe the DP0-9 data. It is used differentially when converting to 4 or 5 bits, and is used single-ended when converting to wider than 5 bits. The clock rate of the line will be determined by the DCKIN signal, and by the setting of the SIZ bits. This output always provides valid differential logic levels.

MUX

MP0-9 – PECL Input

These bits accept data for muxing wider than 5 bits. MPINCK+, used single-ended, determines when this data may change. Please refer to the table in the description for which pins represent what bits for various widths.

MPF0–4± – Differential PECL Input

These signals are used when muxing 4 or 5 bits of parallel data. MPINCK± determines when this data may change. Please refer to the MUX table in the description for which pins represent what bits for various widths.

MTXCLK± – Differential HSPC Input

This is the serial rate clock input to the MUX. It determines the rate at which serial data will be shifted out of the MUX.

MSOUT± – Differential PECL Output

This signal is the serialized data output.

MPINCK± – Differential PECL Output

This signal indicates when the next set of parallel bits may be presented to the SY87724L for muxing. For muxing wider than 5 bits, MPINCK+ is used single-ended. These signals always provide valid differential clock signals regardless of single-ended or differential data mode.

OTHER

V_{CC}	Supply Voltage
V_{CCO}	Output Supply Voltage
GND	Ground
NC	These pins are reserved and are to be left unconnected.

Note:

1. All differential outputs always provide valid differential logic levels regardless of differential or single-ended use.

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Description

General

The SY87724L MDM is designed to perform muxing and demuxing at up to 2.7GHz speeds. The device can simultaneously MUX and demux up to 10 bits of full duplex data. In addition, a full parallel-to-parallel loopback function is implemented, such that parallel data out will loop back to parallel data in, with the device internally connecting the serial output to the serial input.

Narrow DeMUX

In this example, serial data is converted into 4 or 5 bit wide data. Because this can result in very high data rates on the parallel outputs, they are differential. The DFMIN± input indicates, synchronously with DCKIN±, and one clock ahead, the start of a 4 or 5 bit boundary.

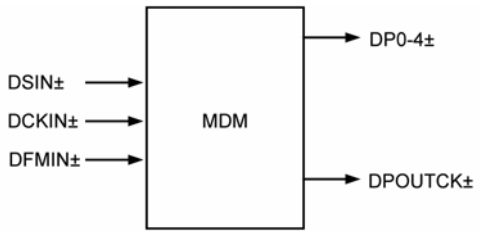

Figure 1. Narrow DeMUX

Every DFMIN± assertion will trigger a new 4 or 5 bit boundary. Should only one DFMIN± assertion occur, then DPOUTCK± will continue to assert every 4 or 5 DCKIN± clocks. Should a subsequent DFMIN± assertion reset the 4 or 5 bit boundary, then DPOUTCK± will always result in a longer assertion, not a shorter one.

For example, if a subsequent DFMIN± resets a 5 bit boundary after the second bit in relation to a previous boundary, then the next DPOUTCK± will always occur 7 DCKIN± later, never 2 DCKIN± later. For four bit output, DP5± are not used.

Wide DeMUX

The more typical case will be to convert the serial data stream into 8 or 10 bit wide data. Because the worst case parallel transfer rate is on the order of 250 to 340 Mega-transfers per second, single ended parallel output is preferred. Thus, only the single-ended side of the differential outputs is used.

This example is much like the narrow demux, except now DFMIN± indicates 8 or 10 bit boundaries.

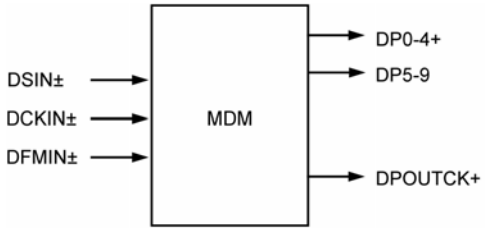

Figure 2. Wide DeMUX

As in the narrow case, DPOUTCK± will never assert twice in 8 or 10 DCKIN± cycles. Should a DFMIN± assertion change the MDM's 8 or 10 bit boundary, DPOUTCK± assertion will be delayed and there will never be a short assertion.

For 8 bit output, DP4± and DP9 are not used.

The following table summarizes the available bit widths. The right column shows the parallel bits, in sequence from first in serially, to last in.

Width	Sequence
4	DP0±, DP1±, DP2±, DP3±
5	DP0±, DP1±, DP2±, DP3±, DP4±
8	DP0+, DP1+, DP2+, DP3+, DP5, DP6, DP7, DP8
10	DP0+, DP1+, DP2+, DP3+, DP4+, DP5, DP6, DP7, DP8, DP9

Table 3. Output Pins for Different Width DeMUX

Narrow MUX

In this scenario, 4 or 5 bit wide parallel data is converted to a serial bit stream. Because this can result in very high data rates on the parallel inputs, they are differential. In this mode of operation, there is no external synchronization, and the MPINCK± signal pair has arbitrary phase with respect to the MTXCLK± clock, which clocks the MUX output shift register.

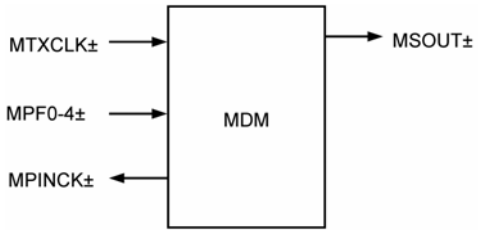

Figure 3. Narrow MUX

MPINCK± indicates when MDM is ready to accept more data. It is derived from MTXCLK±, with an arbitrary phase relationship.

Wide MUX

The more typical case will be to convert 8 or 10 bit wide parallel data words into a serial bit stream. Because the worst case parallel input rate is on the order of 250 to 340 Mega-transfers per second, single-ended parallel inputs are used.

This scenario is much like the narrow MUX case, except now MPINCK+ clocks slower, for 8- or 10-bit parallel words.

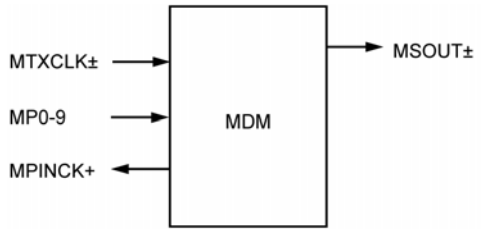

Figure 4. Wide MUX

Note that the input data indication is now single ended, and that completely different input pins are used, as compared to the 4 or 5 bit case.

The following table summarizes the available bit widths. The right column shows the parallel input bits, such as they will appear in the serial output stream.

Width	Sequence
4	MPF0±, MPF1±, MPF2±, MPF3±
5	MPF0±, MPF1±, MPF2±, MPF3±, MPF4±
8	MP5, MP6, MP7, MP8, MP0, MP1, MP2, MP3
10	MP5, MP6, MP7, MP8, MP9, MP0, MP1, MP2, MP3, MP4

Table 4. Output Pins for Different Width MUX

Loopback

To ease system design, the SY87724L MDM has the capability to loop parallel data in, through the MUX, into the demux, and back to parallel data out. This permits system check-out through to the individual MDM device. Note that, for a full check-out, some form of loopback further down the serial stream is required.

Loopback is incorporated into MDM by modifying the serial clock, data, and sync inputs to the demux stage.

During loopback, the source of serial information for the demux is changed. The MSOUT±, MTXCLK± and MSYNOUT± are internally muxed to the DSIN±, DCKIN±, and DFMIN± nodes of the demux section. The MSYNOUT± signal has the same characteristics as the DFMIN logic expects.

This exercises the internal data path, both MUX and demux, for MDM, and also the control logic. The parallel data presented to the parallel inputs will appear, some small but unspecified time later, at the parallel outputs.

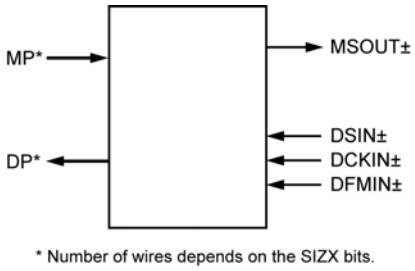

Figure 5. Loopback Function

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Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +3.8V
Input Voltage (V_{IN}). ..... –0.5V to V_{CC}[3]
ECL Output Current (I_{OUT})
Continuous 50mA
Surge 100mA
Lead Temperature (soldering, 20sec.) ..... +260°C
Storage Temperature (T_s) ..... –65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +3.15V to +3.45V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance
EPAD-TQFP (θ_{JA}) Still-air ..... 21°C/W
EPAD-TQFP (θ_{JA}) @ 200 LFM[5] ..... 15°C/W

DC Electrical Characteristics

V_{CC} = V_{CCA} = 3.15V to 3.45V; T_A = –40°C to+85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.15	3.3	3.45	V
I_{CC}	Power Supply Current			650	750	mA

HSPC DC Electrical Characteristics

V_{CC} = V_{CCA} = 3.15V to 3.45V; T_A = –40°C to+85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		V_{CC}–1.165		V_{CC}–0.880	V
V_{IL}	Input LOW Voltage		V_{CC}–1.810		V_{CC}–1.475	V
I_{IL}	Input LOW Current	V_{IN} = V_{IL} (Min)	–0.5			µA
V_{OH}	Output HIGH Voltage	50Ω to V_{CC}–2V	V_{CC}–1.0		V_{CC}–0.75	V
V_{OL}	Output LOW Voltage	50Ω to V_{CC}–2V	V_{CC}–1.55		V_{CC}–1.25	V
V_{OSW}	Output Voltage Differential Swing		0.3			V

PECL DC Electrical Characteristics

V_{CC} = V_{CCA} = 3.15V to 3.45V; T_A = –40°C to+85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		V_{CC}–1.165		V_{CC}–0.880	V
V_{IL}	Input LOW Voltage		V_{CC}–1.810		V_{CC}–1.475	V
I_{IL}	Input LOW Current	V_{IN} = V_{IL} (Min)	–0.5			µA
V_{OH}	Output HIGH Voltage	50Ω to V_{CC}–2V	V_{CC}–1.075		V_{CC}–0.830	V
V_{OL}	Output LOW Voltage	50Ω to V_{CC}–2V	V_{CC}–1.860		V_{CC}–1.570	V
V_{OSW}	Output Voltage Differential Swing		0.6			V

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum value is specified at V_{CC} up to V_{CC} = +6V.
4. It is recommended for the part to be used with 200 LFM airflow.

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TTL DC Electrical Characteristics

V_{CC} = V_{CCA} = 3.15V to 3.45V; T_A = –40°C to+85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7V, V_{CC} = Max.			+20	µA
		V_{IN} = V_{CC}, V_{CC} = Max.			+100	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V, V_{CC} = Max.			300	µA

AC Electrical Characteristics

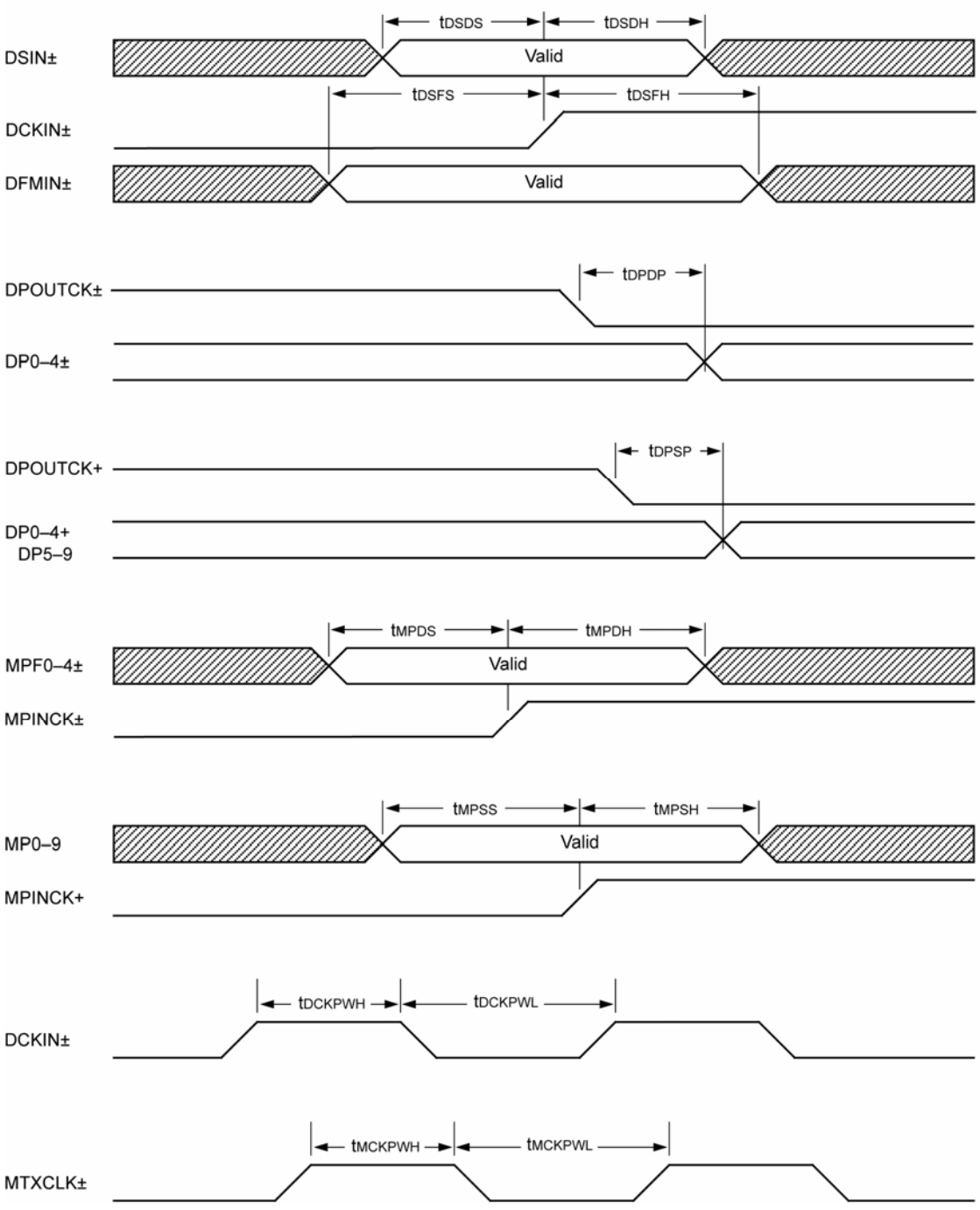
V_{CC} = V_{CCA} = 3.15V to 3.45V; T_A = –40°C to+85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency		2.7			GHz
t_{DCKPWH}, t_{DCKPWL}	Demux Clock Pulse Duty Cycle		45		55	%
t_{DSDS}	Demux Serial Data Set-Up		200			ps
t_{DSDH}	Demux Serial Data Hold		0			ps
t_{DSFS}	Demux Serial Frame Set-Up		150			ps
t_{DSFH}	Demux Serial Frame Hold		50			ps
t_{DPDP}	Demux Parallel Differential Propagation		+200		+800	ps
t_{DPSP}	Demux Parallel Single-Ended Propagation		+200		+1200	ps
t_{MCKPWH} t_{MCKPWL}	MUX Clock Pulse Duty Cycle		45		55	%
t_{MPDS}	MUX Parallel Differential Set-Up(1)		t_{CYC}+650			ps
t_{MPDH}	MUX Parallel Differential Hold(1)		–(t_{CYC}+250)			ps
t_{MPSS}	MUX Parallel Single-Ended Set-Up(1)		t_{CYC}+850			ps
t_{MPSH}	MUX Parallel Single-Ended Hold(1)		–(t_{CYC}+50)			ps
t_R, t_F	Output Rise/Fall Times MCKOUT, MSOUT, MSYNOUT All Others	50Ω to V_{CC}–2V (20% to 80%)		100	120 500	ps

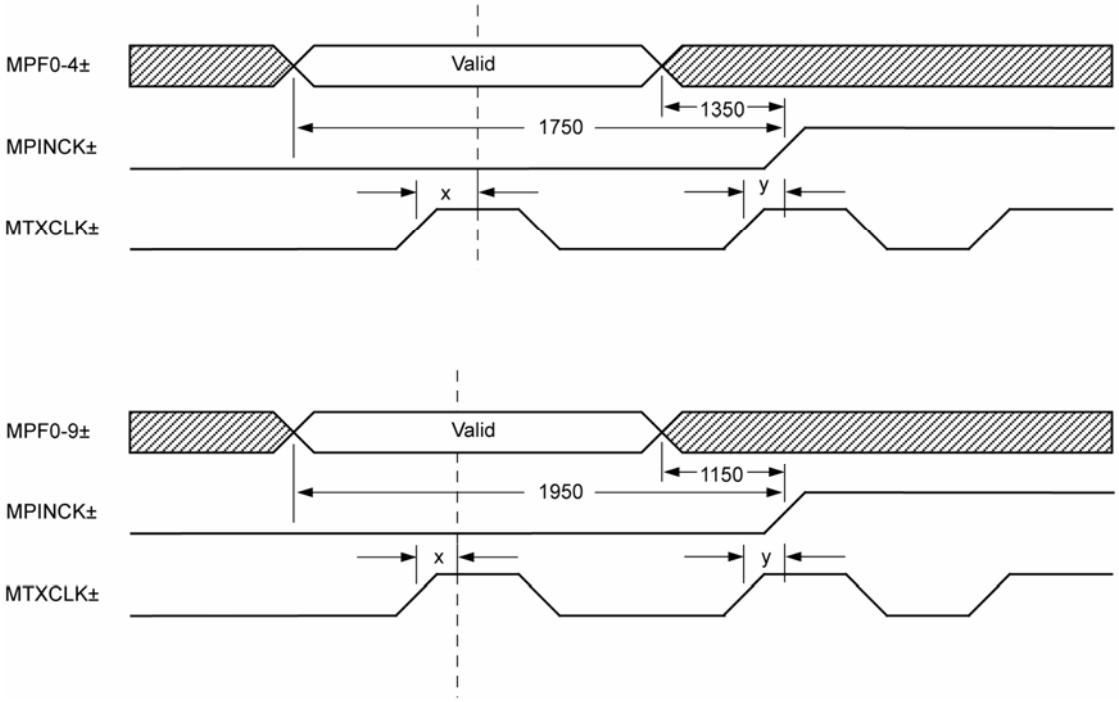
Notes:

1. t_{CYC} = the period of the clock being fed into MTXCLK.

Timing Waveforms



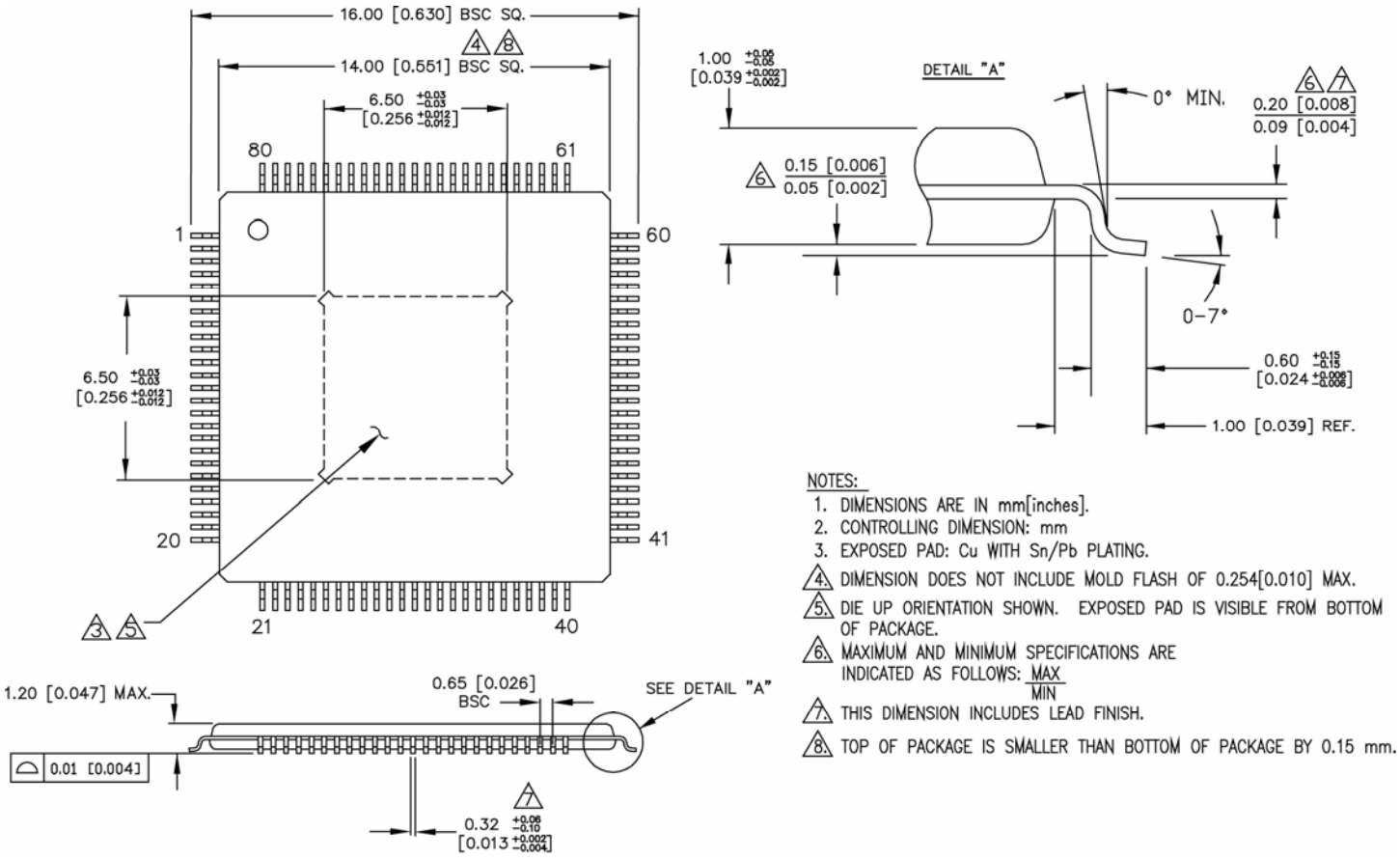
Timing Application Example



Notes:

1. MTXCLK = 1Gbps.
2. Time "*x*" is approximately equal to time "*y*."
3. Set-up and hold for MPF0-4± conditional on the MTXCLK± rising edge just prior to the MTXCLK± rising edge that causes an MPINCK± rising edge.

Package Information(1, 2)



80-Pin EPAD-TQFP (14 x 14 x 1.0mm) (H80-2)

Notes:

1. Exposed pads must be soldered to a ground plane for proper thermal management.
2. It is recommended for the part to be used with 200LFM airflow.

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