

## FEATURES

- 2.5V and 3.3V power supply options
- Guaranteed AC parameters over temperature:
  - $f_{MAX} = 3\text{GHz}$
  - $< 25\text{ps}$  output-to-output skew
  - $< 250\text{ps}$   $t_r / t_f$
  - $< 400\text{ps}$  propagation delay
- Wide temperature range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- Differential design
- $V_{BB}$  output for single-ended input applications
- Fully compatible with industry standard 100K I/O levels
- Available in 32-pin TQFP package



Precision Edge®

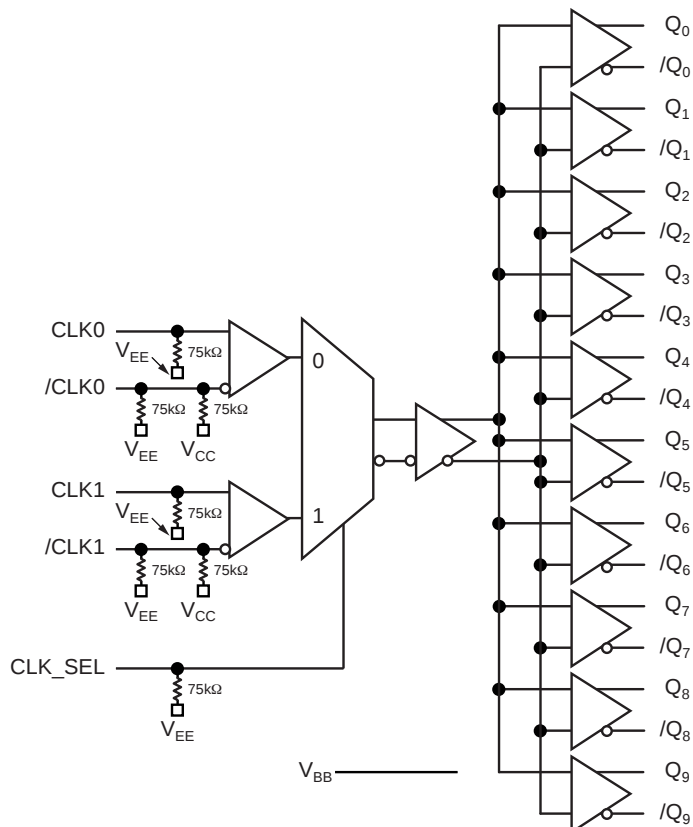
## DESCRIPTION

The SY100EP111U is a high-speed, low skew 1-to-10 differential fanout buffer designed for clock distribution in new, high-performance systems. The internal 2:1 mux allows the input to select between two differential clock sources.

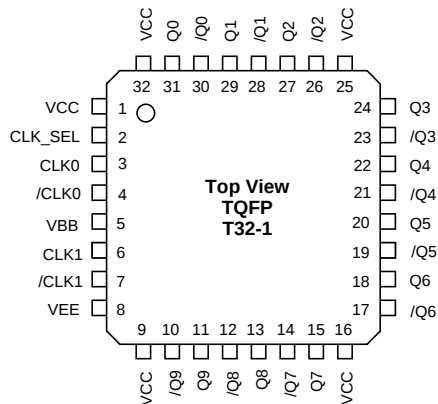
The device is specifically designed for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot.

The  $V_{BB}$  output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using  $V_{BB}$  for this purpose, it is recommended that  $V_{BB}$  is decoupled to  $V_{CC}$  via a  $0.01\mu\text{F}$  capacitor.

## BLOCK DIAGRAM



## PACKAGE/ORDERING INFORMATION



32-Pin TQFP (T32-1)

Ordering Information<sup>(1)</sup>

| Part Number                       | Package Type | Operating Range | Package Marking                             | Lead Finish    |
|-----------------------------------|--------------|-----------------|---------------------------------------------|----------------|
| SY100EP111UTI                     | T32-1        | Industrial      | 100EP111UTI                                 | Sn-Pb          |
| SY100EP111UTITR <sup>(2)</sup>    | T32-1        | Industrial      | 100EP111UTI                                 | Sn-Pb          |
| SY100EP111UTG <sup>(3)</sup>      | T32-1        | Industrial      | 100EP111UTG with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY100EP111UTGTR <sup>(2, 3)</sup> | T32-1        | Industrial      | 100EP111UTG with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY100EP111UTGTX <sup>(2, 4)</sup> | T32-1        | Industrial      | 100EP111UTG with Pb-Free bar-line indicator | Pb-Free NiPdAu |

## Notes:

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.
4. EIA specification orientation.

## PIN NAMES

| Pin         | Function                                                                                                                                                                                                      |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK0, /CLK0 | LVPECL, LVECL, HSTL Clock Inputs: CLK0 input includes a 75k $\Omega$ pull-down. Default is low if left floating. /CLK0 includes an internal 75k $\Omega$ pull-up and pull-down. Default state is $V_{CC}/2$ . |
| CLK1, /CLK1 | LVPECL, LVECL, HSTL Clock Inputs: CLK input includes a 75k $\Omega$ pull-down. Default is low if left floating. /CLK includes an internal 75k $\Omega$ pull-up and pull-down. Default state is $V_{CC}/2$ .   |
| Q0 to Q9    | LVPECL/LVECL Outputs.                                                                                                                                                                                         |
| /Q0 to /Q9  | Complementary LVPECL/LVECL Outputs.                                                                                                                                                                           |
| CLK_SEL     | LVPECL/LVECL Clock Select Input: Internal 75k $\Omega$ resistor connected to $V_{EE}$ . When left floating, the default condition is LOW.                                                                     |
| $V_{BB}$    | Reference Voltage: AC coupled or single-ended input applications.                                                                                                                                             |
| $V_{CC}$    | Positive Power Supply: Bypass with 0.1 $\mu\text{F}$ //0.01 $\mu\text{F}$ low ESR capacitors.                                                                                                                 |
| $V_{EE}$    | Negative Power Supply: LVPECL operation, connect to GND.                                                                                                                                                      |

## FUNCTION TABLE

| CLK_SEL | Active Input |
|---------|--------------|
| 0       | CLK0, /CLK0  |
| 1       | CLK1, /CLK1  |

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

| Symbol            | Rating                                                                                                                                                   | Value                  | Unit |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------|
| $V_{CC} - V_{EE}$ | Power Supply Voltage                                                                                                                                     | 6.0                    | V    |
| $V_{IN}$          | Input Voltage ( $V_{CC} = 0V$ , $V_{IN}$ not more negative than $V_{EE}$ )<br>Input Voltage ( $V_{EE} = 0V$ , $V_{IN}$ not more positive than $V_{CC}$ ) | -6.0 to 0<br>+6.0 to 0 | V    |
| $I_{OUT}$         | Output Current<br>–Continuous<br>–Surge                                                                                                                  | 50<br>100              | mA   |
| $I_{BB}$          | $V_{BB}$ Sink/Source Current <sup>(2)</sup>                                                                                                              | ±0.5                   | mA   |
| $T_{LEAD}$        | Lead Temperature (soldering, 20sec.)                                                                                                                     | +260                   | °C   |
| $T_A$             | Operating Temperature Range                                                                                                                              | -40 to +85             | °C   |
| $T_{store}$       | Storage Temperature Range                                                                                                                                | -65 to +150            | °C   |
| $\theta_{JA}$     | Package Thermal Resistance (Junction-to-Ambient)<br>–Still-Air<br>–500lfpm                                                                               | 50<br>42               | °C/W |
| $\theta_{JC}$     | Package Thermal Resistance (Junction-to-Case)                                                                                                            | 20                     | °C/W |

**Note 1.** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2.** Due to the limited drive capability, use for inputs of same package only.

**DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

| Symbol   | Parameter                  | $T_A = -40^{\circ}\text{C}$ |        |        | $T_A = +25^{\circ}\text{C}$ |        |        | $T_A = +85^{\circ}\text{C}$ |        |        | Unit     | Condition                              |
|----------|----------------------------|-----------------------------|--------|--------|-----------------------------|--------|--------|-----------------------------|--------|--------|----------|----------------------------------------|
|          |                            | Min.                        | Typ.   | Max.   | Min.                        | Typ.   | Max.   | Min.                        | Typ.   | Max.   |          |                                        |
| $V_{CC}$ | Power Supply Voltage       |                             |        |        |                             |        |        |                             |        |        |          |                                        |
|          | (LVPECL)                   | 2.375                       | —      | 3.8    | 2.375                       | —      | 3.8    | 2.375                       | —      | 3.8    | V        |                                        |
|          | (LVECL)                    | -3.8                        | —      | -2.375 | -3.8                        | —      | -2.375 | -3.8                        | —      | -2.375 | V        |                                        |
| $I_{EE}$ | Power Supply Current       | —                           | 55     | 120    | —                           | 70     | 120    | —                           | 85     | 120    | mA       |                                        |
| $I_{IH}$ | Input HIGH Current         | —                           | —      | 150    | —                           | —      | 150    | —                           | —      | 150    | μA       | $V_{IN} = V_{IH}$                      |
| $I_{IL}$ | Input LOW Current          |                             |        |        |                             |        |        |                             |        |        |          |                                        |
|          | CLK0, CLK1<br>/CLK0, /CLK1 | 0.5<br>-150                 | —<br>— | —<br>— | 0.5<br>-150                 | —<br>— | —<br>— | 0.5<br>-150                 | —<br>— | —<br>— | μA<br>μA | $V_{IN} = V_{IL}$<br>$V_{IN} = V_{IL}$ |
| $C_{IN}$ | Input Capacitance          | —                           | —      | —      | —                           | 2      | —      | —                           | —      | —      | pF       |                                        |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

**LVPECL DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>** $V_{CC} = 3.3V \pm 10\%$ ;  $V_{EE} = 0V$ 

| Symbol      | Parameter                                           | $T_A = -40^\circ C$ |      |          | $T_A = +25^\circ C$ |      |          | $T_A = +85^\circ C$ |      |          | Unit | Condition                 |
|-------------|-----------------------------------------------------|---------------------|------|----------|---------------------|------|----------|---------------------|------|----------|------|---------------------------|
|             |                                                     | Min.                | Typ. | Max.     | Min.                | Typ. | Max.     | Min.                | Typ. | Max.     |      |                           |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                   | 2135                | —    | 2420     | 2135                | —    | 2420     | 2135                | —    | 2420     | mV   |                           |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                    | 1355                | —    | 1675     | 1355                | —    | 1675     | 1355                | —    | 1675     | mV   |                           |
| $V_{OL}$    | Output LOW Voltage                                  | 1355                | 1480 | 1605     | 1355                | 1480 | 1605     | 1355                | 1480 | 1605     | mV   | $50\Omega$ to $V_{CC}-2V$ |
| $V_{OH}$    | Output HIGH Voltage                                 | 2155                | 2280 | 2405     | 2155                | 2280 | 2405     | 2155                | 2280 | 2405     | mV   | $50\Omega$ to $V_{CC}-2V$ |
| $V_{BB}$    | Reference Voltage <sup>(2)</sup>                    | 1775                | 1875 | 1975     | 1775                | 1875 | 1975     | 1775                | 1875 | 1975     | mV   |                           |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range <sup>(3)</sup> | 1.2                 | —    | $V_{CC}$ | 1.2                 | —    | $V_{CC}$ | 1.2                 | —    | $V_{CC}$ | V    |                           |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output varies 1:1 with  $V_{CC}$ .

**Note 2.** Single-ended input operation is limited  $V_{CC} \geq 3.0V$  in LVPECL mode.  $V_{BB}$  reference varies 1:1 with  $V_{CC}$ .

**Note 3.**  $V_{IHCMR}$  (Min) varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  (Max) varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**LVPECL DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>** $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ 

| Symbol      | Parameter                                           | $T_A = -40^\circ C$ |      |          | $T_A = +25^\circ C$ |      |          | $T_A = +85^\circ C$ |      |          | Unit | Condition                 |
|-------------|-----------------------------------------------------|---------------------|------|----------|---------------------|------|----------|---------------------|------|----------|------|---------------------------|
|             |                                                     | Min.                | Typ. | Max.     | Min.                | Typ. | Max.     | Min.                | Typ. | Max.     |      |                           |
| $V_{IH}$    | Input HIGH Voltage (Single-ended)                   | 1335                | —    | 1620     | 1335                | —    | 1620     | 1335                | —    | 1620     | mV   |                           |
| $V_{IL}$    | Input LOW Voltage (Single-ended)                    | 555                 | —    | 875      | 555                 | —    | 875      | 555                 | —    | 875      | mV   |                           |
| $V_{OL}$    | Output LOW Voltage                                  | 555                 | 680  | 805      | 555                 | 680  | 805      | 555                 | 680  | 805      | mV   | $50\Omega$ to $V_{CC}-2V$ |
| $V_{OH}$    | Output HIGH Voltage                                 | 1355                | 1480 | 1605     | 1355                | 1480 | 1605     | 1355                | 1480 | 1605     | mV   | $50\Omega$ to $V_{CC}-2V$ |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range <sup>(2)</sup> | 1.2                 | —    | $V_{CC}$ | 1.2                 | —    | $V_{CC}$ | 1.2                 | —    | $V_{CC}$ | V    |                           |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output varies 1:1 with  $V_{CC}$ .

**Note 2.**  $V_{IHCMR}$  (Min) varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  (Max) varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**LVECL DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>** $V_{EE} = -2.375V$  to  $-3.8V$ ;  $V_{CC} = 0V$ 

| Symbol      | Parameter                                           | $T_A = -40^{\circ}C$ |       |       | $T_A = +25^{\circ}C$ |       |       | $T_A = +85^{\circ}C$ |       |       | Unit | Condition          |
|-------------|-----------------------------------------------------|----------------------|-------|-------|----------------------|-------|-------|----------------------|-------|-------|------|--------------------|
|             |                                                     | Min.                 | Typ.  | Max.  | Min.                 | Typ.  | Max.  | Min.                 | Typ.  | Max.  |      |                    |
| $V_{IL}$    | Input LOW Voltage (Single-ended)                    | -1945                | —     | -1625 | -1945                | —     | -1625 | -1945                | —     | -1625 | mV   |                    |
| $V_{IH}$    | Input HIGH Voltage (Single-ended)                   | -1165                | —     | -0880 | -1165                | —     | -0880 | -1165                | —     | -0880 | mV   |                    |
| $V_{OL}$    | Output LOW Voltage                                  | -1945                | -1820 | -1695 | -1945                | -1820 | -1695 | -1945                | -1820 | -1695 | mV   | 50Ω to $V_{CC}-2V$ |
| $V_{OH}$    | Output HIGH Voltage                                 | -1145                | -1020 | -0895 | -1145                | -1020 | -0895 | -1145                | -1020 | -0895 | mV   | 50Ω to $V_{CC}-2V$ |
| $V_{BB}$    | Output Reference Voltage <sup>(2)</sup>             | -1525                | -1425 | -1325 | -1525                | -1425 | -1325 | -1525                | -1425 | -1325 | mV   |                    |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range <sup>(3)</sup> | $V_{EE} + 1.2$       |       | 0.0   | $V_{EE} + 1.2$       |       | 0.0   | $V_{EE} + 1.2$       |       | 0.0   | V    |                    |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

**Note 2.** Single-ended input operation is limited  $V_{EE} \leq -3.0V$  in LVECL mode.

**Note 3.**  $V_{IHCMR}$  (min) varies 1:1 with  $V_{EE}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**HSTL DC ELECTRICAL CHARACTERISTICS** $V_{CC} = 2.375V$  to  $3.8V$ ;  $V_{EE} = 0V$ 

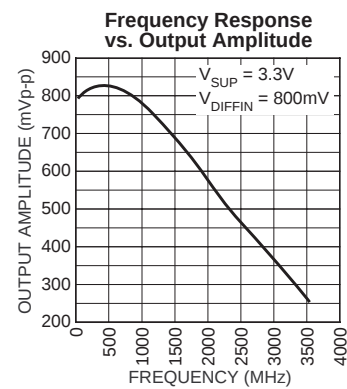
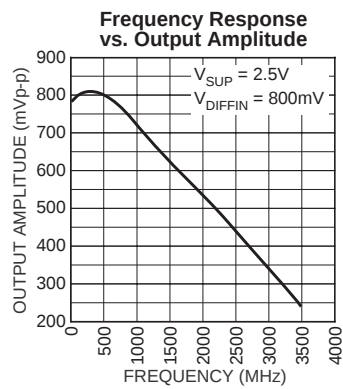
| Symbol   | Parameter               | $T_A = -40^{\circ}C$ |      |      | $T_A = +25^{\circ}C$ |      |      | $T_A = +85^{\circ}C$ |      |      | Unit |
|----------|-------------------------|----------------------|------|------|----------------------|------|------|----------------------|------|------|------|
|          |                         | Min.                 | Typ. | Max. | Min.                 | Typ. | Max. | Min.                 | Typ. | Max. |      |
| $V_{IH}$ | Input HIGH Voltage      | 1200                 | —    | —    | 1200                 | —    | —    | 1200                 | —    | —    | mV   |
| $V_{IL}$ | Input LOW Voltage       | —                    | —    | 400  | —                    | —    | 400  | —                    | —    | 400  | mV   |
| $V_X$    | Input Crossover Voltage | 680                  | —    | 900  | 680                  | —    | 900  | 680                  | —    | 900  | mV   |

**AC ELECTRICAL CHARACTERISTICS**(LVPECL)  $V_{CC} = 2.375$  to  $3.8V$ ,  $V_{EE} = 0V$ ; (LVECL)  $V_{EE} = -2.375V$  to  $-3.8V$ ,  $V_{CC} = 0V$ 

| Symbol       | Parameter                          | $T_A = -40^{\circ}C$ |      |      | $T_A = +25^{\circ}C$ |      |      | $T_A = +85^{\circ}C$ |      |      | Unit | Condition |
|--------------|------------------------------------|----------------------|------|------|----------------------|------|------|----------------------|------|------|------|-----------|
|              |                                    | Min.                 | Typ. | Max. | Min.                 | Typ. | Max. | Min.                 | Typ. | Max. |      |           |
| $f_{MAX}$    | Maximum Frequency <sup>(1)</sup>   | 3                    | —    | —    | 3                    | —    | —    | 3                    | —    | —    | GHz  |           |
| $t_{PD}$     | Propagation Delay (Diff.)          | 250                  | 350  | 400  | 250                  | 350  | 400  | 250                  | 350  | 400  | ps   |           |
| $t_{SKEW}$   | Within-Device Skew                 | —                    | 20   | 25   | —                    | 20   | 25   | —                    | 20   | 25   | ps   | (2)       |
|              | Part-to-Part Skew                  | —                    | 85   | 150  | —                    | 85   | 150  | —                    | 85   | 150  | ps   | (3)       |
| $t_{JITTER}$ | Cycle-to-Cycle Jitter (rms)        | —                    | 0.2  | < 1  | —                    | 0.2  | < 1  | —                    | 0.2  | < 1  | ps   |           |
| $V_{PP}$     | Minimum Input Swing <sup>(4)</sup> | 150                  | 800  | 1200 | 150                  | 800  | 1200 | 150                  | 800  | 1200 | mV   |           |
| $t_r, t_f$   | Output Rise/Fall Time (20% to 80%) | 100                  | 170  | 250  | 100                  | 170  | 250  | 100                  | 170  | 250  | ps   |           |

**Note 1.** Measured with 750mV clock signal, 50% duty cycle. All loading with a  $50\Omega$  to  $V_{CC} - 2.0V$ .**Note 2.** Input clock to any output (Q0 to Q9); Differential.**Note 3.** Measured for same transitions.**Note 4.** See "Timing Waveform."**TIMING WAVEFORM**

TYPICAL CHARACTERISTICS



## TERMINATION RECOMMENDATIONS

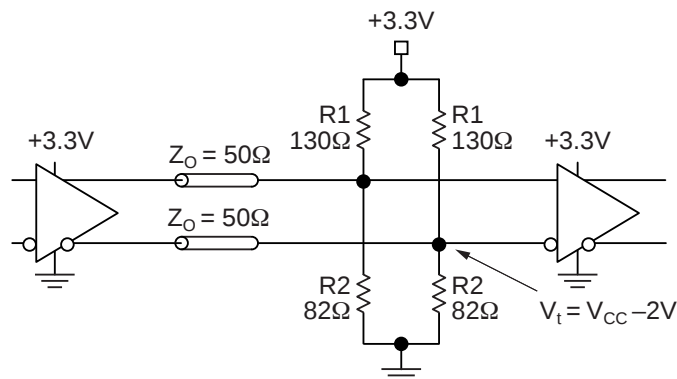


Figure 1. Parallel Termination-Thevenin Equivalent

**Note 1.** For +2.5V systems:  $R1 = 250\Omega$ ,  $R2 = 62.5\Omega$

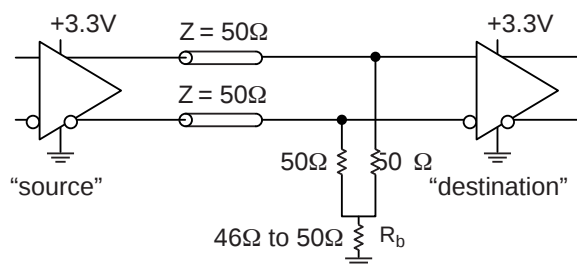


Figure 2. Three-Resistor "Y-Termination"

**Note 1.** Power-saving alternative to Thevenin termination.

**Note 2.** Place termination resistors as close to destination inputs as possible.

**Note 3.**  $R_b$  resistor sets the DC bias voltage, equal to  $V_t$ .

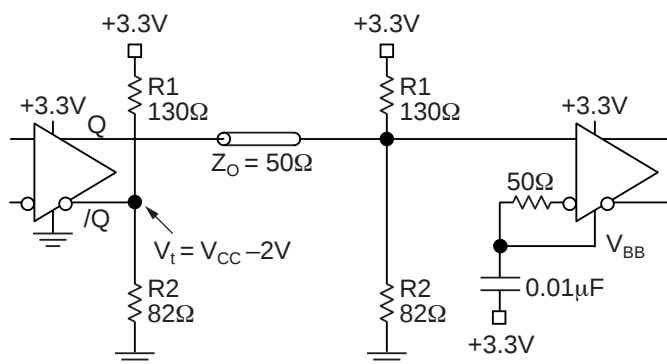


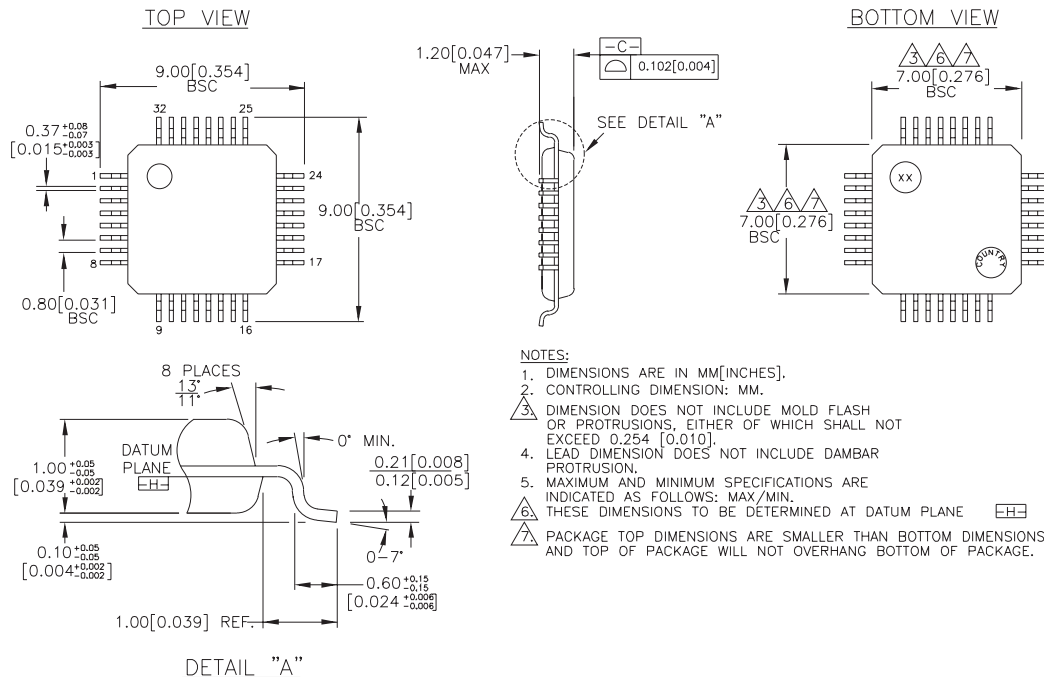
Figure 3. Terminating Unused I/O

**Note 1.** Unused output ( $I/Q$ ) must be terminated to balance the output.

**Note 2.** Micrel's differential I/O logic devices include a  $V_{BB}$  reference pin.

**Note 3.** Connect unused input through  $50\Omega$  to  $V_{BB}$ . Bypass with a  $0.01\mu F$  capacitor to  $V_{CC}$ , not GND.

**Note 4.** For +2.5V systems:  $R1 = 250\Omega$ ,  $R2 = 62.5\Omega$ .

**32-PIN THIN QUAD FLATPACK (T32-1)**

Rev. 01

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