2.5V/3.3V TWO INPUT, 1GHz LVTTL/CMOS-TO-LVPECL 1:4 FANOUT BUFFER/ TRANSLATOR WITH 2:1 INPUT MUX

Precision Edge® SY89834U

FEATURES

- Selects between two LVTTL/CMOS inputs and provides 4 LVPECL output copies
- Guaranteed AC performance over temperature and voltage:
  - DC-to >1.0GHz throughput
  - <500ps propagation delay (IN-to-Q)
  - < 20ps within-device skew
  - < 225ps rise/fall time
- Ultra-low jitter design:
  - < 1ps$_{RMS}$ cycle-to-cycle jitter
  - < 1ps$_{RMS}$ random jitter
  - < 10ps$_{PP}$ deterministic jitter
  - < 10ps$_{PP}$ total jitter (clock)
- Low voltage 2.5V and 3.3V supply operation
- 100K LVPECL outputs
- Industrial temperature range: –40°C to +85°C
- Includes a 2:1 MUX select input
- Accepts single-ended TTL/CMOS inputs and provides four LVPECL outputs
- Available in 16-pin (3mm × 3mm) MLF™ package

Precision Edge®

DESCRIPTION

The SY89834U is a high-speed, 1GHz LVTTL/CMOS-to-LVPECL fanout buffer/translator optimized for high-speed ultra-low skew applications. The input stage is designed to accept two single-ended LVTTL/CMOS compatible signals that feed into a 2:1 MUX. The selected input is translated and distributed as four differential 100K LVPECL outputs. Within device skew is guaranteed to be less than 20ps over supply voltage and temperature.

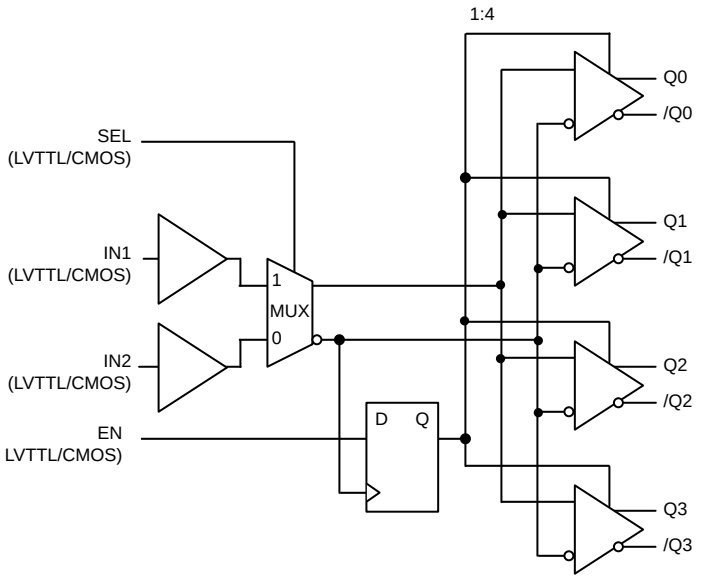
The single-ended input buffers accept TTL/CMOS logic levels. The internal threshold of the buffers is defined as $V_{CC}/2$.

The SY89834U is a part of Micrel's high-speed Precision Edge® family. For applications that require a different I/O combination, consult Micrel's website at: www.micrel.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

APPLICATIONS

- Processor clock distribution/translation
- SONET clock distribution/translation
- Fibre Channel clock distribution/translation
- Gigabit Ethernet clock distribution/translation
- Single-ended ASIC-to-differential communication IC signal translation

FUNCTIONAL BLOCK DIAGRAM



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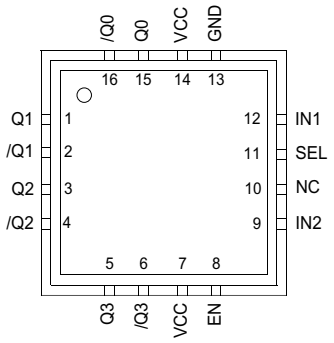
*Micro*LeadFrame and MLF are trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



16-Pin MLF™ (MLF-16)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89834UMI	MLF-16	Industrial	834U	Sn-Pb
SY89834UMITR[2]	MLF-16	Industrial	834U	Sn-Pb
SY89834UMG[3]	MLF-16	Industrial	834U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89834UMGTR[2, 3]	MLF-16	Industrial	834U with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
15, 16 1, 2, 3, 4, 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	Differential 100K LVPECL Outputs: These LVPECL outputs are the precision, low skew copies of the inputs. Please refer to the "Truth Table" section for details. Unused output pairs may be left open. Terminate wtih 50Ω to V_{CC}–2V. See "Output Termination Recommendations" section for more details.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
12, 9	IN1 IN2	Single-ended TTL/CMOS-compatible inputs to the device. These inputs are internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. The input threshold is V_{CC}/2.
10	NC	No connect. Not internally connected.
11	SEL	TTL/CMOS Compatible Select Input for signals IN1 and IN2. The input threshold is V_{CC}/2. HIGH at the SEL input selects signal IN1. LOW at the SEL input selects signal IN2. SEL includes a 25kΩ pull-up resistor. The default state is HIGH when left floating.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors and place as close to each VCC pin as possible.

TRUTH TABLE

IN1	IN2	EN	SEL	Q0–Q3	/Q0–Q3
0	X	1	1	0	1
1	X	1	1	1	0
X	0	1	0	0	1
X	1	1	0	1	0
X	X	0	X	0[1]	0[1]

Note:

1. On next negative transition of the input signal (IN).

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.3V
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current (IN1, IN2) ..... ±50mA
Lead Temperature (Soldering, 20sec.), ... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage Range ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
  MLF™ (θ_{JA})
    Still-Air ..... 60°C/W
  MLF™ (ψ_{JB})
    Junction-to-Board ..... 32°C/W

DC ELECTRICAL CHARACTERISTICS[4]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375 3.0		2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}.		50	75	mA

LVTTL/CMOS INPUTS DC ELECTRICAL CHARACTERISTICS[4]

V_{CC} = 2.5V ±5% or V_{CC} = 3.3V ±10%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	I_{IH} @ V_{IN} = 2.7V	–125		30	µA
I_{IL}	Input LOW Current		–125			µA

(100KEP) LVPECL OUTPUTS DC ELECTRICAL CHARACTERISTICS[4]

V_{CC} = 2.5V ±5% or V_{CC} = 3.3V ±10% , R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC}–1.145	V_{CC}–1.020	V_{CC}–0.895	V
V_{OL}	Output LOW Voltage		V_{CC}–1.945	V_{CC}–1.820	V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing	See Figures 2a.	550	800	1050	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figures 2b.	1100	1600	2100	mV

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still-air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[5]

V_{CC} = 2.5V ±5% or V_{CC} = 3.3V ±10% , R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	Input t_r / t_f ≥ 350ps	1.0			GHz
t_{pd}	Propagation Delay IN-to-Q	Note 6	200	320	500	ps
t_{SW}	Switchover Time SEL-to-Q		200	320	500	ps
t_{SKEW}	Within-Device Skew	Note 7		5	20	ps
	Part-to-Part Skew	Note 8			300	ps
t_{JITTER}	Data Random Jitter (RJ) Deterministic Jitter (DJ)	 Note 9 Note 10			 1 10	 ps_{RMS} ps_{PP}
	Clock Cycle-to-Cycle Jitter Total Jitter (TJ)	 Note 11 Note 12			 1 10	 ps_{RMS} ps_{PP}
DC	Duty Cycle	Input t_r/t_f ≥ 350ps, Note 13	45	50	55	%
t_S	Set-Up Time EN to IN1, IN	Note 14 and Note 15	300			ps
t_H	Hold Time EN to IN1, IN	Note 14 and Note 15	500			ps
t_r, t_f	Output Rise/Fall Times (20% to 80%)		70	140	225	ps

Notes:

5. High-frequency AC parameters are guaranteed by design and characterization.
6. V_{IH} = 2.0V, V_{IL} = 0.8V, 50% duty cycle. Delay measured at 100MHz from the crossing of the input signal with V_{CC}/2 as the crossing of the differential output signal. See Figure 1.
7. Within device skew is measured between two different outputs under identical input transitions.
8. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
9. Random jitter is measured with a K28.7 pattern, measured at ≤f_{MAX}.
10. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}–1 PRBS pattern.
11. Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n – T_{n+1}$, where T is the time between rising edges of the output signal.
12. Total jitter definition: with an ideal clock input frequency of ≤ f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
13. If t_r/t_f is less than 350ps, the duty cycle distortion will increase beyond the duty cycle limits.
14. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications set-up and hold times do not apply.
15. See “Timing Diagrams,” Figure 1a.

TIMING DIAGRAMS

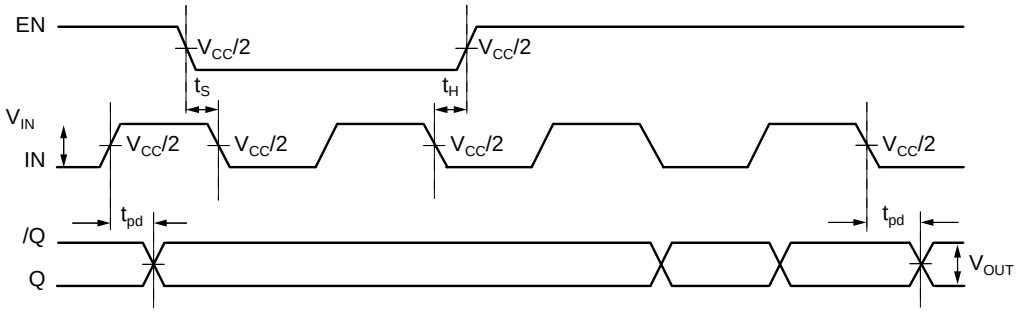


Figure 1a. Timing Diagram (EN, IN1, IN2)

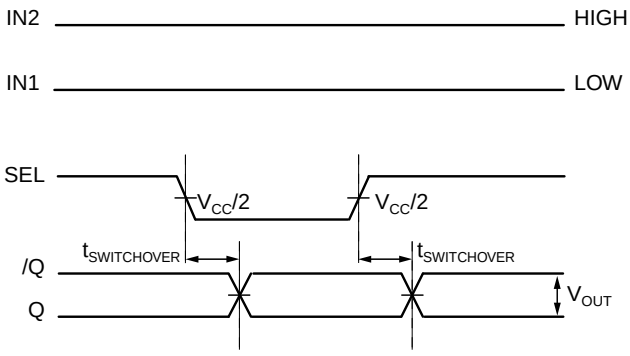


Figure 1b. Timing Diagram (SEL)

SINGLE-ENDED AND DIFFERENTIAL SWINGS

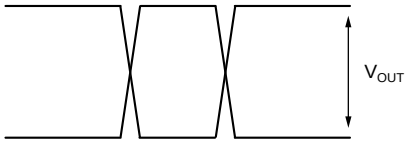


Figure 2a. Single-Ended Swing

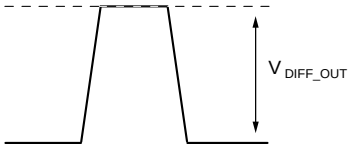
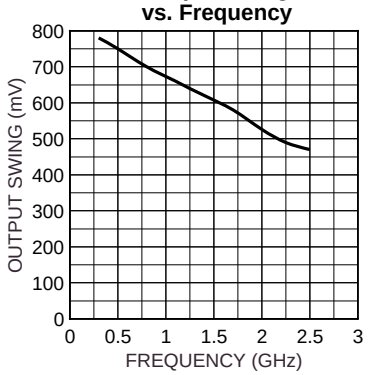


Figure 2b. Differential Swing

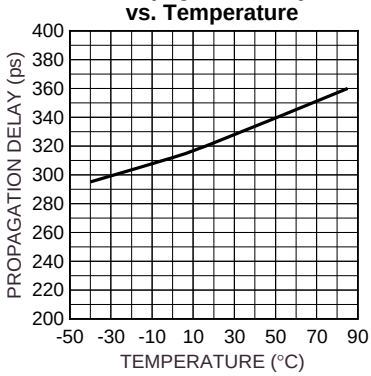
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, R_L = 50Ω to V_{CC}–2V; T_A = 25°C, unless otherwise stated.

Output Swing vs. Frequency



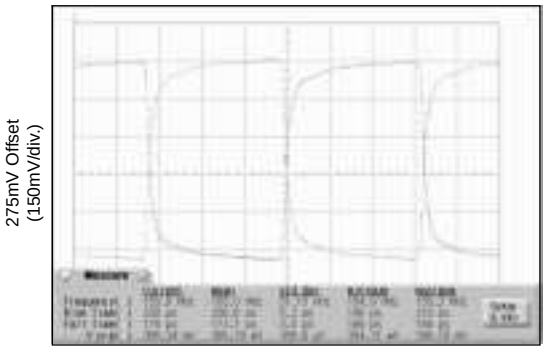
Propagation Delay vs. Temperature



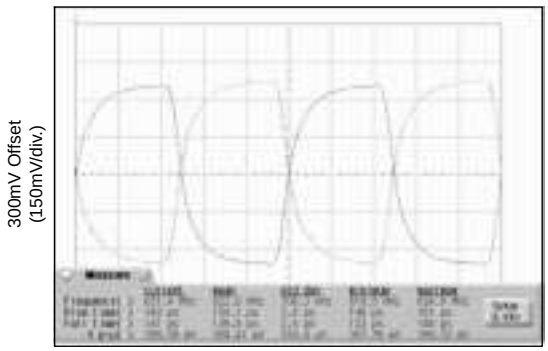
FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, R_L = 50Ω to V_{CC}–2V, T_A = 25°C, unless otherwise stated.

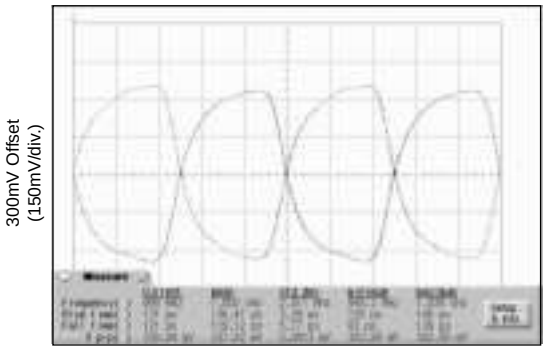
155MHz Output



622MHz Output



1GHz Output



DIFFERENTIAL INPUT

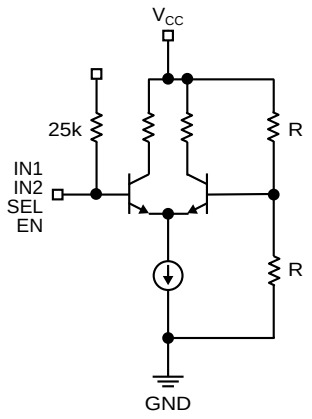


Figure 3. Simplified TTL/CMOS Input Buffer

RELATED PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89830U	2.5V/3.3V/5V 2.5GHz 1:4 PECL/ECL Clock Driver with 2:1 Differential Input Mux	http://www.micrel.com/product-info/products/sy89830u.shtml
SY89831U	Ultra-Precision 1:4 LVPECL Fanout Buffer/ Translator with Internal Termination	http://www.micrel.com/product-info/products/sy89831u.shtml
SY89832U	2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/ Translator with Internal Termination	http://www.micrel.com/product-info/products/sy89832u.shtml
SY89833U	3.3V Ultra-Precision 1:4 LVDS Fanout Buffer/ Translator with Internal Termination	http://www.micrel.com/product-info/products/sy89833u.shtml
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	http://www.amkor.com/products/notes-papers/ MLF-appnote-0301.pdf
HBW Solutions	New Products + Termination App Note	http://www.micrel.com/product-info/as/solutions.shtml

TERMINATION RECOMMENDATIONS

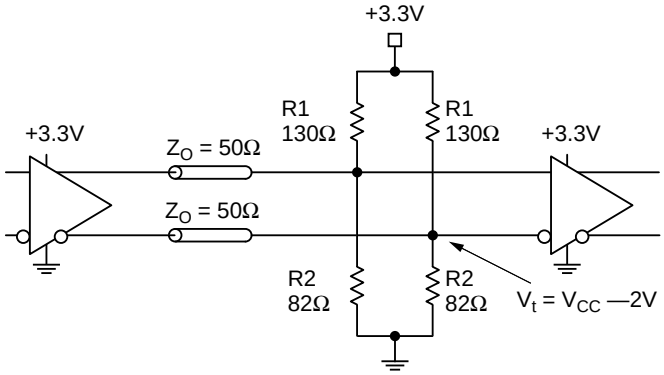


Figure 4a. Parallel Termination–Thevenin Equivalent

Note:

1. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω
   For +3.3V systems: R1 = 130Ω, R2 = 82Ω

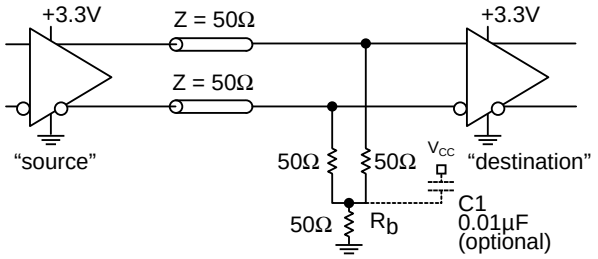


Figure 4b. Three-Resistor "Y–Termination"

Notes:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_t. For +3.3V systems R_b = 50Ω. For +2.5V systems R_b = 19Ω.

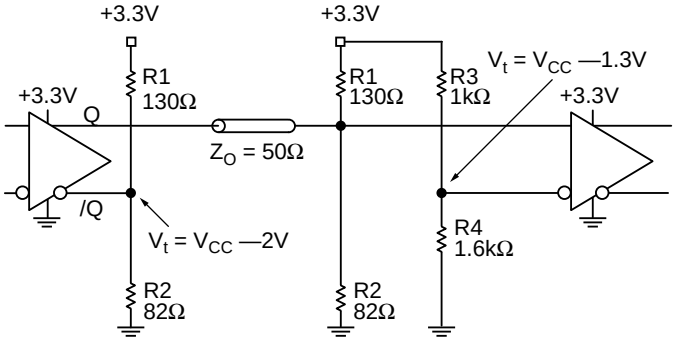
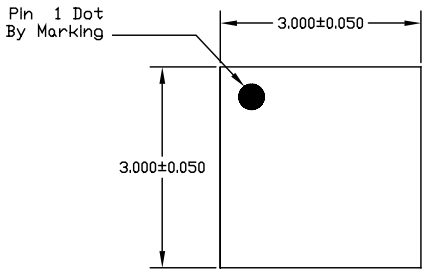


Figure 4c. Terminating Unused LVPECL I/O

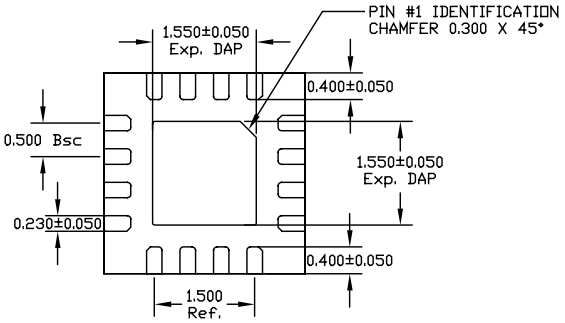
Notes:

1. Unused output (/Q) must be terminated to balance the output.
2. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.
2. Unused output pairs (Q and /Q) may be left floating.

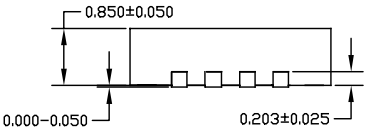
16 LEAD EPAD *Micro*LeadFrame™ (MLF-16)



TOP VIEW

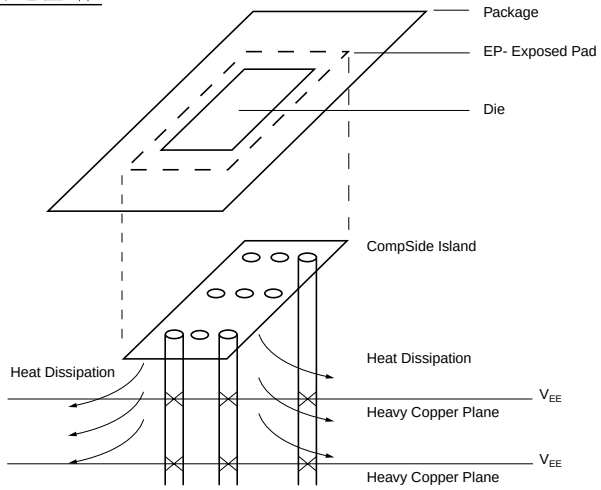


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB.)

Package Notes:

Note 1. Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
Note 2. Exposed pads must be soldered to a ground for proper thermal management.

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