MIC3263

Six-Channel WLED Driver for Backlighting Applications with Flicker-Free Dimming

General Description

The MIC3263 is a high-efficiency Pulse Width Modulation (PWM) boost switching regulator that is optimized for constant-current WLED driver backlighting applications. The MIC3263 drives six channels of up to ten WLEDs per channel. Each channel is matched in current to within ±3% for constant brightness across the screen and can be programmed from 15mA to 30mA.

The MIC3263 provides a very flexible dimming control scheme with better accuracy and noise immunity. The dimming frequency can be set to any value between 100Hz and 20kHz by an external resistor. The dimming ratio is determined by the duty cycle of a dimming ratio control input signal and can be set to one of 16 levels with a minimum ratio of 1%.The LED dimming current is set by an external resistor to allow programming of LED current between 15mA and 30mA.

The dimming ratio of the MIC3263 is fixed to 16 log levels to better match the sensitivity of the human eye. Each of the dimming levels has hysteresis to avoid skipping between levels and allow for high noise immunity.

The MIC3263 has a programmable PWM switching frequency from 400 KHz to 1.8 MHz to allow small inductor sizes. The 6V to 40V wide input voltage range of MIC3263 allows direct operation from 6V or high cell count Li-Ion batteries commonly found in notebook computers.

The MIC3263 is available in a low-profile 24-pin 4mm x 4mm MLF® package and has a junction temperature range of –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

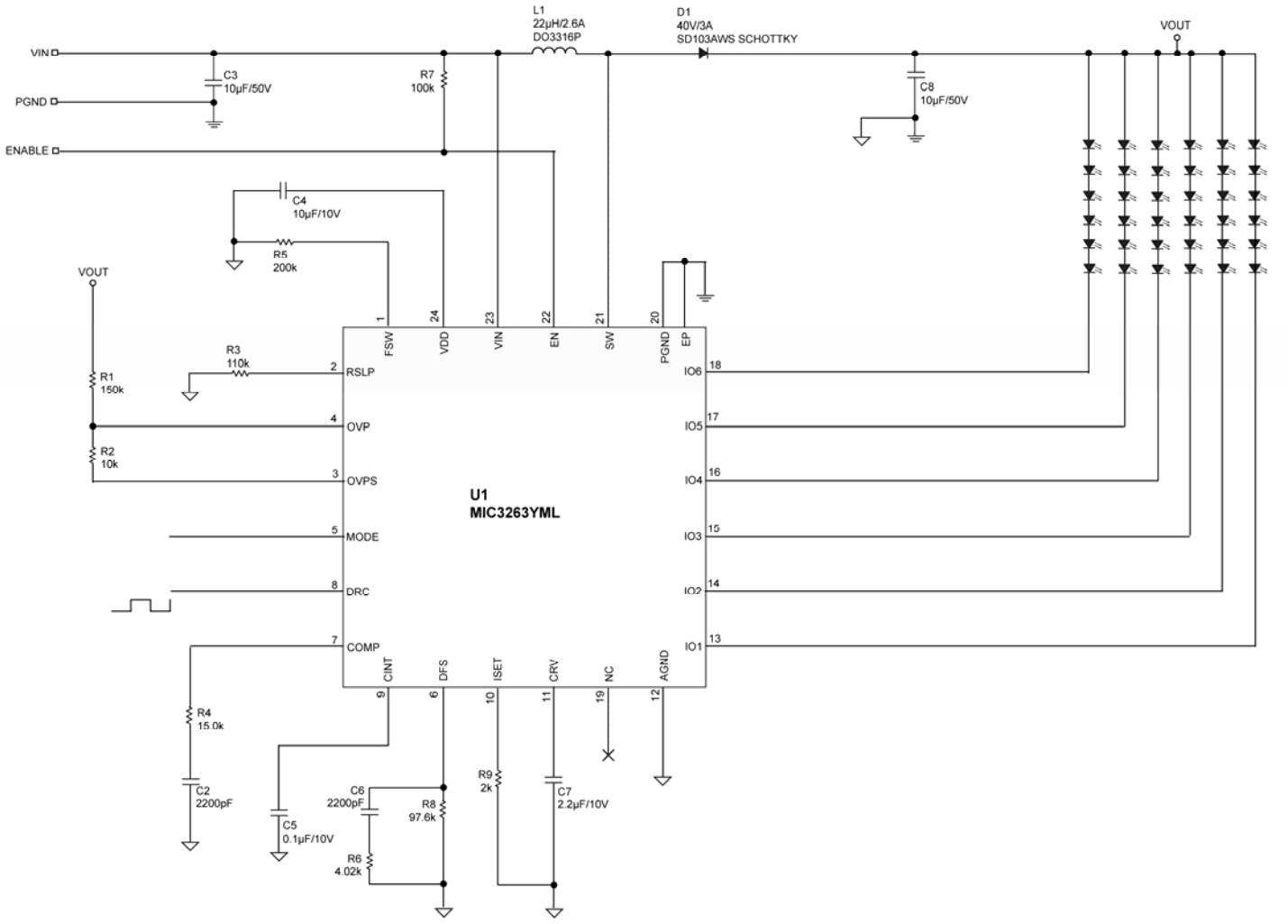
- 6V to 40V wide input voltage range
- Drives 6 channels of up to 10 white LEDs
- Programmable WLED current from 15mA to 30mA
- Highly reliable operation with open and short LEDs
- Accurate 16 dimming log levels sets the dimming ratio from 1% to 100%
- Flicker-Free Dimming filters the jitter from the dimming control input signal and eliminates dimming flicker
- Allows external dimming control
- Accurate LED channel current matching ±3%
- Accurate initial LED current setting ±2%
- Programmable switching frequency from 400kHz to 1.8MHz
- High efficiency up to 90%
- Low (<40µA) shutdown current over temperature
- Over temperature protection
- Programmable over-voltage protection
- –40°C to +125°C junction temperature range
- Available in 24-pin 4mm x 4mm MLF® package

Applications

- White LED driver for backlighting
- Notebooks
- LCD Panels and Monitors
- Multimedia players
- Navigation equipment
- Gaming systems
- Video poker
- Slot machines

MLF is a registered trademark of Micrel, Inc.

Typical Application



MIC3263 Typical Application Schematic

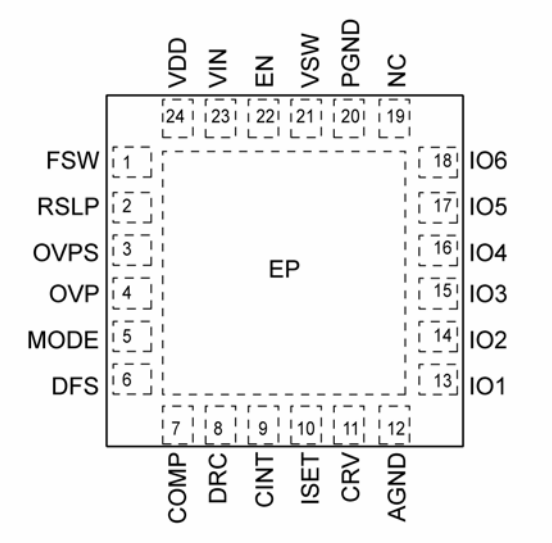
Ordering Information

Part Number	Junction Temperature Range[1]	Package	Lead Finish
MIC3263YML	–40° to +125°C	24-Pin 4mm x 4mm MLF®	Pb-Free

Note:

1. Other Voltage available. Contact Micrel for detail

Pin Configuration



24-Pin 4mm x 4mm MLF®

Pin Description

Pin Number	Pin Name	Pin Function
1	FSW	Booster Switching Frequency: Connect a resistor-to-GND to set the switching frequency from 400kHz to 1.8MHz.
2	RSLP	Slope Compensation Adjustment Resistor.
3	OVPS	OVP and FB voltage divider virtual ground.
4	OVP	Overvoltage Protection Input. This is also the FB voltage for the error amp in the Boost stage.
5	MODE	Select a dimming frequency range: 0V for 100Hz to 2kHz and V_{DD} for 1.5kHz to 20kHz. If DFS is connected to V_{DD}, MODE pin is used for an external dimming pulse input.
6	DFS	Set a dimming frequency from 100Hz to 20kHz through an external resistor and MODE. Requires a series RC for stability. If DFS is connected to V_{DD}, an external dimming pulse can be applied to the MODE pin.
7	COMP	Loop Compensation connect R and C-to-GND.
8	DRC	Dimming Ratio Control Pulse: Its duty cycle is converted to one of 16 dimming levels. The duty-cycle difference between two adjacent levels is ±6.25%. And about 2% duty-cycle hysteresis exists between two adjacent levels to eliminate dimming flicker. DRC can be from 100Hz to 40kHz.
9	CINT	Integration Cap: Use a 0.01µF for 2kHz to 20kHz and 0.1µF for 100Hz ─ 2kHz.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
10	ISET	LED Dimming Current Set: Connect a resistor-to-GND to set the dimming current from 15mA to 30mA. Use 2kΩ for 30mA, and 3kΩ for 20mA.
11	CRV	Capacitor reference voltage: Connect a 2.2µF capacitor-to-GND.
12	AGND	Analog signal Ground.
13, 14, 15, 16, 17, 18	IO1 ─ IO6	LED Channel Current Sinker: Connect the cathode of each channel of LEDs to one current sinker.
19	NC	No Connect.
20	PGND	Power Ground.
21	VSW	Switch Node: Internal power NPN collector.
22	EN	Enable Pin: Connect HIGH or LOW; do not float.
23	VIN	Supply: 6V to 40V.
24	VDD	Output of internal LDO: Connect a 10µF capacitor-to-GND.
	EP	Connect to PGND

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}), Enable (V_{EN}) ..... +42V
Switch Voltage (V_{SW}) ..... –0.3V to +42V
Regulated Voltage (V_{DD}) ..... –0.3V to +6V
Over-Voltage Protection (V_{OVP}) ..... –0.3V to +42V
Switch Voltage (V_{OVPS}) ..... –0.3V to +42V
DFS Voltage (V_{DFS}) ..... –0.3V to (V_{DD} + 0.3V)
RSLP (V_{RSLP}) ..... –0.3V to (V_{DD} + 0.3V)
MODE Voltage (V_{MODE}) ..... –0.3V to (V_{DD} + 0.3V)
FSW Voltage (V_{FSW}) ..... –0.3V to (V_{DD} + 0.3V)
DRC Voltage (V_{DRC}) ..... –0.3V to (V_{DD} + 0.3V)
CRV Voltage (V_{CRV}) ..... –0.3V to (V_{DD} + 0.3V)
CINT Voltage (V_{CINT}) ..... –0.3V to (V_{DD} + 0.3V)
ISET Voltage (V_{ISET}) ..... –0.3V to (V_{DD} + 0.3V)
Comp Voltage (V_{COMP}) ..... –0.3V to (V_{DD} + 0.3V)
IO1–IO6 Voltage ($V_{IO1-IO6}$) ..... –0.3V to +42V
AGND to PGND ..... –0.3V to +0.3V
Lead Temperature (soldering, 10 ─ 20s) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C
ESD Rating[3] 1.5kV

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +6V to +40V
Enable (V_{EN}) ..... 0 to +40V
MODE (V_{MODE}) ..... 0 to +5.5V
DFS (V_{DFS}) ..... 0 to +5.5V
DRC (V_{DRC}) ..... 0 to +5.5V
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
24-Pin MLF® (θ_{JA}) ..... 43°C/W

Electrical Characteristics[4]

V_{IN} = 12V; L = 22µH, C_{OUT} =10µF, T_A = 25°C, **BOLD** values indicate –40°C≤ T_J ≤ +125°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Supply Voltage Range	30mA 8 LEDs/Channel, All six Channels	**8**		**40**	V
V_{IN}	Supply Voltage Range	30mA 6 LEDs/Channel, All six Channels	**6**		**40**	V
I_{VIN}	Quiescent Current	Not Switching, V_{OVP} = 4V		6.5	10	mA
V_{DDREG}	VDD Regulation	V_{IN} = 6V to 40V, I_{DD} = 0mA to 6mA	4.5	5	5.5	
I_{SD}	Shutdown Current (DC Pin Low)	V_{EN} = 0V		6.5	20	µA
Current Control						
IO1 ─ IO6	Minimum IO (1–6) Voltage for operation to Sink 30mA	Voltage on IO (1–6) if Only One Channel is Used and I_{SET} = 30mA		1.2		V
V_{OS}	Maximum Output Voltage Overshoot when Current Sources are OFF in PWM Dim Mode	22µH, 10µF		3		%
$I_{LEDMATCH}$	Channel Current Matching	I_{LED} = 30mA and Dimming Ratio = 100% V_{IO} = 1.2V on All Channels	–**3**	0	+**3**	%
I_{LEDSET}	Initial Current Setting Accuracy	R_{SET} = 2k I_{LED} = 30mA	–2 **–3**	0	+2 **+3**	%
F_{DIMR}	PWM Dimming Frequency Adjust Range	MODE = 0V, R_{DFS} = 400kΩ, Frequency = 100Hz MODE = 0V, R_{DFS} = 32kΩ, Frequency = 1.2kHz MODE = V_{DD}, R_{DFS} = 400kΩ, Frequency = 1.6kHz MODE = V_{DD}, R_{DFS} = 32kΩ, Frequency = 20kHz	0.1		20	kHz

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Specification for packaged product only.

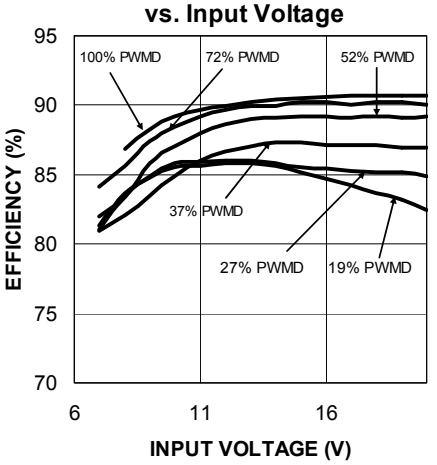
Electrical Characteristics[4] (Continued)

V_{IN} = 12V; L = 22µH, C_{OUT} =10µF, T_A = 25°C, **BOLD** values indicate –40°C≤ T_A ≤ +125°C, unless noted.

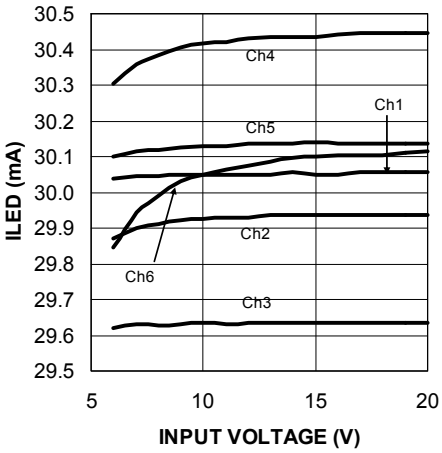
Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{DIMA}	PWM Dimming Frequency Accuracy	F_{DIM} = 100Hz to 2kHz; MODE = 0 F_{DIM} = 1.6kHz to 20kHz; MODE = V_{DD}	–20 –20	0 0	+20 +20	%
F_{DRC}	DRC Input Range		0.1		40	kHz
V_{PWM}	DRC Pin Thresholds	Turn on	1.3			V
		Turn off			0.4	
V_{EN}	EN Pin Thresholds	Turn on	1.3			V
		Turn off			0.4	
I_{EN}	Enable Pin Current			40	60	µA
Boost Converter						
D_{MAX}	Maximum Duty Cycle		90			%
I_{SW}	Switch Current Limit	V_{IN} = 6V to 20V, Guaranteed by Design	1.6	2.4		A
V_{SW}	Equivalent Switch $V_{CE(ON)}$	V_{IN} = 12V, I_{SW} = 1.0A		0.3		V
I_{SW}	Switch Leakage Current	V_{IN} = 0V, V_{IN} = 40V		0.01	20	µA
N	Efficiency	V_{IN} = 12V, Load = 6 Channels of 8 LEDs at 20mA with 3.6V per LED, Frequency = 400kHz		90		%
F_{SW}	Oscillator Frequency Range	Frequency Setting Range	0.4	1.2	1.8	MHz
f_{SW}	Oscillator Frequency	R_{FSW} = 160kΩ	0.96	1.2	1.44	MHz
V_{OVP}	Overvoltage Protection	Comparators OVP Pin to 2.36V		2.36		V
T_{SD}	Thermal Shutdown	Temperature Rising		160		°C
		Hysteresis		20		

Typical Characteristics

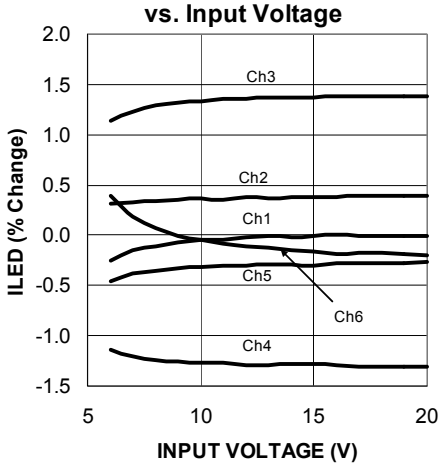
Dimming Efficiency vs. Input Voltage



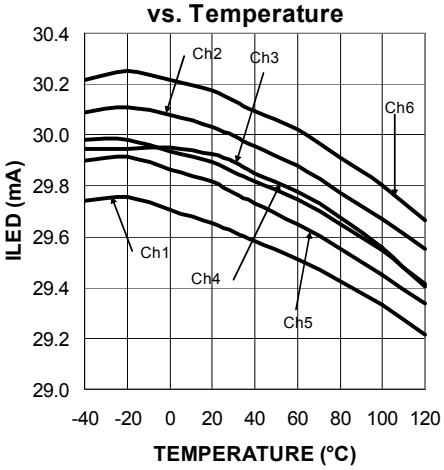
ILEDs vs. Input Voltage



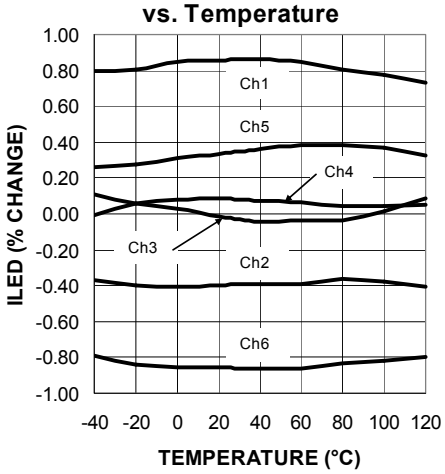
% Change in ILEDs vs. Input Voltage



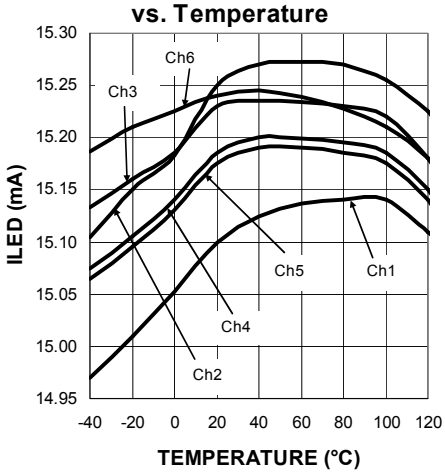
ILED @30mA vs. Temperature



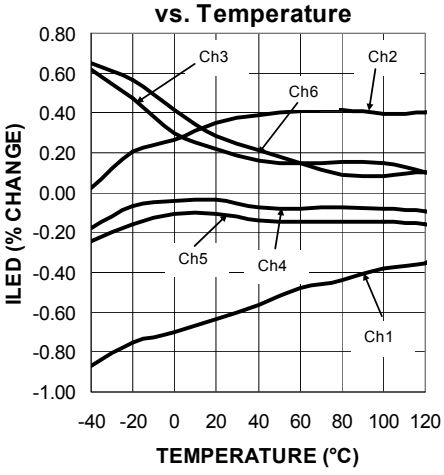
% Change in ILED@30mA vs. Temperature



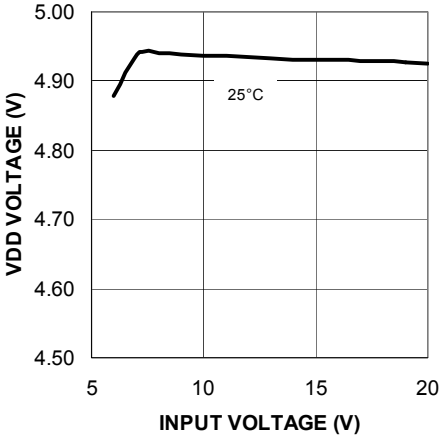
ILED @15mA vs. Temperature



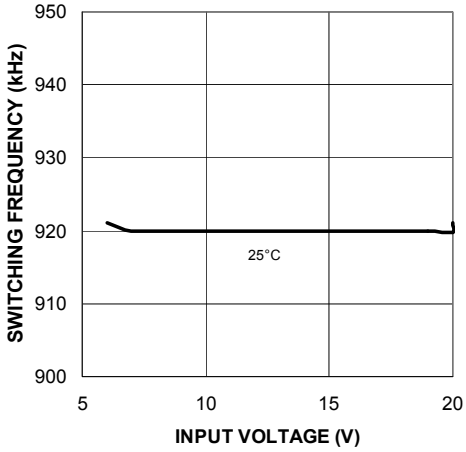
% Change in ILED @15mA vs. Temperature



VDD Voltage vs. Input Voltage

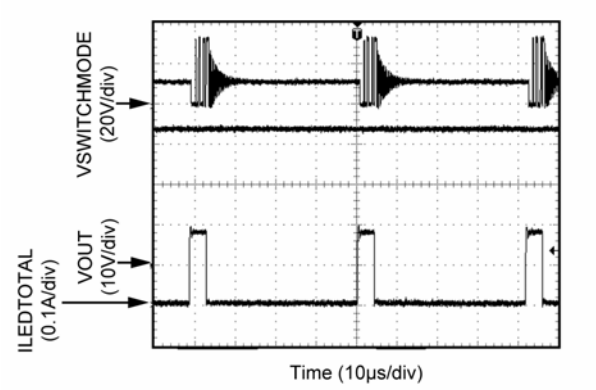


Switching Frequency vs. Input Voltage

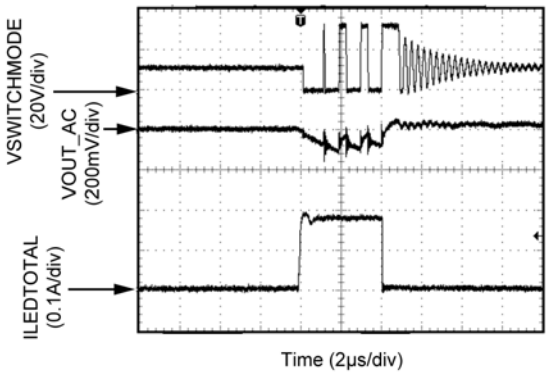


Functional Characteristics

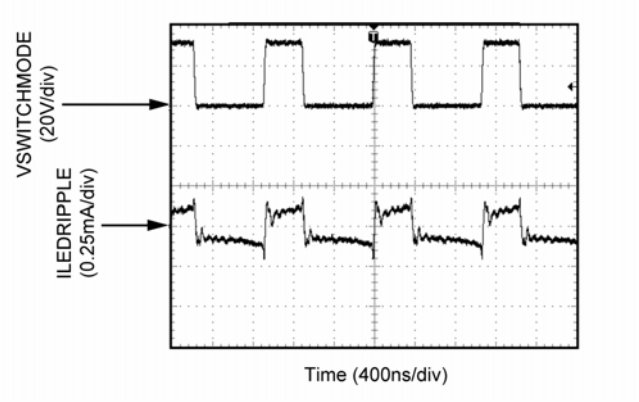
V_{OUT}, V_{SW}, I_{LED} at 10% Dimming



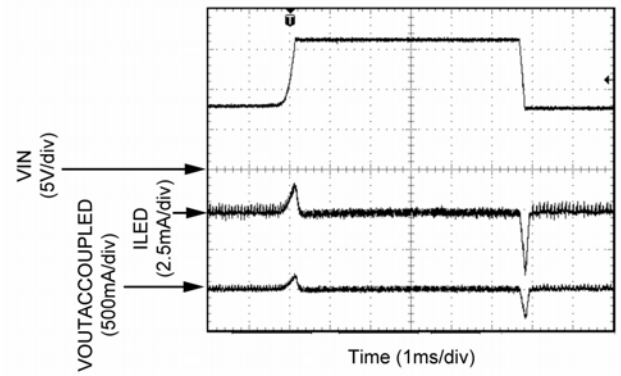
Dimming Transient Response



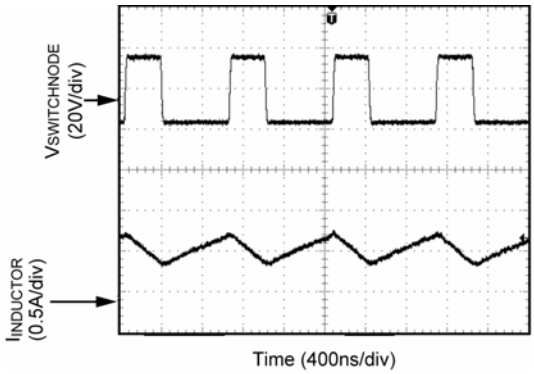
LED Ripple Current



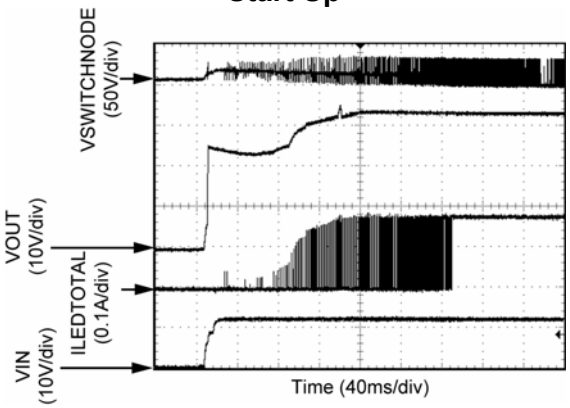
Line Transient Response



Switching Waveform

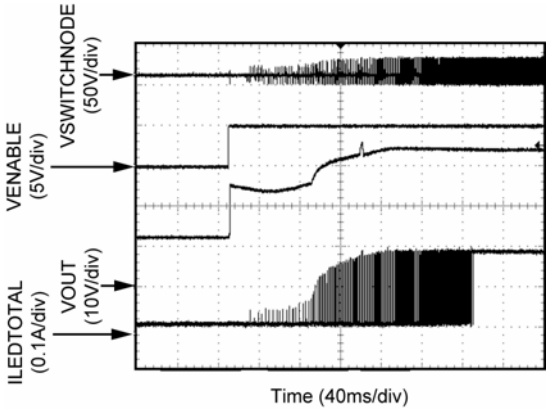


Start Up

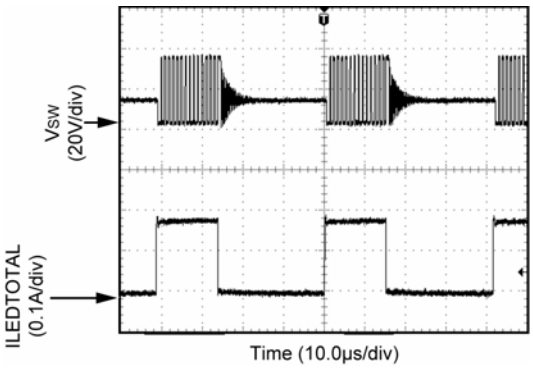


Functional Characteristics (Continued)

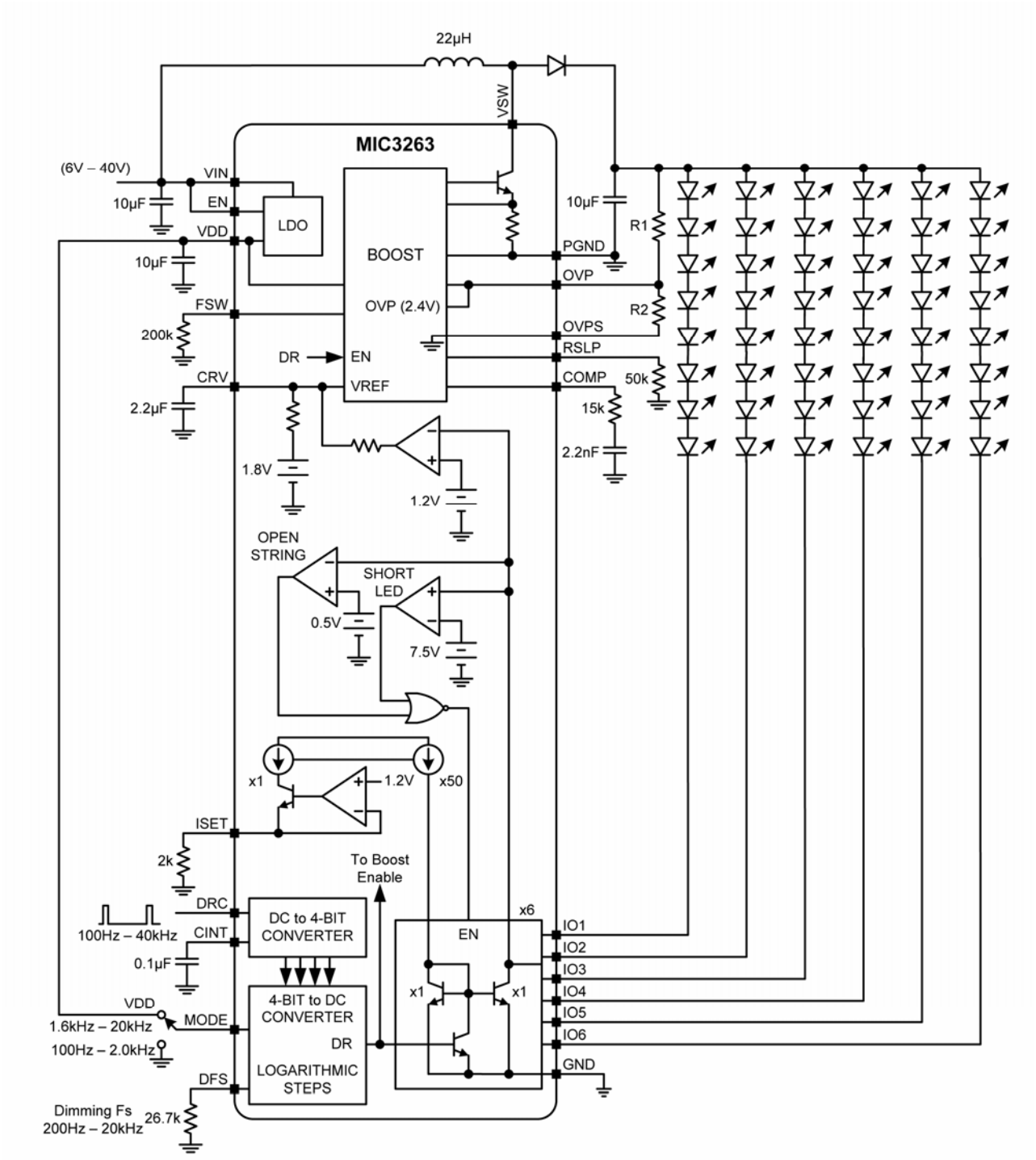
ENABLE Start Up



PWM Dimming



Functional Diagram



Functional Description

The MIC3263 is a six-channel LED driver. A constant output current converter is the preferred method for driving LEDs. The MIC3263 is specifically designed to operate as a constant-current LED driver to keep the current in all six channels constant. PWM dimming is employed in each channel. Each channel of LED current is individually and tightly regulated during each Duty Ratios (DR) on-time. During the DR off-time the LED current is turned off. The duty cycle of the DR pulse determines the brightness of the LEDs. The MIC3263 is designed to operate as a boost controller in which the output voltage is higher than the input voltage. This configuration allows for the design of multiple LEDs in series to help maintain color and brightness. During each DR pulse off-time the boost converter is turned off (not switching). The boost converter is on (switching) during each DR pulse on-time.

The MIC3263 has a very-wide input voltage range of 6V and 40V to help accommodate for a diverse range of input voltage applications. In addition, the LED current can be programmed through the use of an external resistor (R_{ISET}). This provides design flexibility in adjusting the current for a particular application. The MIC3263 can control the brightness of the LEDs via its PWM dimming capability. Applying a PWM dimming signal (up to 40kHz) to the DRC pin allows for control of the brightness of the LED. It has a boost stage that boosts the V_{IN} to a high enough voltage to forward bias the LED channels. The MIC3263 is a constant current controller. The controller keeps the current in each of the six channels at a constant value. Each channel has an independent current regulator in series with each LED channel. The current in each channel is within 3% of the others.

The MIC3263 uses three main control loops (Figure 1 control loops):

1) Current Amp loop (Fastest)
2) Booster loop (Fast)
3) Capacitor Reference Voltage (CRV) loop (Slow)

The current Amplifier Loop is faster than the Boost Loop and CRV Loop. CRV is the reference voltage for the boost error amp.

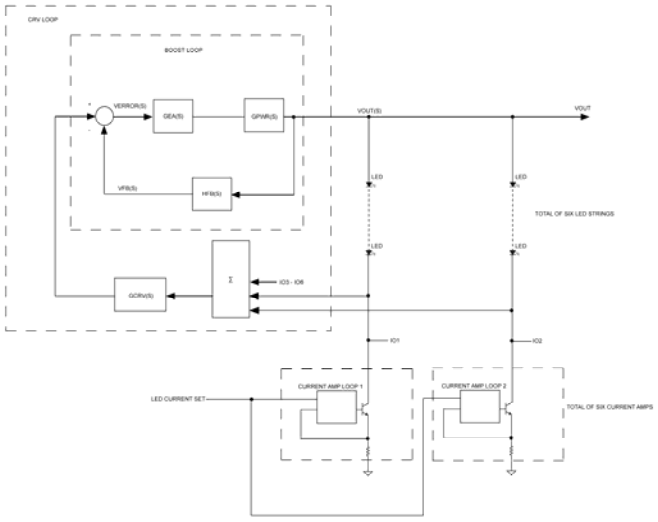


Figure 1. Constant-Current Control Loops

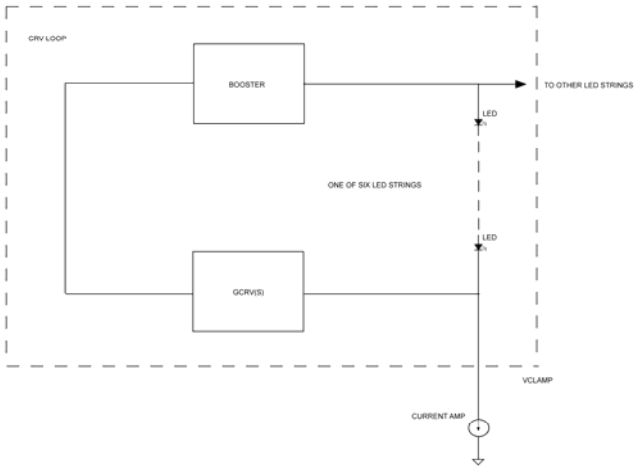


Figure 2. Simplified Control Loop

The objective of these loops is to keep the LED current constant. The boost output voltage V_{OUT} will vary when CRV changes. V_{OUT} will be what it needs to be to keep ILEDs constant. The current amp loop is so fast the other loops can be viewed as static DC values. On a pulse to pulse basis the boost loop is fast enough that CRV is a constant value.

The goal of the CRV loop is to keep the collector's voltage V(IO1–IO6) at or about 1.2V, thereby keeping the bipolar transistor in the linear region and also keep the power loss across the bipolar as low as possible. Keeping the bipolar in the linear region allows the current amp loop to be able to regulate the LED current.

V(IO) Too High

If the collector voltage V(IO1–IO6) is greater than 1.2V, then the CRV loop will slowly discharge (lower the voltage) the CRV capacitor. Since the CRV capacitor is used as the reference voltage for the boost error amp the boost voltage (V_{OUT}) will decrease. With lower V_{OUT}, V(IO) also decreases. Discharging of CRV continues until V(IO) is 1.2V.

V(IO) Too Low

If the collector voltage V(IO1-IO6) is less than 1.2V the CRV loop will slowly charge (increase the voltage) the CRV. Since CRV is used as the reference voltage for the boost converter's error amp the boost voltage (V_{OUT}) will increase. With higher V_{OUT}, V(IO) also increases. Charging of CRV continues until V(IO) is about 1.2V.

These control loops operate as described above during DR high pulses. When DR is low the booster is off and the **last state of the CRV charge or discharge will continue** until the next DR pulse. If the external PWM Dimming pulse (DRC) is removed, the internal dimming pulse (DR) will continue dimming at the same dimming level before the signal at DRC was removed and the CRV loop will keep operating normally. If external PWM DIM is 0% then charge/discharge states will discontinue and CRV will no longer be charged or discharged. CRV will slowly discharge through the circuitry connected to it

Boost Controller Operation

The MIC3263 uses a peak current-mode boost controller in its boost stage. The boost converter is a pulse width modulation (PWM) controller and operates thus. A flip-flop (FF) is set on the leading edge of the clock cycle. When the FF is set a gate driver drives the power bipolar switch on. Current flows from V_{IN} through the inductor (L) and through the internal power switch and current sense resistor-to-PGND. The voltage across the current sense resistor is added to a slope compensation ramp (needed for stability). The sum of the current-sense voltage and the slope compensation voltages (V_{CS}) is fed into the positive terminal of the PWM comparator. The other input to the PWM comparator is the error amp output (called V_{EA}). The error amp's negative input is the feedback voltage (V_{OVP}). The OVP pin is used as the voltage feedback to the error amplifier. In this way the output voltage is regulated. If V_{OVP} drops, V_{EA} increases and therefore the power switch remains on longer so that V_{CS} can increase to the level of V_{EA}. The reverse occurs when V_{OVP} increases.

The output voltage is always higher than the input voltage. The external CRV (see C7 in Typical Application illustration) is used as the reference voltage to the boost error amp.

The boost regulated output voltage is:

Equation 1

$$V_{OUT} = CRV \times \frac{(R1 + R2)}{R2}$$

The MIC3263 is designed for a wide input voltage range, from 6V to 40V. As a peak current-mode controller, the MIC3263 provides the benefits of superior line transient response as well as an easier to design compensation.

MIC3263 provides several protection features, including:

- Current Limit (I_{LIMIT}) ─ Current sensing for over current and overload protection
- Over-Voltage Protection (OVP) ─ output over-voltage protection to prevent operation above a safe upper limit
- The boost stage is on (switching) during a high DR pulse and is off (not switching) when the DR pulse is low.

Application Information

At Start Up

At start up, a switch connects 1.8V to the CRV. The feedback resistor divider (R1 and R2) is calculated to achieve the approximate boost output voltage with a V_{CRV} of 1.8V.

Example:

- 8 LEDs at 3.5V each = 28V
- VIO = 1.2V
- V_{OUT} = 29.3V estimate
- Set R divider to: R1 =150k R2 = 9.88k

The CRV control loop will charge/discharge CRV until the correct boost voltage appears at the output.

Case 1

If 29.3V is too high to properly forward bias the LED channel at the ISET current level, then the current amp loop will decrease the drive to the bipolar transistor and V(IO) will increase and the CRV control loop will decrease CRV and the boost output voltage (V_{OUT}) will decrease.

Case 2

If 29.3V is not high enough to properly forward bias the LED channel at the ISET current level, the current amp loop will drive the bipolar transistor harder and V(IO) will drop and the CRV control loop will increase CRV and the boost output voltage (V_{OUT}) will increase.

Internal Dimming Control

In the internal dimming mode, the dimming is determined by the DFS and MODE pins. An external pulse is tied to the DRC pin. The duty cycle of the external pulse (pulse at DRC) is converted to one of 16 levels called Duty Ratios (DR) (see Table 2 for DR ratios). It is this internal pulse (DR) that is used to PWM dim the LEDs.

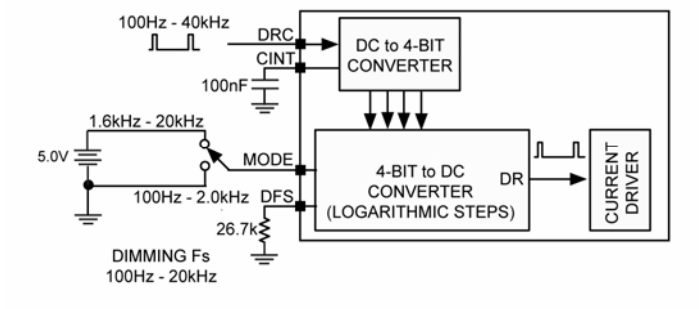


Figure 3. Internal Dimming Control

External Dimming Control

In external dimming mode, connect the DFS pin to V_{DD} and apply a PWM dimming pulse to the MODE pin. The external pulse directly controls the LED current drivers (see Figure 4).

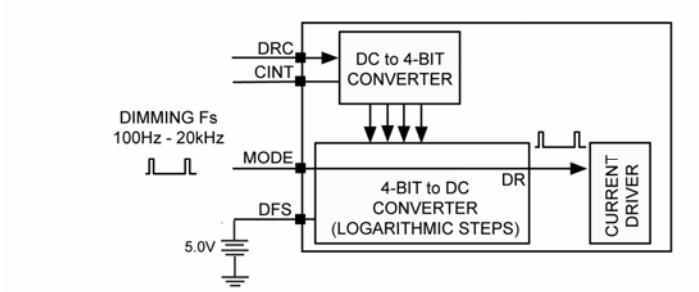


Figure 4. External Dimming Control

Faults

Open LED in Channel

If any LED in a channel fails open, the voltage on the collector of the current amp transistor (IO1-IO6) will go low. The circuitry that monitors the IO pins will detect less than 0.5V and turn off base drive to the transistor. A flip-flop latches the fault condition and a power down and power up sequence is required to reset that channel.

Without base drive to the transistor, the channel of LEDs will turn off and a high impedance will be present at the collector (IO). The other five channels will continue operating normally. This fault sequence is identical if up to three LED channels fail open. If four channels fail open or short, then the remaining two LED channels will stay on and no more faults will be detected.

Short LED in Channel

If any LED in a channel fails shorted, the voltage on collector of the current amp transistor (IO1–IO6) will go high in voltage. If the circuitry that monitors the current amp bipolar transistor detects more than 7.5V at the collector (IO), then the base drive to the transistor will turn off. A flip-flop latches the fault condition. A power-down and power-up sequence is required to reset that channel. A channel can tolerate a two LED difference before a fault is detected.

Without base drive to the transistor, the channel of LEDs will turn off and a high impedance is present at the collector (IO). The other five channels will continue operating normally. This fault sequence is identical if more than one LED channel fails open. If four channels fail open or short, then the remaining two LED channels will stay on and no more faults will be detected.

Shorted Cathode (or IO Short)

If the circuitry that monitors the current amp bipolar transistor detects less than 0.5V at the collector (IO), then the base drive to the transistor will turn off. A flip-flop latches the fault condition. A power-down and power-up sequence is required to reset that channel.

Without base drive to the transistor, the channel of LEDs will turn off and a high impedance is present at the collector (IO). The other five channels will continue operating normally. This fault sequence is identical if more than one LED channel fails open. If four channels fail open or short, then the remaining two LED channels will stay on and no more faults will be detected.

OVP

An open LED in a channel will not trigger an OVP. OVP monitors the boost output voltage. If an open occurs on the load (all channels open) an OVP fault will trigger an over-voltage condition. When the OVP triggers, it turns off the boost and starts an OVP cycle. If one, two, or three channels open, they will not trigger an OVP. Four open channels will trigger an OVP fault and will cycle on and off at about 2Hz as long as there are four open channels. If one of the LED channels is reconnected (not open), then operation returns to normal for those three channels that are reconnected with out having to go through a power on reset.

In the event of a load opening (four or more channels open) the following will occur:

1. VIO will drop below 1V
2. Charge pump will raise CRV during each DR pulse on-time
3. CRV will increase to 2.4V
4. When CRV reaches 2.4V the boost output maximum voltage will be; V_{OUT_MAX} = 2.4* (R2+R2)/R1.
5. Feedback V_{OVP} will reach 2.4V and the OVP comparator will trip and turn off the booster.
6. With the booster off, V_{OUT} and V_{OVP} will discharge. When feedback reduces to 1.7V the booster is turned back on.
7. The OVP circuit will switch 1.8V onto CRV
8. If the load is still open the cycle will continue.

Condition	Fault	Monitor	Result
1 LED Shorts	NO	IO > 1.2V	All Channels On
2 LEDs Short in Same Channel	NO	1.2 < IO < 7.5	All Channels On
More Than 2 LEDs Short in Same Channels	YES	IO > 7.5V	1 Channel Off; 5 Channels On
1 LED Opens in Channel 1	YES	IO < 0.5V	1 Channel Off; 5 Channels On
2 or 3 Channels Open LEDs	YES	IO < 0.5V	3 Channels Off; 3 Channels On
4 or More Channels Open	YES	IO < 0.5V	4 Channels Off; 2 Channels On
All Channels Open	YES	OVP Threshold Exceeded	OVP Triggered
V_{OUT} Shorted	YES	Current Limit Exceeded	Output Current is Limited

Table 1. Fault Summary

Power-On Sequence

V_{IN} needs to be present before PWM pulses are applied to the DRC pin. Some channels may not turn on if the power up sequence isn't followed. This is because the circuits that monitor the IO pins may see transients during the turn on-time and may interpret voltage spikes during turn on as a fault, preventing that channel from turning on. When a channel is off, its IO pin is at high impedance.

It is best to follow the sequence:

1. V_{IN}
2. PWM dimming at DRC
3. Enable high

Pin Descriptions

FSW

Sets the boost switching frequency. Connect a resistor from FSW to GND to set the switching frequency between 400kHz and 1.8MHz. Use the following equations to select R_{FSW}:

$$R_{FSW}\ (k\Omega) \approx 500 - 0.3 \times f_{SW}(kHz)$$

RSLP

The boost section is a peak current mode typology and needs slope compensation to eliminate sub-harmonic oscillation (see "Slope Compensation").

OVPS

This is a virtual ground of the resistor divider feedback network in the boost stage. At turn on, a switch connects this node-to-ground. When the part is disabled the switch will open and disconnects the feedback resistor network from ground. This eliminates current draw from V_{IN} by the boost resistor divider network.

OVP

This is the over-voltage protection monitor. Also this is the feedback signal that connects to the error amp input.

MODE

This selects the internal PWM dimming frequency range. When mode is low the PWM dimming frequency range is 100Hz to 2kHz. When mode is high the PWMD frequency range is 1.5kHz to 20kHz. Mode is high selects High Frequency (HF) mode; Mode is low selects Low Frequency (LF) mode.

DFS

DFS stands for Dimming Frequency Select. The dimming frequency of the LEDs is different than the input dimming frequency at the DRC input. The MIC3263 uses an internal dimming frequency. This internal dimming frequency is programmable by an external resistor to ground R_{DFS}.

For direct dimming control, connect DFS to V_{DD} and use the MODE pin for the input dimming pulse. This method by passes the internal dimming control and allows for dimming control by the external PWM pulse.

When using internal dimming the range is determined by the MODE pin and the actual frequency is determined by R_{DFS}. Connect a resistor to ground to select a dimming frequency.

Use the following equations to determine the value for R_{DFS}:

$$R_{DFS}(k\Omega) = -20 \times f_{DIM}(kHz) + 432 \text{ (HF Mode)}$$

$$R_{DFS}(k\Omega) = -335 \times f_{DIM}(kHz) + 433 \text{ (LF Mode)}$$

Example:

For a dimming frequency of 10kHz, use the HF Mode:

$$R_{DFS}(k\Omega) = -20 \times 10 + 432 = 232k\Omega \text{ in HF Mode}$$

For 1kHz, use LF Mode:

$$R_{DFS}(k\Omega) = -335 \times 1 + 433 = 98k\Omega \text{ in LF Mode}$$

Use the closest standard value.

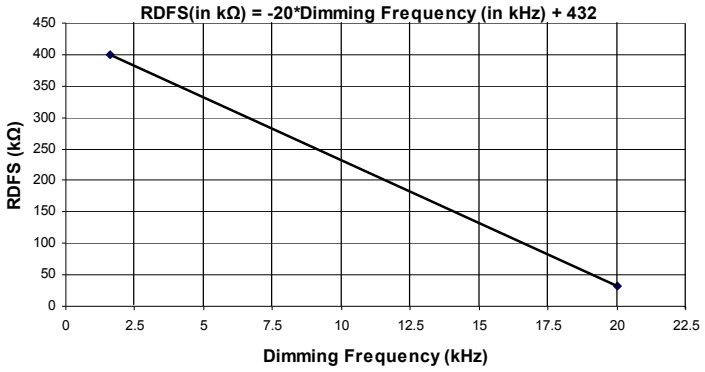


Figure 5. R_{DFS} vs. Dimming Frequency in HF Mode

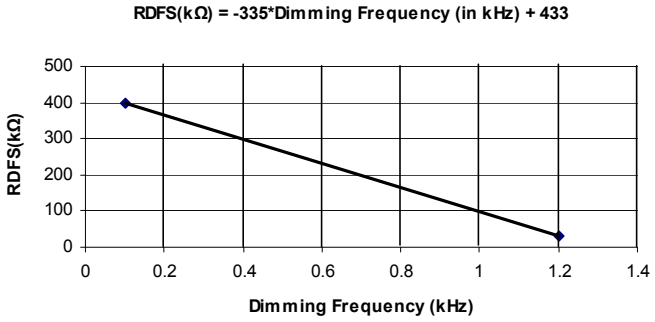


Figure 6. R_{DFS} vs. Dimming Frequency in LF Mode

The input frequency to the DRC pin can be 100Hz to 40kHz and the internal dimming frequency DR will be determined by R_{DFS}.

The duty cycle of the input frequency at DRC is converted according to Table 2 for the actual dimming duty cycle.

For direct dimming control, connect DFS to V_{DD} and use the MODE pin for the input dimming pulse. This method by passes the internal dimming control and allows for dimming control by the external PWM.

DFS Filter

In addition to the R_{DFS} resistor-to-ground at the DFS pin, a series RC filter is required when operating at dimming frequencies below 1kHz. The reason is that the DFS pin is the output of a transconductance differential amplifier. The differential amplifier has a high-frequency pole.

At low dimming frequencies of around 1kHz R_{DFS} is high around 100kΩ and the differential amplifier pole produces a phase shift that can cause instabilities in the DFS control.

Therefore, a RC filter is required to compensate for the lagging phase shift created by the pole by adding a zero and therefore, a phase lead at the DFS pin. Use a 4kΩ resistor in series with a 2.2nF ceramic capacitor. When using a dimming frequency of 2 kHz or less. The filter has no ill effect at higher dimming frequencies.

COMP

Connect a capacitor and resistor to ground to compensate the boost stage.

DRC

Dimming Ratio Control (DRC) is an input PWM dimming control. The MIC3263 converts this to one of sixteen dimming ratios that is used to dim the LEDs. The dimming ratio is built on a log scale.

CINT

C_{INT} integrates the DRC input pulse. For a PWM frequency range of around 1kHz use 100nF. For a PWM frequency range of around 20kHz pulse, use 10nF. For a PWM frequency range of around 100Hz pulse use 1µF.

ISET

Set the LED current of all six channels by this resistor. Use 2kΩ for 30mA and 3kΩ for 20mA. The R_{ISET} is inversely proportional to I_{LED}. Use the following equation to find R_{ISET}:

$$R_{ISET} = \frac{60}{I_{LED}} \Omega$$

For the best current matching accuracy design for an I_{LED} current of 15mA to 30mA.

CRV

Use a 2.2µF capacitor at the CRV pin. This is used as the reference voltage of the boost stage. The CRV capacitor is continually being charged or discharged in order to keep V_{OUT} at the right level (refer to Functional Diagram illustration). CRV will be charged to keep the IO's at about 1.2V.

IO1–IO6

These are the connections to the linear-mode current amplifier in each channel. Connect the cathode end of the LED channels to these pins. The control loop will keep this at about 1.2V. 1.2V insures that the current amplifier is in the linear region and therefore can regulate the LED current.

In cases where there are a different number of LEDs in a channel, the V(IO) of the channel with the fewest LEDs will have a higher V(IO). V(IO) can be as high as 7.5V before the fault monitoring circuits will sense that channel as a short to V_{OUT}.

When there are a different number of LEDs in a channel the IO voltage will be higher in the channels that have less LEDs in order to keep the LEDs biased correctly. A difference of up to 7.5V between channels can occur because of this. If the circuits that monitors the IO pins sees a fault, that channel will turn off and that channel's IO pin will be at high impedance. An off channel's IO pin will be near or below the booster output voltage. On a channel that has a shorted LED, that channel's IO voltage will increase to keep correct voltage drops on the other series LEDs. It is best to use equal number of LEDs in each channel but there will always be differences in the LEDs voltage drops so all IOs will not have the exact same voltage. Each channel has its own monitoring circuit monitoring the IO1–IO6 pins. If any V(IO) drops below 0.5V (if an LED opens), that channel is turned off and the other channels are unaffected. If any IO goes about 7.5V (if several LEDs short to V_{OUT}), that channel is turned off and the other channels are unaffected.

VSW

This is the boost-stage switch node, the collector of the internal power switch.

EN

Connect EN high to enable the part, low to disable. Do not leave the EN pin floating.

VIN

Supply voltage to the part (6V–40V).

VDD

This is the output of the internal LDO regulator. Connect a 10µF ceramic capacitor to this pin.

PWM Dimming

The duty cycle of the PWM pulse applied to the DRC input is converted to 16 log levels. This logarithmic dimming is a unique feature of the MIC3263 which better matches the sensitivity of the human eye compared to linear dimming. The DRC duty-cycle to DR duty-cycle conversion is shown in Table 2.

N	DRC Duty Cycle %	PWM Dimming Ratio (DR) $DR = 10^{(N-1)/7}$ %
0	0	0
1	6.25	1.0
2	12.5	1.4
3	18.75	1.9
4	25	2.7
5	31.25	3.7
6	37.5	5.2
7	43.75	7.2
8	50	10
9	56.25	14
10	62.5	19
11	68.75	27
12	75	37
13	81.25	52
14	87.5	72
15	93.75	100

Table 2. Dimming Ratio

To avoid skipping between dimming levels, the MIC3263 uses Flicker-Free Dimming control. This technique uses a digital filter and hysteresis on the DRC pulse to provide a clean DR output. The digital filter has a 0.1µF capacitor on the CINT pin to average the duty cycles of the PWM pulses. The averaged duty cycle has to be 4.16% higher than the nominal value before moving to the next dimming level as shown in Figure 7. Likewise, to move the previous dimming level the duty cycle has to be –4.16% lower than the nominal. To prevent flicker the duty-cycle hysteresis is set a 2%.

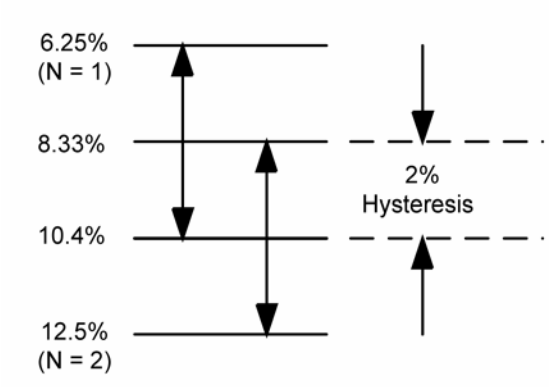


Figure 7. Duty-Cycle Thresholds and Hysteresis

PWM Dimming Limits

The minimum pulse width of the PWM Dim is determined by the PWM Dimming frequency and the L and C used in the boost stages output filter. At low-PWM Dimming frequencies, higher dimming ratios can be achieved:

$$\text{Dim Ratio} = \frac{T_{PWMD}}{T_{LEDON}}$$

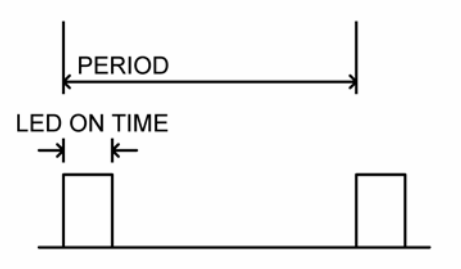


Figure 8. PWM Dimming Ratio

Consider that the human eye will perceive light flicker at a PWM dimming frequency below 100Hz. At 100Hz the time between pulses is 10µs. If the PWM dimming minimum pulse width is 5µs, then:

$$\text{Dim Ratio} = \frac{10\text{ms}}{5\mu\text{s}} = 2000/1$$

If high dimming ratios are required, a lower dimming frequency is required. During each DR pulse, the inductor current has to ramp up to it steady state value to generate the necessary boost output voltage in order for the full programmed LED current to flow in the LED channels. The smaller the inductance value the faster this time is and a narrower PWM dimming pulse can be achieved. But smaller inductance means higher ripple current.

Figure 9 shows the waveforms during PWM dimming pulses. The DRC duty cycle is 75% and therefore the dimming ratio (DR) is 37%. Ch1 is the switch node. Ch2 is the sum of all six ILED channels. Figure 9 shows the boost converter is OFF (not switching) between PWM dimming pulses.

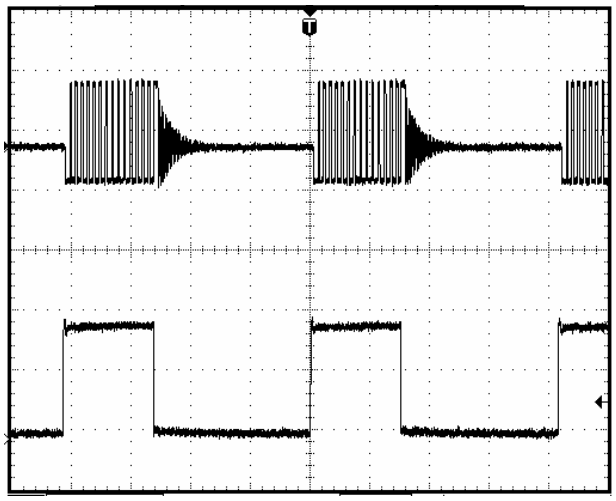


Figure 9. PWM Dimming Pulses
(Ch1 Switch Node; Ch2 is the I_{LED} Total)

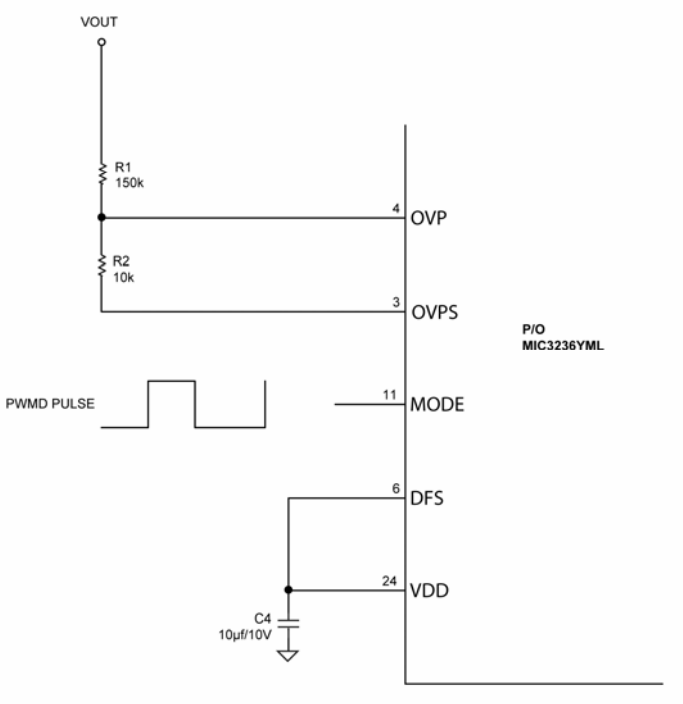


Figure 10. Direct Dimming Control

Direct Dimming

For direct dimming control connect DFS to V_{DD} and use the MODE pin for the dimming pulse. This method will bypass the internal dimming control and allows for dimming control by the external PWM Dimming pulse (see Figure 9).

Boost Stage

A current-mode control is easier to compensate than voltage mode control, thus allowing for a less complex control loop stability design. An error amplifier amplifies the difference between the feedback voltage and the voltage on the CRV capacitor. This amplified error signal is called the $V_{CONTROL}$. A PWM comparator compares the output of the error amp ($V_{CONTROL}$) to the sum of inductor current and slope compensation currents. When the current sums reach $V_{CONTROL}$, the PWM pulse is terminated and the boost power switch is turned off. A portion of the energy stored in the inductor flows into the output capacitor.

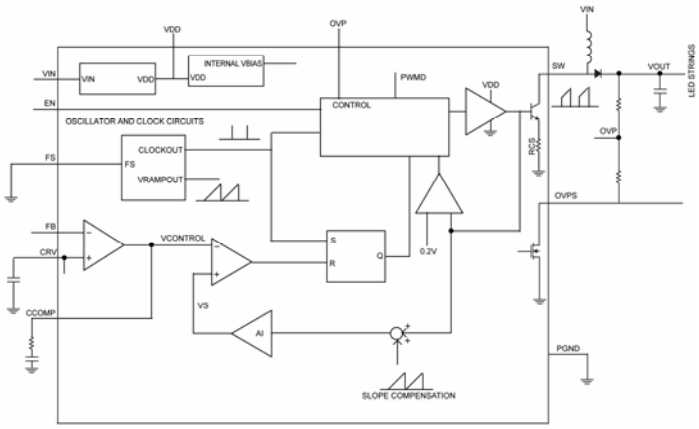


Figure 11. Boost Stage

The operating duty cycle can be calculated using the equation provided below:

$$D = \frac{(V_{OUT} - eff \times V_{IN})}{V_{OUT}} \text{ and } D' = 1 - D$$

Find L using the following equation:

$$L = \frac{V_{IN} \times D}{I_{L\_PP} \times F_{sw}}$$

I_{L_PP} is the inductor peak-to-peak ripple current.

Use a I_{L_PP} of 20% to 40% of the total load current. F_{SW} is the boost switching frequency.

Output Capacitor

In a boost converter, to find the C_{OUT} for a given V_{OUT} ripple use the following calculation:

$$C_{OUT} = \frac{I_{LED_{total}} \times D}{V_{RIPPLE} \times F_{sw}}$$

V_{RIPPLE} can usually be kept below 50mV:

$$I_{LED\_TOTAL} = 6 \times 30mA = 180mA$$

In the MIC3263, the LED current in each channel is individually regulated by that channels current amplifier (linear current regulator). These current regulators are fast enough to follow the boost output voltage ripple and to keep the LED ripple currents much lower than C_{OUT} can filter the output ripple voltage.

Slope Compensation

The boost stage uses peak current mode and requires slope compensation. Slope compensation is required to maintain internal stability of the boost stage across all duty cycles and to prevent any unstable oscillations. The MIC3263 uses a combination of internal slope compensation and a additional slope compensation that is set by an external resistor, RSLP. The ability to set the proper slope compensation through the use of a single external component results in design flexibility. This slope compensation resistor, RSLP, can be calculated as follows:

$$RSLP = \frac{V_{OUT(MAX)} - L \times F_{sw}}{8.64 \times 10^{-6} \times V_{IN(MIN)}}$$

where $V_{IN(MAX)}$ and $V_{OUT(MAX)}$ can be selected to system specifications. The lowest value of RSLP should be 15kΩ. Calculate RSLP using the lowest V_{IN} and maximum V_{OUT} the system will operate.

Example: For these operating conditions:

$V_{IN(MIN)}$ = 12V, $V_{OUT(MAX)}$ = 32V, L = 22µH,
F_{SW} = 1MHz

$$RSLP = \frac{32V - 22\mu H \times 1Mhz}{8.64 \times 10^{-6} \times 12V} = 96.5k\Omega$$

Use the next highest standard value.

Table 3 compiles and lists RSLP values for one set of operating conditions. Select RSLP for V_{IN_MIN} and V_{O_MAX}.

V_{IN} = 12V, V_{OUT} = 32V			
F(kHz)	8.2µH	10µH	22µH
	RSLP	RSLP	RSLP
400	2.77E+05	2.70E+05	2.24E+05
500	2.69E+05	2.60E+05	2.03E+05
600	2.61E+05	2.51E+05	1.81E+05
700	2.53E+05	2.41E+05	1.60E+05
800	2.45E+05	2.31E+05	1.39E+05
900	2.37E+05	2.22E+05	1.18E+05
1000	2.30E+05	2.12E+05	96451
1100	2.22E+05	2.03E+05	75231
1200	2.14E+05	1.93E+05	54012
1300	2.06E+05	1.83E+05	32793
1400	1.98E+05	1.74E+05	15000
1500	1.90E+05	1.64E+05	15000
1600	1.82E+05	1.54E+05	15000
1700	1.74E+05	1.45E+05	15000
1800	1.66E+05	1.35E+05	15000

Table 3. RSLC Values

Boost Compensation

Current-mode control simplifies the compensation. In current mode the double pole created by the output L and C is reduced to a single pole. The explanation for this is beyond the scope of this data sheet, but it can be thought because the inductor current becomes a constant current source and can't act to change phase.

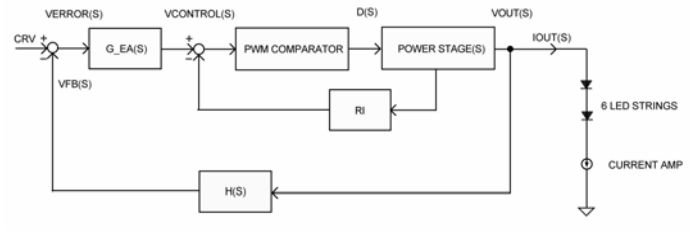


Figure 12. MIC3263 Current-Mode Loop Diagram

From the small signal block diagram the loop transfer function is:

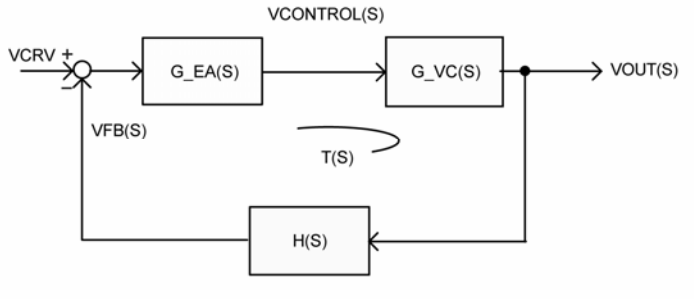


Figure 13. Simplified Voltage Control Loop

Equation 2:

$$T(s) = G_{ea}(s) \times G_{VC}(s) \times H(s)$$

where:

$$H(s) = \frac{V_{CRV}}{V_{OUT}} \text{ and}$$

$$G_{ea}(s) = g_m \left(Z_O \text{ II } \left(R_{COMP} + \frac{1}{sC_{COMP}} \right) \right)$$

Equation 3:

$$G_{vc}(s) = \frac{V_{OUT}(s)}{V_{CONTROL}(s)}$$

$$= \left(\frac{1}{Ri}\right)\left(\frac{D'R_{LOAD}}{2}\right)\frac{\left(1 - \frac{sL}{D'^2 R_{LOAD}}\right)}{\left(1 + \frac{sR_{LOAD}C_{OUT}}{2}\right)}$$

where $R_{LOAD} = \frac{V_{OUT}}{I_{OUT}}$ and $Ri = Ai \times Rcs = 0.4\Omega$.

$A_i = 20$

$R_{CS} = 0.02\Omega$

A_I and R_{CS} are quantities that are internal to the MIC3263.

The equation for $G_{VC}(S)$ is a theoretical model and should give an approximate idea of where the poles and zeros are located.

Equation 3 shows that $s = \frac{D'^2 R_{LOAD}}{L}$ is a right-half plane zero (f_{RHPZ}):

Equation 4:

$$\text{RHP Zero} \rightarrow f_{RHPZ} = \frac{D'^2 R_{LOAD}}{2\pi L}$$

The loop bandwidth should be about 1/10 of the f_{RHPZ} to ensure stability. From Equation 3, it is shown that there is only the single pole due to $R_{LOAD}C_{OUT}$. This greatly simplifies the compensation.

One needs only to get a bode plot of the transfer function of the control to output $G_{VC}(S)$ with a network analyzer.

To measure $G_{VC}(S)$, tie CRV to a DC voltage source. Tie CRV to the steady state voltage that CRV will operate usually between 1V and 2.4V. By connecting CRV to a constant DC voltage, this effectively opens the CRV control loop and allows the measurement of the boost control loop. $G_{VC}(S)$ can be calculated with a computer using the above equation. From the bode plot of $G_{VC}(S)$ find what the gain of $G_{VC}(s)$ is at 1/10 of f_{RHPZ} or less. Next design the error amp gain $G_{EA}(s)$ so the loop gain at the cross over frequency $T(f_{CO})$ is 0db where f_{CO} =1/10 of f_{RHPZ} or lower.

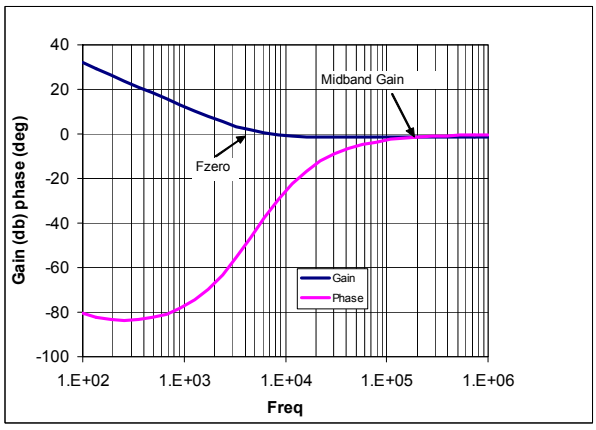


Figure 14. Error Amp Transfer Function

Error Amp

The error amp is a g_m type and the gain – $G_{EA}(S)$ – is:

Equation 5:

$$G_{ea}(s) = g_m \left(Z_O \text{ II } \left(R_{COMP} + \frac{1}{sC_{COMP}} \right) \right)$$

g_m = 0.056mA/V and Z_O = 5MΩ. The error amplifier zero is $f_{Zero} = \frac{1}{2\pi R_{COMP} C_{COMP}}$. Set the f_{CO} at the mid band where $G_{EA}(f_{CO}) = g_m \times R_{COMP}$. At $f_{ZERO} \times 10$ the phase boost is near its maximum.

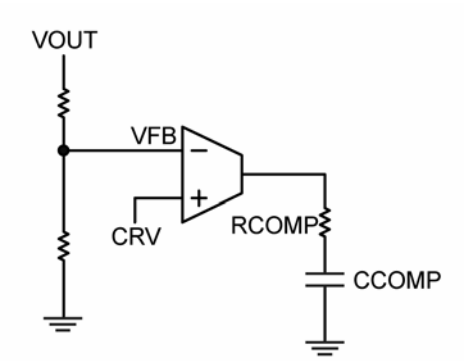


Figure 15. Internal Error Amp and External Compensation

Example 1

Conditions: V_{IN} = 12V, V_{OUT} = 29V, I_{OUT} = 0.18A, L = 22µH, C_{OUT} = 4.7µF $R_{LOAD} = V_{OUT}/I_{OUT}$ = 161Ω. When V_{CRV} = 1.8V, the f_{RHPZ} is:

$$f_{RHPZ} = \frac{D'^2 R_{LOAD}}{2\pi L} = 162\text{kHz}$$

Figure 16 shows a plot of:

$$G_{vc}(s) = \frac{V_{OUT}(s)}{V_{CONTROL}(s)}$$

$$= \left(\frac{1}{Ri}\right)\left(\frac{D'R_{LOAD}}{2}\right)\frac{\left(1 - \frac{sL}{D'^2 R_{LOAD}}\right)}{\left(1 + \frac{sR_{LOAD}C_{OUT}}{2}\right)}$$

This example illustrates the R_{HPZ} at 162kHz. Figure 16 details the –90° phase shift due to the R_{HPZ}.

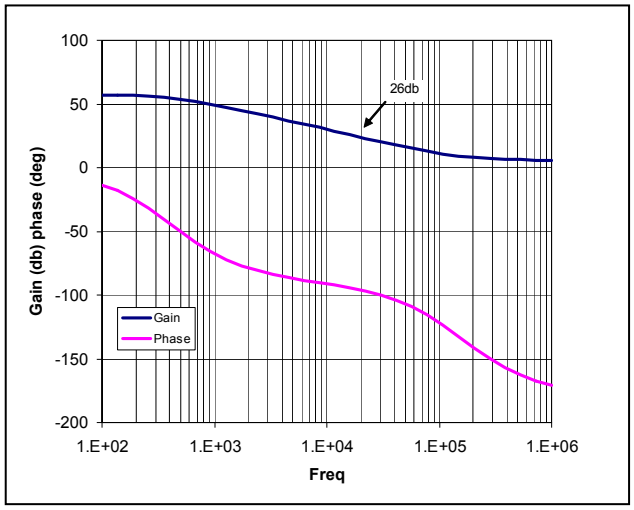


Figure 16. Control-to-Output Gain (G_{VC})

The goal is to make the loop transfer function $T(f_{CO})$ crossover well before the R_{HPZ}.

Chose a $f_{co} = \frac{f_{RHPZ}}{10}$ or less; chose f_{co} = 16kHz .

From the plot and or calculation, the magnitude of:---

$$\left|G_{VC}(16kHz)\right| = 26db$$

$$\left|H(s)\right| = 20Log\left(\frac{1.8V}{29V}\right) = -24db$$

From:

$$T(s) = G_{ea}(s) * G_{VC}(s) * H(s)$$

$$\left|T(16kHz)\right| = \left|G_{ea}(16kHz)\right| + 26db - 24db = 0$$

$$\left|G_{ea}(16kHz)\right| = -2db \rightarrow 0.8v/v$$

$$0.8 = g_m\left(Z_O \,\|\, R_4\right) \cong g_m * R_4$$

Therefore R4 = 15kΩ. Next set the error amplifier's zero at about 5kHz. Therefore C2 = 2.2nF. The location of the f_{ZERO} affects the phase boost in the loop transfer function. If f_{ZERO} were closer to 16kHz the phase boost would be less and vise versa.

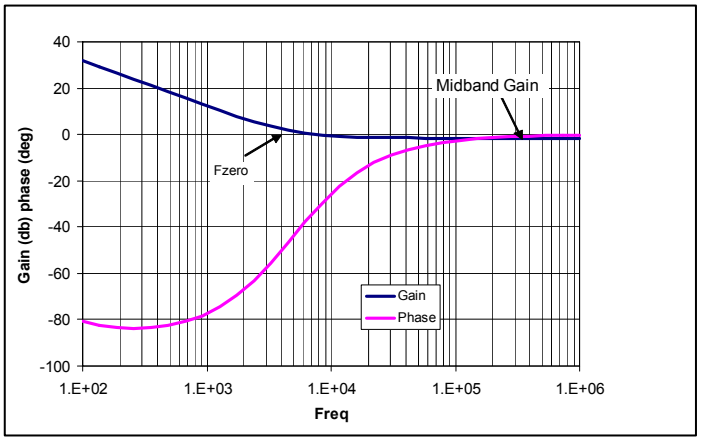


Figure 17. Error Amp Gain and Phase (in Example 1)

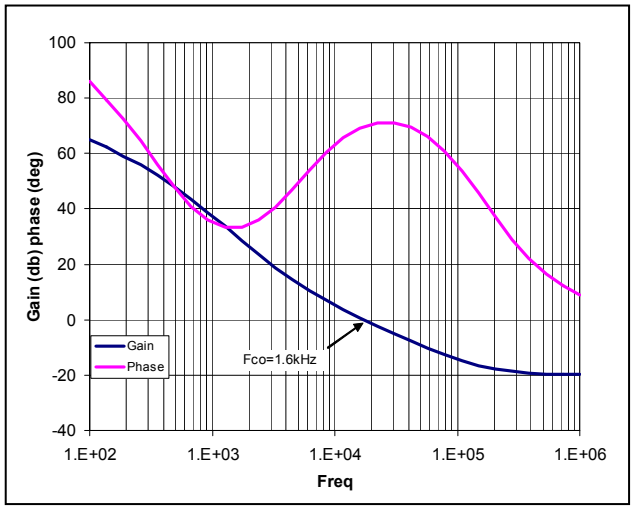


Figure 18. Loop Gain and Phase (in Example 1)

Design Procedure for a LED Driver

Symbol	Parameter	Minimum	Nominal	Maximum	Units
Input					
V_{IN}	Input Voltage	8	12	14	V
I_{IN}	Input Current				
Output					
LEDs	Number of LEDs	8/Channel	8/Channel	8/Channel	
Chs	Number of Channels	6	6	6	Channels
V_F	Forward Voltage of LED	3.4	3.6	4.0	V
V_{IO}	Voltage Drop at the IO Pin	1.1	1.2	2	
V_{OUT}	Output Voltage	28	30	34	V
$I_{LED/ch}$	LED Current/Channel	30	30	30	mA
I_{OUT}				0.18	A
P_{OUT}	Output Power			6.2	W
DIM IN	PWM Dimming	1		100	%
F_{DIM}	Dimming Frequency (internal)		5		kHz
OVP	Output Over-Voltage Protection			40	V
F_{SW}	Switching Frequency		1		MHz
eff	Efficiency	80	85		%
V_{DIODE}	Forward Drop of Schottky Diode		0.5		V

Design Example

In this example, a boost six-channel LED driver operating off a 12V input is being designed. This design has been created to drive six channels of eight LEDs/channels for a total of 48 LEDs. The LED current will be set at 30mA. One is designing for 80% minimum efficiency at a switching frequency of 1MHz.

For 34V out:

Let R2=150k,

$$R1 = \frac{V_{CRV} \times R2}{V_{OUT} - V_{CRV}} = \frac{1.8V \times 150k\Omega}{34V - 1.8V} = 8.39k\Omega$$

Therefore: V_{OVP}= 2.4* (R2+R2)/R1=45V. 45V is too high, meaning V_{CRV} has to operate at a higher voltage than 1.8V. The CRV loop will charge the CRV capacitor to the necessary voltage to regulate.

Let V_{CRV} = 2.2V therefore:

$$R1 = \frac{V_{CRV} \times R2}{V_{OUT} - V_{CRV}} = \frac{2.2V \times 150k\Omega}{34V - 2.2V} = 10.4k\Omega$$

Use the closest standard value of 10.5kΩ.

Therefore:

$$V_{OVP} = 2.4* (R2+R2)/R1 = 40V$$

Select R_{ISET} for a Given ILED

$$R_{ISET} = \frac{60}{I_{LED}}\Omega = \frac{60}{30mA} = 2k\Omega$$

Use 2kΩ for R_{ISET} (R9)

Switching Frequency Set R_{FSW}

To find the value of R_{FSW} use the following equation:

$$R_{FSW}(k\Omega) \approx 500 - 0.3 \times f_{SW}(kHz)$$

$$R_{FSW}(k\Omega) \approx 500 - 0.3 \times (1000) = 200k\Omega$$

Use 200kHz for R_{FSW} (R5).

Dimming Frequency Select Resistor R_{DFS}

F_{DIM} is 5kHz therefore HF mode is used. Connect MODE to V_{DD}. To find R_{DFS} (R8) use the following equation:

$$R_{DFS}(\text{in } k\Omega) = 432 - 20 \times F_{DIM}(\text{in kHz})$$
$$= 432 - 20 \times 10 = 232(k\Omega)$$

The input frequency to the DRC pin can be 100Hz to 40kHz and the internal dimming frequency DR will always be 5kHz.

The duty cycle of the input frequency at DRC is converted according to Table 2 for the actual dimming duty cycle.

Since the dimming frequency is high the filter R6 and C6 is not necessary. They may be used with no ill effect.

Operating Duty Cycle

The operating duty cycle can be calculated using Equation 6.

Equation 6:

$$D_{NOM} = \frac{\left(V_{OUT(NOM)} - \text{eff} \times V_{IN(NOM)}\right)}{V_{OUT(NOM)}}$$

$$D_{MAX} = \frac{\left(V_{OUT(MAX)} - \text{eff} \times V_{IN(MAX)}\right)}{V_{OUT(MAX)}}$$

$$D_{MIN} = \frac{\left(V_{OUT(MAX)} - \text{eff} \times V_{IN(MAX)}\right)}{V_{OUT(MAX)}}$$

Therefore D_{NOM} = 66%, D_{MAX} = 80% and D_{MIN} = 58%.

Inductor Selection

First calculate the RMS input current (nominal, minimum, and maximum) for the system given the operating conditions listed in the design example table. The minimum value of the RMS input current is necessary to ensure proper operation. Using Equation 7, the following values have been calculated:

Equation 7:

$$I_{IN\_RMS(MAX)} = \frac{V_{OUT(MIN)} \times I_{OUT(MIN)}}{\text{eff} \times V_{IN(MAX)}} = 0.43A_{(RMS)}$$

$$I_{IN\_RMS(NOM)} = \frac{V_{OUT(NOM)} \times I_{OUT(NOM)}}{\text{eff} \times V_{IN(NOM)}} = 0.53A_{(RMS)}$$

$$I_{IN\_RMS(MIN)} = \frac{V_{OUT(MAX)} \times I_{OUT(MAX)}}{\text{eff} \times V_{IN(MIN)}} = 0.9A_{(RMS)}$$

I_{OUT} is the same as I_{LED} total

Selecting the inductor current (peak-to-peak) I_{L_PP} to be between 20% to 50% of $I_{IN\_RMS(max)}$, in this case 40%, we obtain:

$$I_{L\_PP(MAX)} = 0.40 \times I_{IN\_RMS(MAX)} = 0.4 \times 0.9 = 0.36A_{PP}$$

There is a trade off between the inductor value and the minimum PWM dimming pulse. The larger the inductor, the longer the PWM dimming pulse time will be. Due to this, the percentage of the ripple current may be limited by the required PWM dimming pulse. Also, the internal current amplifiers will attenuate the LED ripple current by more than a magnitude. It is recommended to operate in the continuous conduction mode. The value of "L" in Equation 8 represents Continuous Conduction Mode.

Equation 8:

$$L = \frac{V_{IN} \times D}{I_{L\_PP} \times F_{SW}}$$

Using the nominal values, one gets:

$$L = \frac{12V \times 0.66}{0.36A \times 1MHz} = 22\mu H$$

If not a standard value, use the next higher standard value. Select the standard inductor value of 22µH.

Going back and calculating the actual ripple current gives:

$$I_{L\_PP} = \frac{V_{IN(NOM)} \times D_{NOM}}{L \times F_{SW}} = \frac{12V \times 0.66}{22\mu H \times 1MHz} = 0.36A_{PP}$$

The average input current is different than the RMS input current because of the ripple current. If the ripple current is low, then the average input current nearly equals the RMS input current. In the case where the average input current is different than the RMS, Equation 9 shows the following:

Equation 9:

$$I_{IN\_AVE(MAX)} = \sqrt{\left(I_{IN\_RMS(MAX)}\right)^2 - \frac{\left(I_{IN\_PP}\right)^2}{12}}$$

$$I_{IN\_AVE(MAX)} = \sqrt{\left(0.9\right)^2 - \frac{\left(0.36\right)^2}{12}} \approx 0.9A$$

The Maximum Peak input current I_{L_PK} can found using Equation 10:

Equation 10:

$$I_{L\_PK(MAX)} = I_{IN\_AVE(MAX)} + 0.5 \times I_{L\_PP(MAX)} = 1.0A$$

The saturation current (I_{SAT}) at the highest operating temperature the inductor must be rated higher than this.

The power dissipated in the inductor is:

Equation 11:

$$P_{INDUCTOR(max)} = I_{IN\_RMS(MAX)}^2 \times DCR$$

A Coilcraft # DO3316P-223ML is used in this example. Its DCR is 85 mΩ, I_{SAT} =2.6A.

$$P_{INDUCTOR(MAX)} = 0.9^2 \times 85\ m\Omega = 67mW$$

Output Capacitor

In this LED driver application, the I_{LED} ripple current is a more important factor compared to that of the output ripple voltage (although the two are directly related). To find the C_{OUT} for a required I_{LED} ripple use the following calculation:

For an output ripple $I_{LED(RIPPLE)}$ = 20mA.

Equation 12:

$$C_{OUT} = \frac{I_{LED(total)} \times D}{V_{Ripple} \times F_{sw}}$$

V_{RIPPLE} can usually be kept below 50mV:

$$I_{LED(total)} = 6 \times 30mA = 180mA$$

$$C_{OUT} = \frac{0.18A \times 0.76}{50mV \times 1Mhz} = 2.7\mu F$$

Use 2.7µF or higher.

The amount that C_{OUT} will discharge depends upon the time between PWM Dimming pluses and the size of the output capacitor. At the next PWM Dimming pulse C_{OUT} has to be charged up to the full output voltage V_{OUT} before the desired LED current flows.

Input Capacitor

The input capacitor is shown in the Typical Application. For superior performance, ceramic capacitors should be used because of their low Equivalent Series Resistance (ESR). The input capacitor C_{IN} ripple current is equal to the ripple in the inductor. The ripple voltage across the input capacitor, is the ESR of C_{IN} times the inductor ripple. The input capacitor will also bypass the EMI generated by the converter as well as any voltage spikes generated by the inductance of the input line. For a required $V_{IN(RIPPLE)}$.

Equation 13:

$$C_{IN} = \frac{I_{IN\_PP}}{8 \times V_{IN(RIPPLE)} \times F_{SW}} = \frac{\left(0.36A\right)}{8 \times 50mV \times 1MHz} = 0.8\mu F$$

This is the minimum value that should be used. To protect the IC from inductive spikes or any overshoot, a larger value of input capacitance may be required. Use 2.2µF or higher as a good safe min.

Rectifier Diode Selection

A Schottky diode is best used here because of the lower forward voltage and the low reverse recovery time. The voltage stress on the diode is the maximum V_{OUT} and therefore, a diode with a higher rating than maximum V_{OUT} should be used. An 80% de-rating is recommended here as well.

Equation 14:

$$I_{DIODE\_(MAX)} = I_{OUT(MAX)} = 0.18A$$

Equation 15:

$$P_{DIODE(MAX)} \approx V_{DIODE} \times I_{DIODE\_(MAX)}$$

A SK34A is used in this example, it's V_{DIODE} is 0.5V.

$$P_{DIODE(MAX)} \approx 0.5V \times 0.18A \approx 0.09W$$

MIC3263 Power Losses

To find the power losses in the MIC3263: There is about 25mA to 35mA input from V_{IN} into the V_{DD} pin. The internal bipolar power switch has an $V_{CE(ON\ MAX)}$ of about 0.5V.

$$V_{CE(ON\ MAX)} \approx 0.5V$$

Equation 16:

$$P_{MIC3263(MAX)} = V_{IN(MAX)} \times 35mA + PWR_{SW(MAX)}$$

Where $PWR_{SW(MAX)}$ is the power loss of the internal bipolar power switch. The power switch power losses are the sum of the on-time losses; $PWR_{SW(MAX)}$ and the switching losses: $PWR_{SW(SWITCHING\ MAX)}$.

$$PWR_{SW(MAX)} = PWR_{SW(MAX)} + PWR_{SW(SWITCHING\ MAX)}$$

Equation 17:

$$PWR_{SW\_ON(MAX)} = I_{SW\_RMS(MAX)} \times V_{CE\_ON\_RMS(MAX)}$$

$$I_{SW\_RMS(MAX)} = \sqrt{D_{(MAX)} \times \left(I_{IN\_AVE(MAX)}^2 + \frac{(I_{IN\_PP})^2}{12} \right)}$$

$$\approx \sqrt{D_{(MAX)}} \times I_{IN\_AVE(MAX)}$$

$$V_{CE\_ON\_RMS(MAX)} = \sqrt{D_{(MAX)}} \times V_{CE\_ON(MAX)}$$

$$PWR_{SW\_ON(MAX)} = D_{(MAX)} \times I_{AVE(MAX)} \times V_{CE\_ON(MAX)}$$

$$PWR_{SW\_ON(MAX)} = 0.8 \times 0.9A \times 0.5V = 0.36W$$

Equation 18:

$$PWR_{SW\_SWITCHING(MAX)} = V_{OUT(MAX)} \times I_{IN\_AVE(MAX)} \times tsw \times F_{sw}$$

tsw ≈ 20ns is the internal power switch on an off transition time

$$PWR_{SW\_SWITCHING(MAX)} = 34V \times 0.9 \times 20ns \times 1MHz = 0.61W$$

Therefore:

$$P_{MIC3263(MAX)} = 14V \times 35mA + 0.97 = 1.46W$$

Snubber

If a high-frequency ringing is present at V_{SW}, a snubber may be needed. A snubber is a damping resistor in series with a DC blocking capacitor in parallel with the power switch. When the power switch turns off, the drain to source capacitance and parasitic inductance will cause a high frequency ringing at the switch node. A snubber circuit as shown in the application schematics may be required if ringing is present at the switch node. A critically damped circuit at the switch node is where R equals the characteristic impedance of the switch node.

Equation 18:

$$R_{SNUBBER} = \sqrt{\frac{L_{PARISITIC}}{C_{DS}}}$$

The explanation of the method to find the best R snubber is beyond the scope of this data sheet. Use $R_{SNUBBER} \approx 2\Omega$ ½ W and $C_{SNUBBER} \approx$ 470pF to 1000pF. If a snubber is used, the power dissipation in the $R_{SNUBBER}$ is:

$$R_{SNUBBER} = C_{SNUBBER} \times V_{OUT}^2 \times F_{SW}$$

$$P_{SNUBBER} = 470pF \times 34V^2 \times 1MHz = 0.54W$$

Table 2 illustrates the power losses in the Design Example.

Description	Value
Power Loss in the L	0.069W
Power Loss in the Schottky Diode	0.09W
MIC3263 Power Loss	1.46W
Maximum Total Losses	1.62W
Minimum Efficiency	80%

Table 2. Major Power Losses

OVP

The output voltage that the OVP will trigger is set according to Equation 19. Using the values for this example gives a max output voltage of:

Equation 19:

$$V_{OVP} = 2.4\times (R2+R2)/R1=40V$$

RSLP

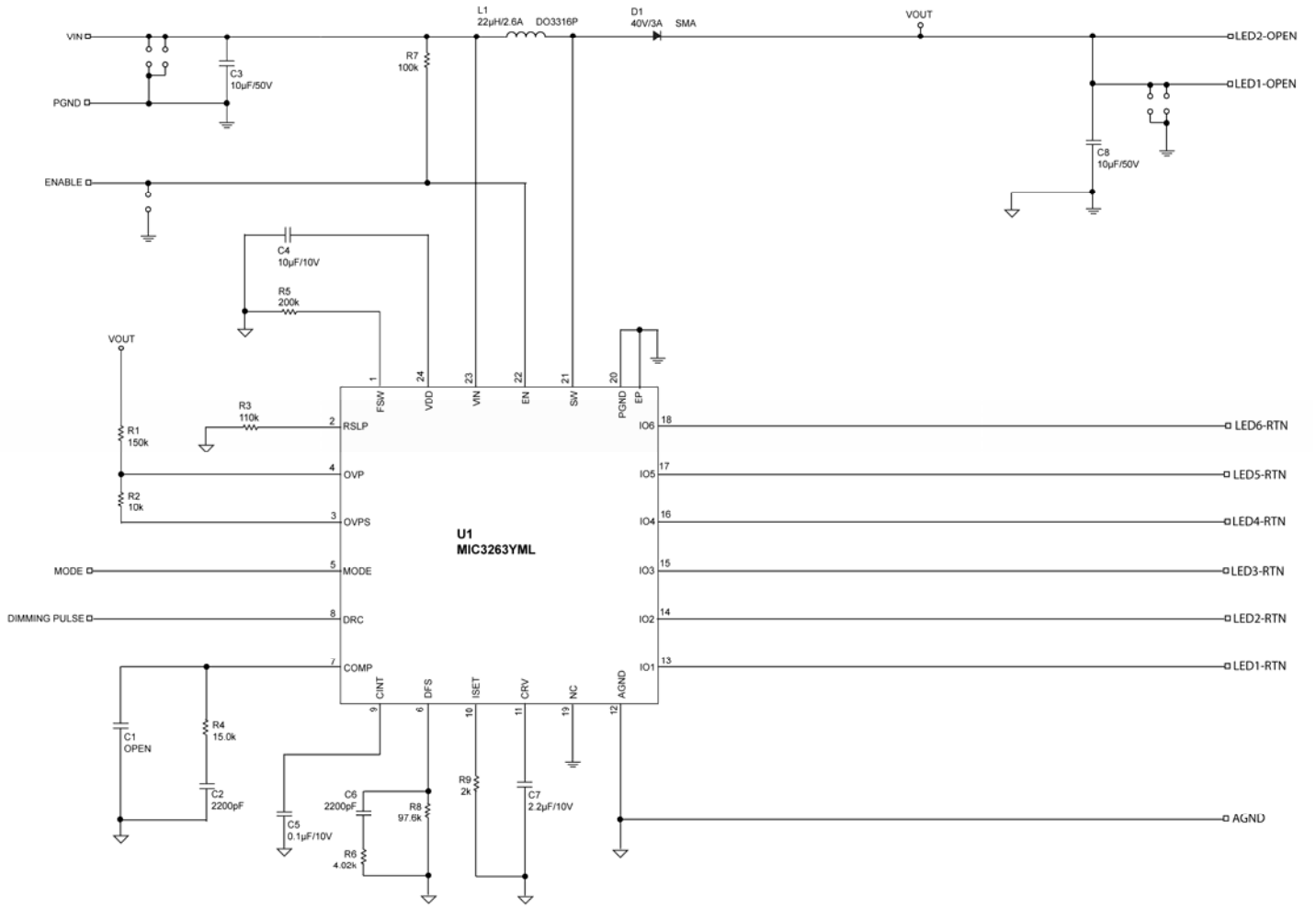
To find RSLP use Equation 1 (which is repeated here): Use the minimum V_{IN} and the maximum V_{OUT}.

$$RSLP = \frac{V_{OUT(MAX)} - L \times F_{sw}}{8.64 \times 10^{-6} \times V_{IN(MIN)}}$$

In this example:

$$RSLP = \frac{34 - 22\mu H \times 1Mhz}{8.64 \times 10^{-6} \times 8} = 174k\Omega$$

Evaluation Board Schematic



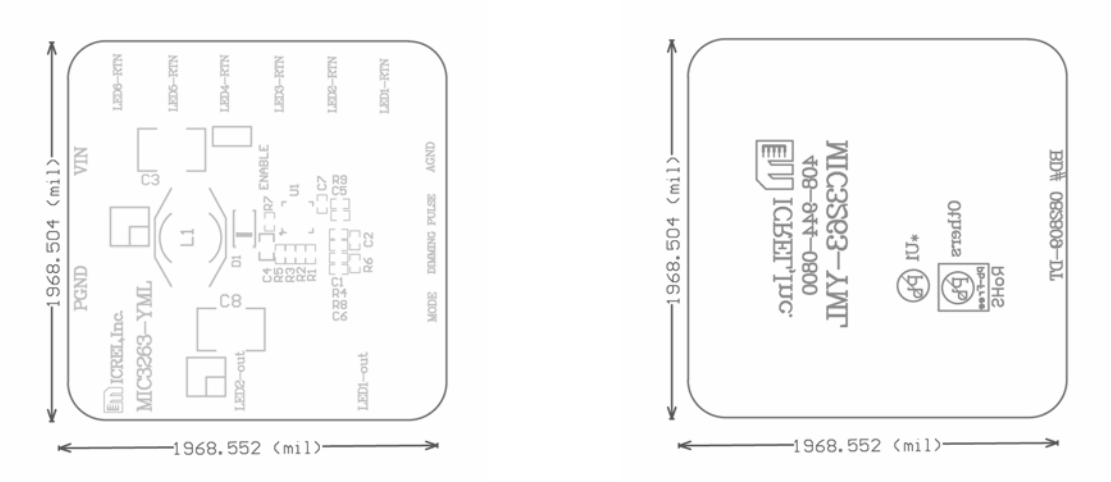
Bill of Materials

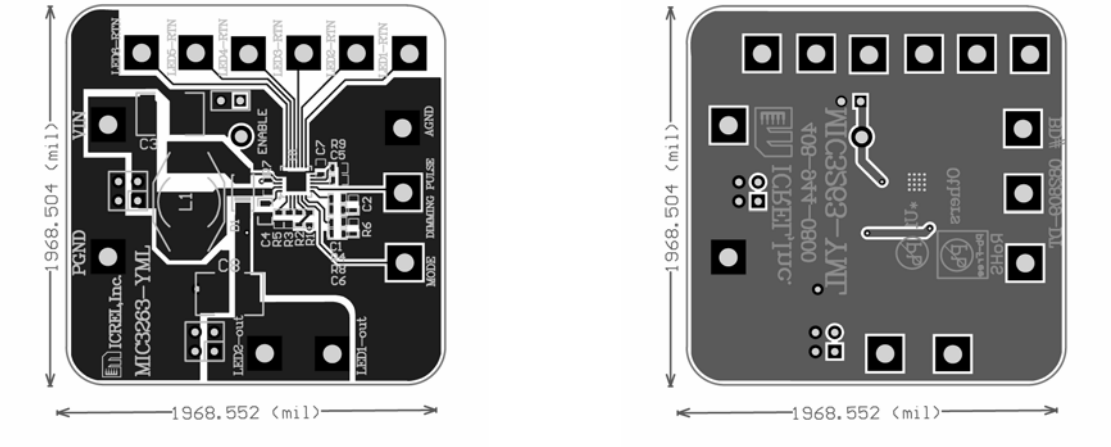
Item	Part Number	Manufacturer	Description	Qty.
C1			OPEN	
C2, C6	0603ZC222KAT2A	AVX[1]	2200pF, 10V, X7R, 0603	2
	C1608X7R1H222K	TDK[2]		
	GRM188R71H222K	muRata[3]		
C3, C8	C5750X7R1H106M	TDK[2]	10µF, 50V, X7R, 2220	2
	22205C106KAZ2A	AVX[1]		
C4	GRM21BR71A106KE51L	muRata[3]	10µF, 10V, 0805	1
	0805ZD106KAT2A	AVX[1]		
C5	0603YC104KAT2A	AVX[1]	0.1µF, 16V, X7R, 0603	1
	C1608X7R1C104K	TDK[2]		
	GRM188R71C104K	muRata[3]		
C7	0603ZD225KAT2A	AVX[1]	2.2µF, 10V, X5R, 0603	1
	GRM188R61A225KE34D	muRata[3]		
	C1608X5R1A225K	TDK[2]		
D1	SK34A	MCC[4]	Schottky 3A, 40V (SMA)	1
	B349LA-13	Diode, Inc. [5]		
L1	DO3316P-223ML	Coilcraft[6]	22µH, 2.6A	1
R1	CRCW0603150KFKEA	Vishay Dale[7]	150k	2
R2	CRCW060310K0FKEA	Vishay Dale[7]	10k	1
R3	CRCW0603110KKFKEA	Vishay Dale[7]	110k (RSLP)	1
R4	CRCW060315K0FKEA	Vishay Dale[7]	15.0k, 0603 (R_{COMP})	1
R6	CRCW060340K2FKEA	Vishay Dale[7]	4.02k	
R5	CRCW0603200KFKEA	Vishay Dale[7]	200k	1
R7	CRCW0603100KFKEA.	Vishay Dale[7]	100k	1
R8	CRCW060326K7FKEA	Vishay Dale[7]	97.6k	1
R9	CRCW06032K00FKEA.	Vishay Dale[7]	2k	1
U1	MIC3263YML	**Micrel, Inc.[8]**	**Six-Channel WLED Driver for Backlighting Applications**	**1**

Notes:

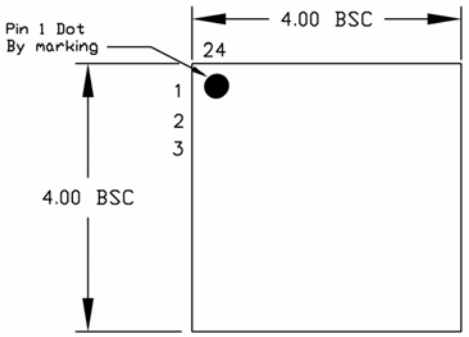
1. AVX: www.avx.com.
2. TDK: www.tdk.com.
3. Murata Tel: www.murata.com.
4. MCC: www.mccsemi.com.
5. Diode, Inc.: www.diodes.com.
6. Coilcraft: www.coilcraft.com.
7. Vishay: www.vishay.com.
8. **Micrel, Inc.: www.micrel.com.**

Evaluation Board PCB Layout

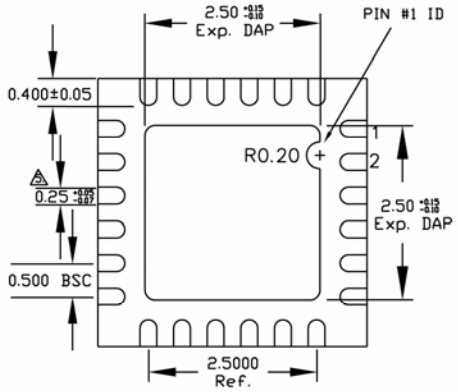




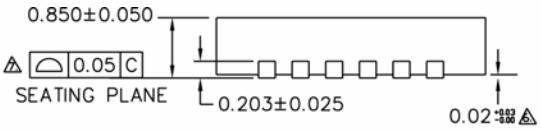
Package Information



TOP VIEW



BOTTOM VIEW



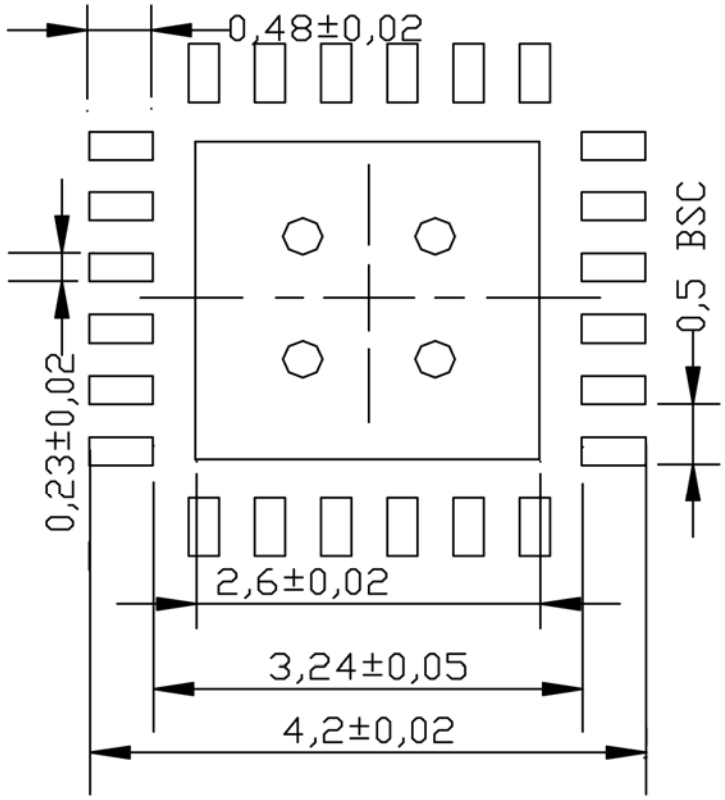
SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

24-Pin 4mm x 4mm (MLF®)

Recommended Land Pattern

LP # MLF44Q-24LD-LP-1
All units are in mm
Tolerance ± 0.05 if not noted



MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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