MONOLITHIC MANCHESTER ENCODER/DECODER (SERIES 3D3523)

RoHS Compliant

data delay devices, inc. ®

FEATURES

- All-silicon, low-power CMOS technology
- Encoder and decoder function independently
- Encoder has buffered clock output
- 3.3V operation
- Vapor phase, IR and wave solderable
- Low ground bounce noise
- **Maximum data rate:** 50 MBaud
- **Data rate range:** ±15%
- **Lock-in time:** 1 bit

PACKAGES

CIN	1	14	VDD
CEN	2	13	CBUF
RX	3	12	LOOP
COUT	4	11	TXENB
DIN	5	10	DOUTB
RESB	6	9	TXB
GND	7	8	TX

3D3523D-xxx   SOIC (.150)

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D3523 is a monolithic CMOS Manchester Encoder/Decoder combo chip. The device uses bi-phase-level encoding to embed a clock signal into a data stream for transmission across a communications link. In this encoding mode, a logic one is represented by a high-to-low transition in the center of the bit cell, while a logic zero is represented by a low-to-high transition.

The Manchester encoder combines the clock (CIN) and data (DIN) into a single bi-phase-level signal (TX). An inverted version of this signal (TXB) is also available. The data baud rate (in MBaud) is equal to the input clock frequency (in MHz). A replica of the clock input is also available (CBUF).

The encoder may be reset by setting the RESB input low; otherwise, it should be left high. The TX and TXB signals may be disabled (high-Z) by setting TXENB high. Similarly, CBUF may be disabled by setting CEN low. Under most operating conditions, TX and TXB are always enabled, and CBUF is not used. With this in mind, the 3D3523 provides internal pull-down resistors on CEN and TXENB, so that most users can leave these inputs uncommitted.

The Manchester decoder accepts the embedded-clock signal at the RX input. The recovered clock and data signals are presented on COUT and DOUTB, respectively, with the data signal inverted. The operating baud rate (in MBaud) is specified by the dash number of the device. The input baud rate may vary by as much as ±15% from the nominal device baud rate without compromising the integrity of the information received.

Because the decoder is not PLL-based, it does not require a long preamble in order to lock onto the received signal. Rather, the device requires at most one bit cell before the data presented at the output is valid. This is extremely useful in cases where the information arrives in bursts and the input is otherwise turned off.

Normally, the encoder and decoder function independently. However, if the LOOP input is set high, the encoded TX signal is fed back internally into the decoder and the RX input is ignored. This feature is useful for diagnostics. The LOOP input has an internal pull-down resistor and may be left uncommitted if this feature is not needed.

PIN DESCRIPTIONS

Encoder:
CIN   Clock Input
DIN   Data Input
RESB   Reset
CEN   Clock buffer enable
TXENB Transmit enable
CBUF   Buffered clock
TX,TXB Transmitted signal

Decoder:
RX   Received Signal
COUT   Recovered Clock
DOUTB Recovered Data

Common:
LOOP   Loop enable
VDD   +3.3 Volts
GND   Ground

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TABLE 1: PART NUMBER SPECIFICATIONS

PART NUMBER	DECODER BAUD RATE (MBaud)		
	Nominal	Minimum	Maximum
3D3523D-0.5	0.50	0.43	0.57
3D3523D-1	1.00	0.85	1.15
3D3523D-5	5.00	4.25	5.75
3D3523D-10	10.00	8.50	11.50
3D3523D-20	20.00	17.00	23.00
3D3523D-25	25.00	21.25	28.75
3D3523D-50	50.00	42.50	57.50

NOTE: Any baud rate between 0.5 and 50 MBaud not shown is also available at no extra cost.

APPLICATION NOTES

ENCODER

The Manchester encoder subsystem samples the data input at the rising edge of the input clock. The sampled data is used in conjunction with the clock rising and falling edges to generate the by-phase level Manchester code.

The encoder employs the timing of the clock rising and falling edges (duty cycle) to implement the required coding scheme, as shown in Figure 1. To reduce the difference between the output data high time and low time, it is essential that the deviation of the input clock duty cycle from 50/50 be minimized.

The encoder presents at its outputs the true and the complimented encoded data. The High-to-Low time skew of the selected data output should be budgeted by the user, as it relates to his application, to satisfactorily estimate the distortion of the transmitted data stream. Such an estimate is very useful in determining the functionality and margins of the data link, if a Manchester decoder is used to decode the received data.
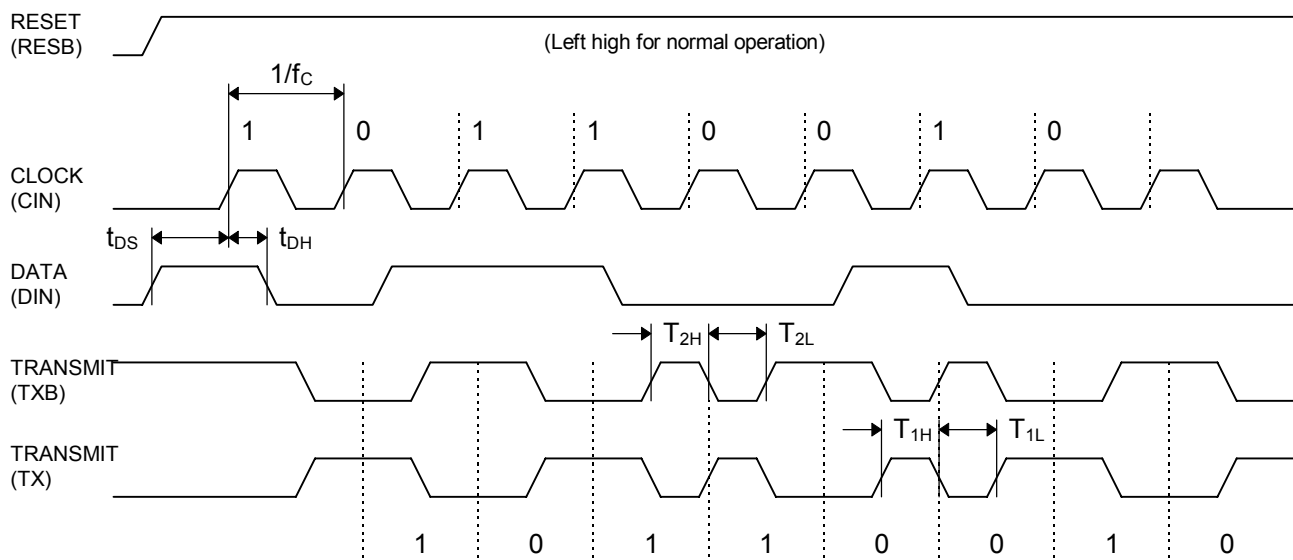

Figure 1: Timing Diagram (Encoder)

APPLICATION NOTES (CONT'D)

DECODER

The Manchester decoder subsystem samples the input at precise pre-selected intervals to retrieve the data and to recover the clock from the received data stream. Its architecture comprises finely tuned delay elements and proprietary circuitry which, in conjunction with other circuits, implement the data decoding and clock recovery function.

Typically, the encoded data transmitted from a source arrives at the decoder corrupted. Such corruption of the received data manifests itself as jitter and/or pulse width distortion at the decoder input. The instantaneous deviations from nominal Baud Rate and/or Pulse Width (high or low) adversely impact the data extraction and clock recovery function if their published limits are exceeded. **See Table 4, Allowed Baud Rate/Duty Cycle.** The decoder, being a self-timed device, is tolerant of frequency modulation (jitter) present in the input data stream, provided that the input data pulse width variations remain within the allowable ranges.

The decoder presents at its outputs the decoded data (inverted) and the recovered clock. The decoded data is **valid at the rising edge of the clock.**

The clock recovery function operates in two modes dictated by the input data stream bit sequence. When a data bit is succeeded by its inverse, the clock recovery circuit is engaged and forces the clock output low for a time equal

to **one over twice the baud rate**. Otherwise, the input is presented at the clock output unchanged, shifted in time. Therefore, the clock duty cycle is strongly dependent on the baud rate, as this will affect the clock-high duration.

The clock output falling edge is not operated on by the clock recovery circuitry. It, therefore, preserves more accurately the clock frequency information embedded in the transmitted data. It can therefore be used, if desired, to retrieve clock frequency information.

INPUT SIGNAL CHARACTERISTICS

The 3D3523 inputs **are CMOS compatible. The user should assure him/herself that** the 50% (of VDD) threshold is used when referring to all timing, especially to the input clock duty cycle (encoder) and the received data (decoder).

POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

CMOS integrated circuitry is strongly dependent on power supply and temperature. The monolithic 3D3523 Manchester encoder/decoder utilizes novel and innovative compensation circuitry to minimize timing variations induced by fluctuations in power supply and/or temperature. Nevertheless, optimum performance is achieved by providing a stable power supply and a clean ground plane, and by placing a bypass capacitor (0.1uf typically) as close to the device as possible.
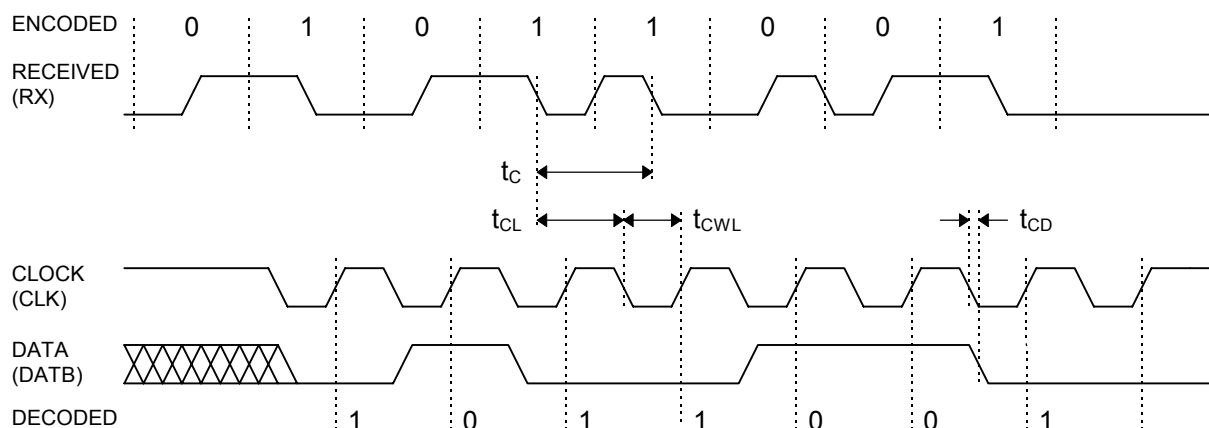
Figure 2: Timing Diagram (Decoder)

DEVICE SPECIFICATIONS

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-10	10	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 3: DC ELECTRICAL CHARACTERISTICS
(-40C to 85C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		5	mA	
High Level Input Voltage	V_{IH}	2.0		V	
Low Level Input Voltage	V_{IL}		1.0	V	
High Level Input Current	I_{IH}		1.0	μA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}		1.0	μA	$V_{IL} = 0V$
High Level Output Current	I_{OH}		-4.0	mA	$V_{DD} = 3.0V$ $V_{OH} = 2.4V$
Low Level Output Current	I_{OL}	4.0		mA	$V_{DD} = 3.0V$ $V_{OL} = 0.4V$
Output Rise & Fall Time	T_R & T_F		2	ns	$C_{LD} = 5$ pf

*I_{DD}(Dynamic) = 2 * C_{LD} * V_{DD} * F
  where: C_{LD} = Average capacitance load/pin (pf)
          F = Input frequency (GHz)

Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

TABLE 4: AC ELECTRICAL CHARACTERISTICS
(-40C to 85C, 3.0V to 3.6V, except as noted)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Baud Rate (Encoder)	f_{BN}			50	MBaud	
Clock Frequency	f_C			50	MHz	
Data set-up to clock rising	t_{DS}	3.5			ns	
Data hold from clock rising	t_{DH}	0			ns	
TX High-Low time skew	$t_{1H} - t_{1L}$	-3.5		3.5	ns	1
TXB High-Low time skew	$t_{2H} - t_{2L}$	-2.0		2.0	ns	1
TX - TXB High/Low time skew	$t_{1H} - t_{2L}$	-3.0		3.0	ns	1
Nominal Input Baud Rate (Decoder)	f_{BN}	5		50	MBaud	
Allowed Input Baud Rate Deviation	f_B	-0.15 f_{BN}		0.15 f_{BN}	MBaud	0C to 70C 25C, 3.3V
Allowed Input Baud Rate Deviation	f_B	-0.05 f_{BN}		0.05 f_{BN}	MBaud	3.0V to 3.6V
Allowed Input Baud Rate Deviation	f_B	-0.03 f_{BN}		0.03 f_{BN}	MBaud	-55C to 125C 3.0V to 3.6V
Allowed Input Duty Cycle		42.5	50.0	57.5	%	
Bit Cell Time	tc		1000/f_B		ns	
Input Data Edge to Clock Falling Edge	t_{CL}		0.75 tc		ns	
Clock Width Low	t_{CWL}		500/f_{BN}		ns	±2ns or 5%
Clock Falling Edge to Data Transition	t_{CD}	3.0	4.0	5.0	ns	

Notes: 1: Assumes a 50% duty cycle clock input

AUTOMATED TESTING - MONOLITHIC PRODUCTS

TEST CONDITIONS

INPUT:
Ambient Temperature: $25^{\circ}C \pm 3^{\circ}C$
Supply Voltage (Vcc): $5.0V \pm 0.1V$
Input Pulse: High = $3.0V \pm 0.1V$
Low = $0.0V \pm 0.1V$
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width: PW_{IN} = 1/(2*BAUD)
Period: PER_{IN} = 1/BAUD

OUTPUT:
R_{load}: $10K\Omega \pm 10\%$
C_{load}: $5pf \pm 10\%$
Threshold: 1.5V (Rising & Falling)

Device Under Test — $10K\Omega$ — Digital Scope
470Ω — 5pf
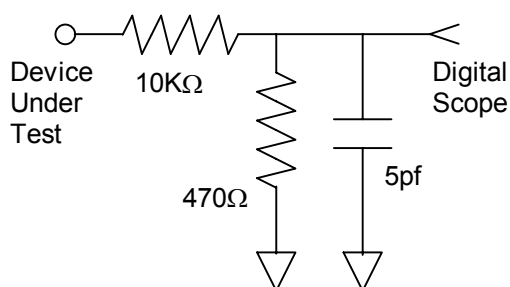
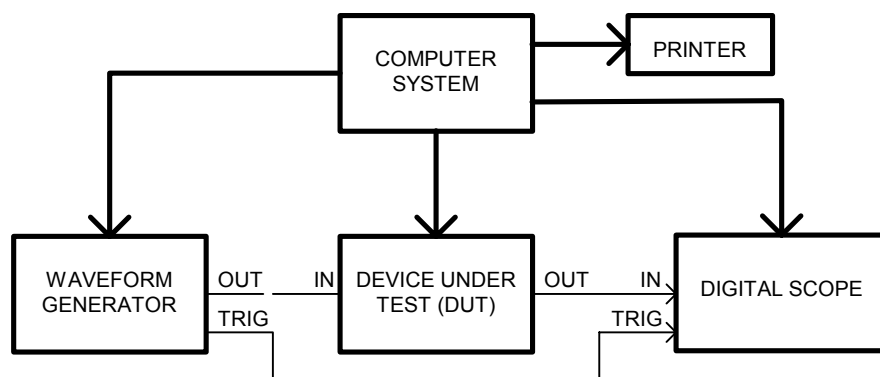**NOTE:** The above conditions are for test only and do not in any way restrict the operation of the device.

Figure 3: Test Setup

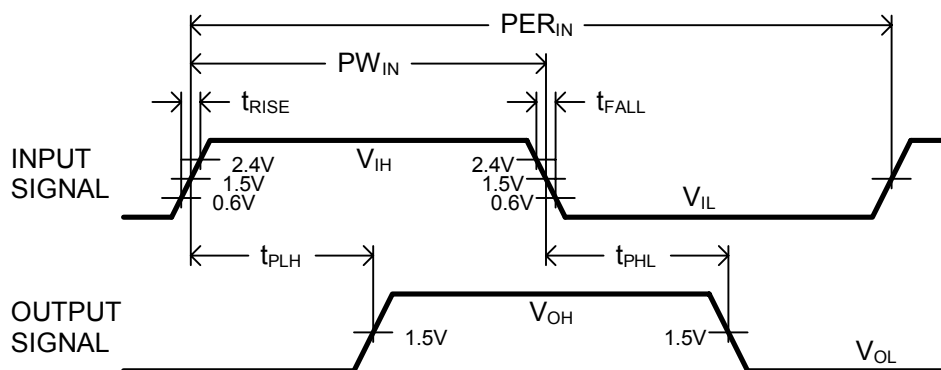**Figure 4: Timing Diagram**