

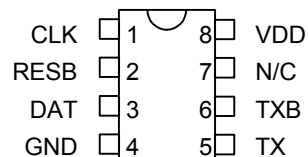
# MONOLITHIC MANCHESTER ENCODER (SERIES 3D3521)



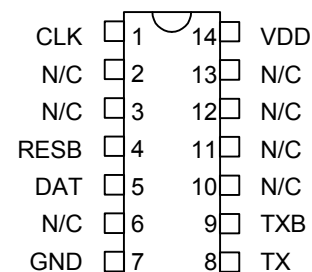
## FEATURES

- All-silicon, low-power CMOS technology
- 3.3V operation
- CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Low ground bounce noise
- **Maximum data rate:** 50 MBaud

## PACKAGES



3D3521Z SOIC (.150)



3D3521D SOIC (.150)

For mechanical dimensions, click [here](#).  
For package marking details, click [here](#).

## FUNCTIONAL DESCRIPTION

The 3D3521 is a monolithic CMOS Manchester Encoder. The clock and data, present at the unit input, are combined into a single bi-phase-level signal. In this encoding mode, a logic one is represented by a high-to-low transition within the bit cell, while a logic zero is represented by a low-to-high transition. The unit operating baud rate (in MBaud) is equal to the input clock frequency (in MHZ). All pins marked N/C must be left unconnected.

The all-CMOS 3D3521 integrated circuit has been designed as a reliable, economic alternative to hybrid Manchester Encoders. It is CMOS-compatible and is offered in space saving surface mount 8-pin and 14-pin SOICs.

## PIN DESCRIPTIONS

|      |                        |
|------|------------------------|
| DAT  | Data Input             |
| CLK  | Clock Input            |
| RESB | Reset                  |
| TX   | Signal Output          |
| TXB  | Inverted Signal Output |
| VDD  | +3.3 Volts             |
| GND  | Ground                 |

## APPLICATION NOTES

The 3D3521 Manchester Encoder samples the data input at the rising edge of the input clock. The sampled data is used in conjunction with the clock rising and falling edges to generate the by-phase level Manchester code.

### INPUT SIGNAL CHARACTERISTICS

The 3D3521 Manchester Encoder inputs **are CMOS compatible. The user should assure himself that** the 50% (of VDD) threshold is used when referring to all timing, especially to the input clock duty cycle.

### CLOCK DUTY CYCLE ERRORS

The 3D3521 Manchester Encoder employs the timing of the clock rising and falling edges (duty cycle) to implement the required coding scheme. To reduce the difference between the output data high time and low time, it is essential that the deviation of the input clock duty cycle from 50/50 be minimized.

### OUTPUT SIGNAL CHARACTERISTICS

The 3D3521 presents at its outputs the true and the complimented encoded data.

The High-to-Low time skew of the selected data output should be budgeted by the user, as it relates to his application, to satisfactorily estimate the distortion of the transmitted data stream.

Such an estimate is very useful in determining the functionality and margins of the data link, if a 3D3522 Manchester Decoder is used to decode the received data.

### POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

CMOS integrated circuitry is strongly dependent on power supply and temperature. The monolithic 3D3521 Manchester encoder utilizes novel and innovative compensation circuitry to minimize timing variations induced by fluctuations in power supply and/or temperature.

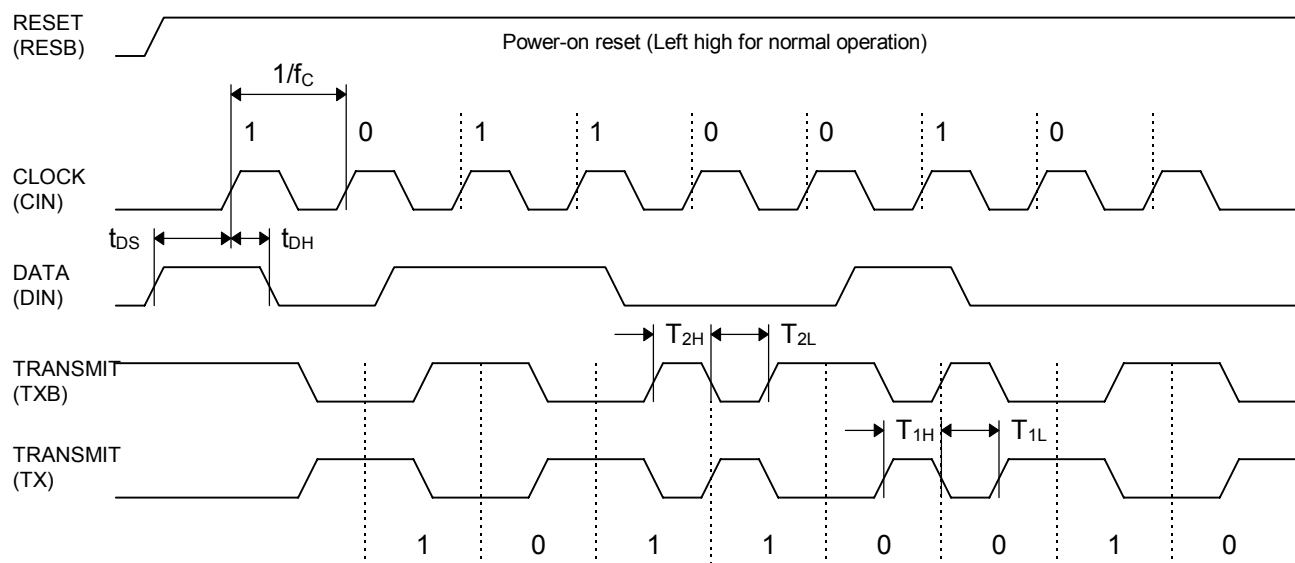


Figure 1: Timing Diagram

## DEVICE SPECIFICATIONS

**TABLE 1: ABSOLUTE MAXIMUM RATINGS**

| PARAMETER           | SYMBOL            | MIN  | MAX                  | UNITS | NOTES  |
|---------------------|-------------------|------|----------------------|-------|--------|
| DC Supply Voltage   | V <sub>DD</sub>   | -0.3 | 7.0                  | V     |        |
| Input Pin Voltage   | V <sub>IN</sub>   | -0.3 | V <sub>DD</sub> +0.3 | V     |        |
| Input Pin Current   | I <sub>IN</sub>   | -10  | 10                   | mA    | 25C    |
| Storage Temperature | T <sub>STRG</sub> | -55  | 150                  | C     |        |
| Lead Temperature    | T <sub>LEAD</sub> |      | 300                  | C     | 10 sec |

**TABLE 2: DC ELECTRICAL CHARACTERISTICS**

(-40C to 85C, 3.0V to 3.6V)

| PARAMETER                 | SYMBOL                          | MIN | MAX  | UNITS | NOTES  |
|---------------------------|---------------------------------|-----|------|-------|--|
| Static Supply Current*    | I <sub>DD</sub>                 |     | 5    | mA    |  |
| High Level Input Voltage  | V <sub>IH</sub>                 | 2.0 |      | V     |  |
| Low Level Input Voltage   | V <sub>IL</sub>                 |     | 1.0  | V     |  |
| High Level Input Current  | I <sub>IH</sub>                 |     | 1.0  | μA    | V <sub>IH</sub> = V <sub>DD</sub>                |
| Low Level Input Current   | I <sub>IL</sub>                 |     | 1.0  | μA    | V <sub>IL</sub> = 0V                             |
| High Level Output Current | I <sub>OH</sub>                 |     | -4.0 | mA    | V <sub>DD</sub> = 3.0V<br>V <sub>OH</sub> = 2.4V |
| Low Level Output Current  | I <sub>OL</sub>                 | 4.0 |      | mA    | V <sub>DD</sub> = 3.0V<br>V <sub>OL</sub> = 0.4V |
| Output Rise & Fall Time   | T <sub>R</sub> & T <sub>F</sub> |     | 2    | ns    | C <sub>LD</sub> = 5 pf                           |

\*I<sub>DD</sub>(Dynamic) = 2 \* C<sub>LD</sub> \* V<sub>DD</sub> \* F  
 where: C<sub>LD</sub> = Average capacitance load/pin (pf)  
 F = Input frequency (GHz)

Input Capacitance = 10 pf typical  
 Output Load Capacitance (C<sub>LD</sub>) = 25 pf max

**TABLE 3: AC ELECTRICAL CHARACTERISTICS**

(-40C to 85C, 3.0V to 3.6V)

| PARAMETER                   | SYMBOL                            | MIN  | TYP | MAX | UNITS | NOTES |
|-----------------------------|-----------------------------------|------|-----|-----|-------|-------|
| Input Baud Rate             | f <sub>BN</sub>                   |      |     | 50  | MBaud |       |
| Clock Frequency             | f <sub>C</sub>                    |      |     | 50  | MHz   |       |
| Data set-up to clock rising | t <sub>DS</sub>                   | 3.5  |     |     | ns    |       |
| Data hold from clock rising | t <sub>DH</sub>                   | 0    |     |     | ns    |       |
| TX High-Low time skew       | t <sub>1H</sub> - t <sub>1L</sub> | -3.5 |     | 3.5 | ns    | 1     |
| TXB High-Low time skew      | t <sub>2H</sub> - t <sub>2L</sub> | -2.0 |     | 2.0 | ns    | 1     |
| TX - TXB High/Low time skew | t <sub>1H</sub> - t <sub>2L</sub> | -3.0 |     | 3.0 | ns    | 1     |

Notes: 1: Assumes a 50% duty cycle clock input

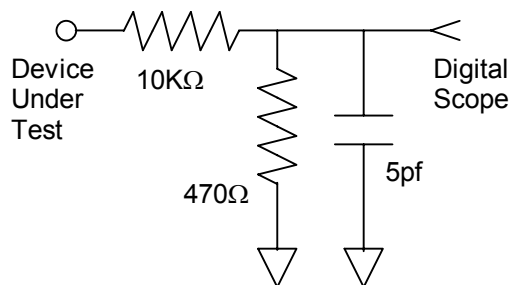
**INPUT:**

Low =  $0.0V \pm 0.1V$

**Period:**  $PER_{IN} = 1/BAUD$

**OUTPUT:**

**Threshold:** 1.5V (Rising & Falling)



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graph TD; CS[COMPUTER SYSTEM] --> PR[PRINTER]; CS --> WG[WAVEFORM GENERATOR]; CS --> DUT[DEVICE UNDER TEST DUT]; CS --> DS[DIGITAL SCOPE]; WG -- OUT --> DUT_IN[DUT IN]; DUT -- OUT --> DS_IN[DS IN]; WG -- TRIG --> DS_TRIG[DS TRIG]; DUT -- TRIG --> DS_TRIG;
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