

# High Voltage, High Gain BIMOSFET™ Monolithic Bipolar MOS Transistor

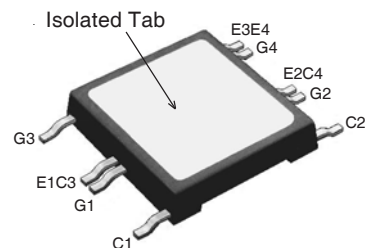
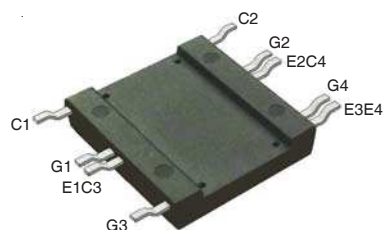
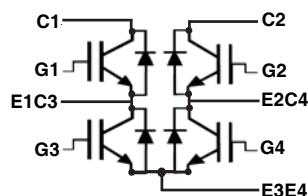
## MMIX4B12N300

$$V_{CES} = 3000V$$

$$I_{C110} = 11A$$

$$V_{CE(sat)} \leq 3.2V$$

(Electrically Isolated Tab)



G = Gate                      E = Emitter  
C = Collector

Symbol	Test Conditions	Maximum Ratings	
$V_{CES}$	$T_C = 25^\circ C$ to $150^\circ C$	3000	V
$V_{CGR}$	$T_J = 25^\circ C$ to $150^\circ C$ , $R_{GE} = 1M\Omega$	3000	V
$V_{GES}$	Continuous	$\pm 20$	V
$V_{GEM}$	Transient	$\pm 30$	V
$I_{C25}$	$T_C = 25^\circ C$	26	A
$I_{C110}$	$T_C = 110^\circ C$	11	A
$I_{CM}$	$T_C = 25^\circ C$ , $V_{GE} = 19V$ , 1ms	98	A
	10ms	52	A
<b>SSOA</b>	$V_{GE} = 15V$ , $T_{VJ} = 125^\circ C$ , $R_G = 20\Omega$	$I_{CM} = 98$	A
<b>(RBSOA)</b>	Clamped Inductive Load	1500	V
$P_C$	$T_C = 25^\circ C$	125	W
$T_J$		-55 ... +150	$^\circ C$
$T_{JM}$		150	$^\circ C$
$T_{stg}$		-55 ... +150	$^\circ C$
$T_L$	1.6mm (0.062 in.) from Case for 10s	300	$^\circ C$
$T_{SOLD}$	Plastic Body for 10 seconds	260	$^\circ C$
$F_C$	Mounting Force	50..200 / 11..45	Nm/lb.in.
$V_{ISOL}$	50/60Hz, 1 Minute	4000	V~
<b>Weight</b>		8	g

Symbol	Test Conditions ( $T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{CES}$	$I_C = 250\mu A$ , $V_{GE} = 0V$	3000		V
$V_{GE(th)}$	$I_C = 250\mu A$ , $V_{CE} = V_{GE}$	3.0		5.0 V
$I_{CES}$	$V_{CE} = 0.8 \cdot V_{CES}$ , $V_{GE} = 0V$ Note 2, $T_J = 125^\circ C$			25 $\mu A$ 1 mA
$I_{GES}$	$V_{CE} = 0V$ , $V_{GE} = \pm 20V$			$\pm 100$ nA
$V_{CE(sat)}$	$I_C = I_{C90}$ , $V_{GE} = 15V$ , Note 1 $T_J = 125^\circ C$		2.8 3.5	V V

### Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage

### Advantages

- Low Gate Drive Requirement
- High Power Density

### Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Capacitor Discharge Circuits

Symbol Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)		Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$I_C = I_{C90}, V_{CE} = 10\text{V}$ , Note 1	6.5	10.8	S
$I_{C(ON)}$	$V_{GE} = 20\text{V}$ , $V_{CE} = 15\text{V}$ , Note 1		200	A
$C_{ies}$	$V_{CE} = 25\text{V}$ , $V_{GE} = 0\text{V}$ , $f = 1\text{MHz}$		1290	pF
$C_{oes}$			56	pF
$C_{res}$			19	pF
$Q_g$	$I_C = I_{C90}, V_{GE} = 15\text{V}$ , $V_{CE} = 1000\text{V}$		62	nC
$Q_{ge}$			13	nC
$Q_{gc}$			8.5	nC
$t_{d(on)}$	<b>Resistive Switching Times, <math>T_J = 25^\circ\text{C}</math></b> $I_C = I_{C90}$ , $V_{GE} = 15\text{V}$ $V_{CE} = 1250\text{V}$ , $R_G = 10\Omega$		64	ns
$t_r$			140	ns
$t_{d(off)}$			180	ns
$t_f$			540	ns
$t_{d(on)}$	<b>Resistive Switching Times, <math>T_J = 125^\circ\text{C}</math></b> $I_C = I_{C90}$ , $V_{GE} = 15\text{V}$ $V_{CE} = 1250\text{V}$ , $R_G = 10\Omega$		65	ns
$t_r$			395	ns
$t_{d(off)}$			175	ns
$t_f$			530	ns
$R_{thJC}$			1.00	$^\circ\text{C/W}$
$R_{thCS}$		0.05		$^\circ\text{C/W}$
$R_{thJA}$		30		$^\circ\text{C/W}$

**Reverse Diode**

Symbol Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)		Characteristic Values		
		Min.	Typ.	Max.
$V_F$	$I_F = 12\text{A}$ , $V_{GE} = 0\text{V}$			2.1 V
$t_{rr}$	$I_F = 6\text{A}$ , $V_{GE} = 0\text{V}$ , $-di_F/dt = 100\text{A}/\mu\text{s}$		1.4	$\mu\text{s}$
$I_{RM}$		$V_R = 100\text{V}$ , $V_{GE} = 0\text{V}$		21

**Notes:**

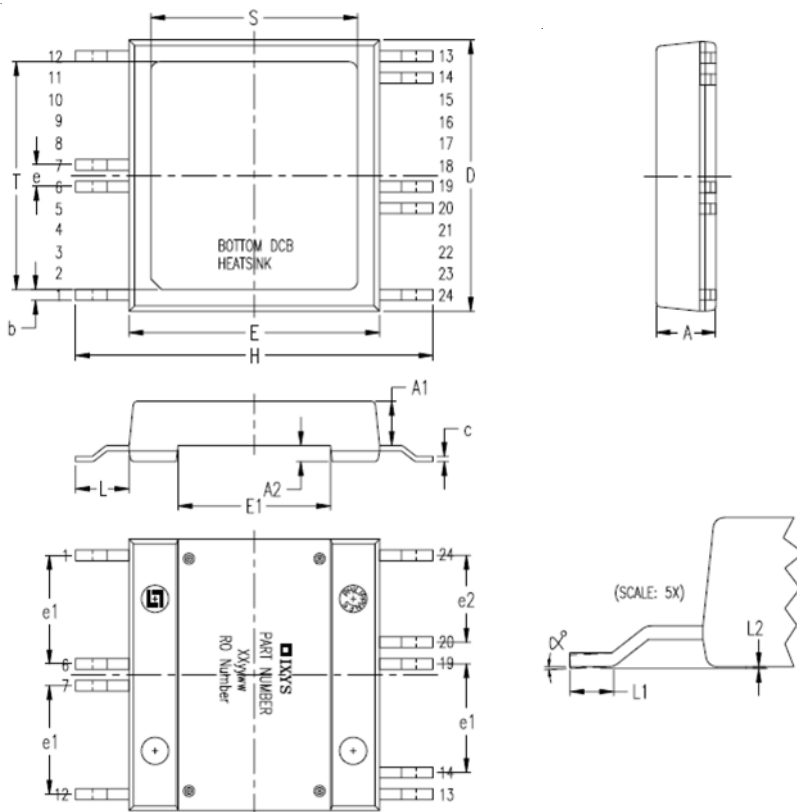
1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .
2. Device must be heatsunk for high temperature leakage current measurements to avoid thermal runaway.

**PRELIMINARY TECHNICAL INFORMATION**

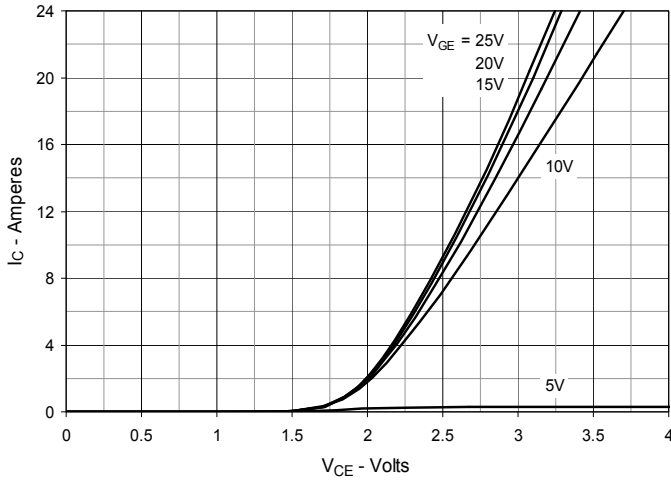
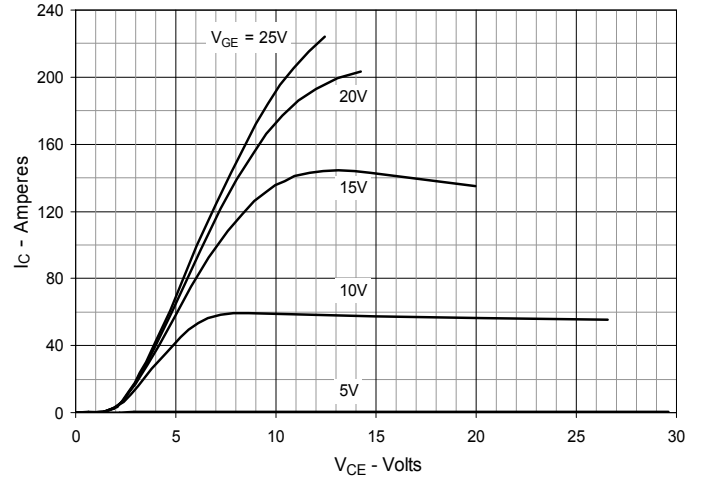
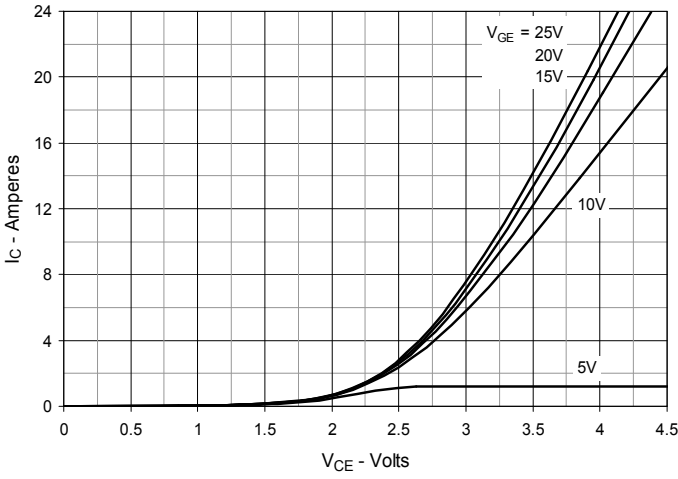
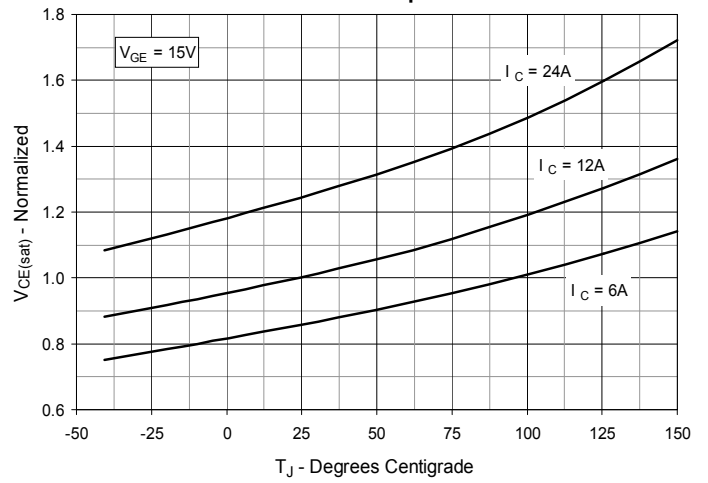
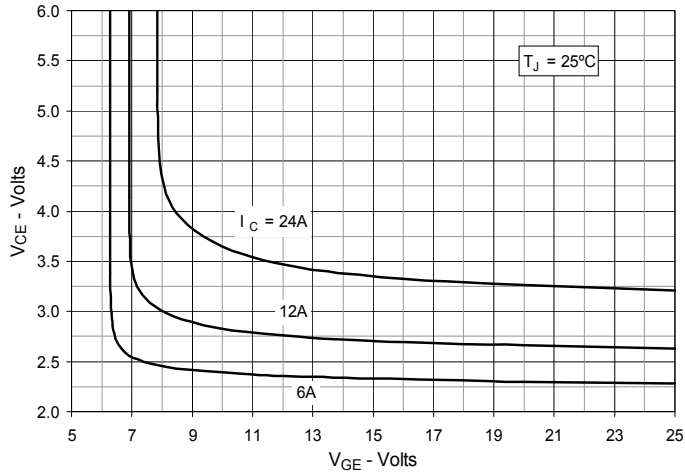
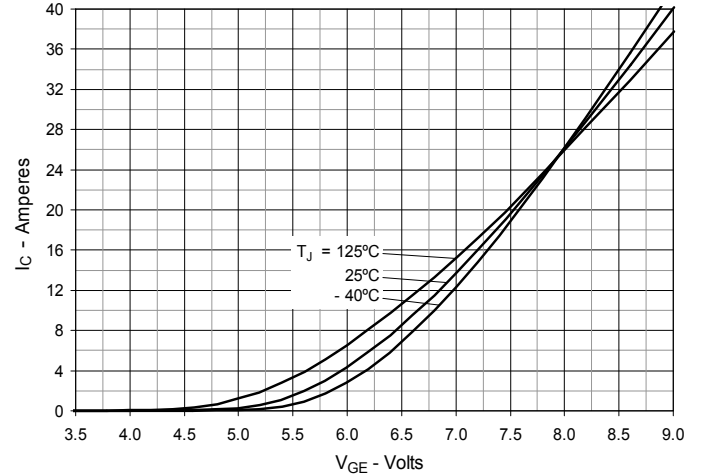
The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

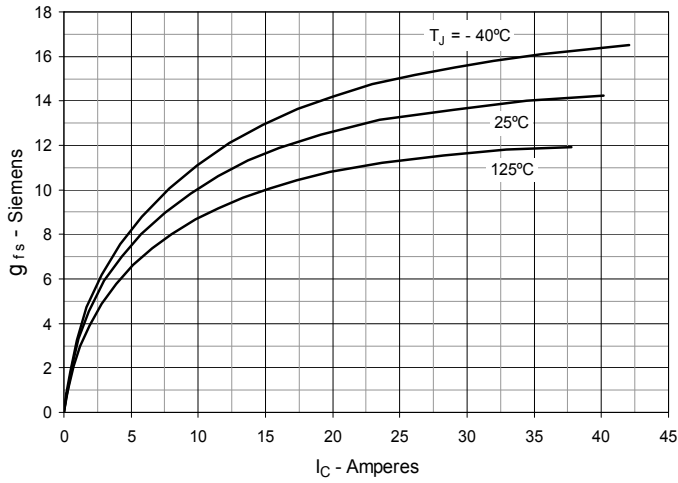
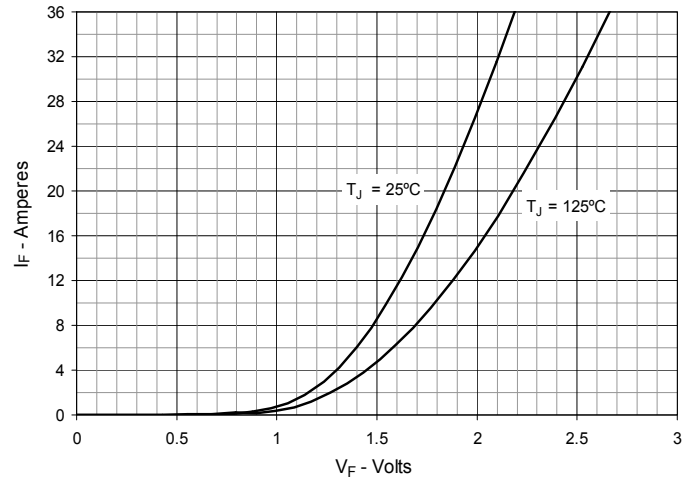
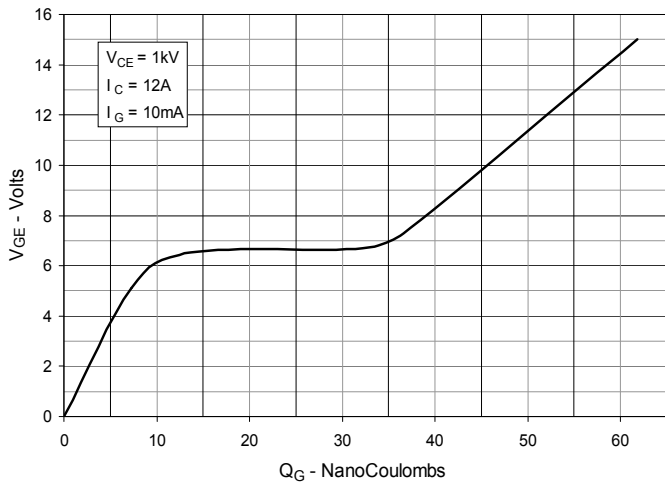
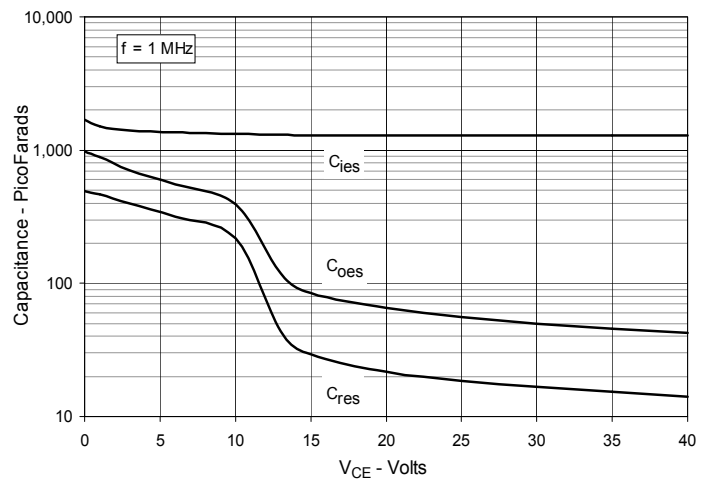
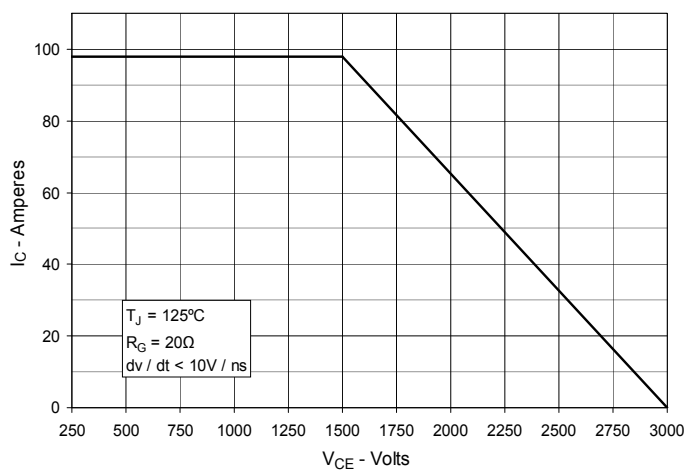
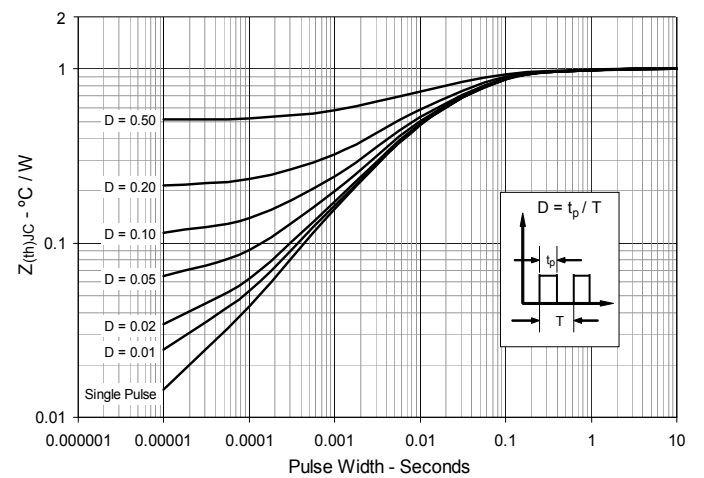
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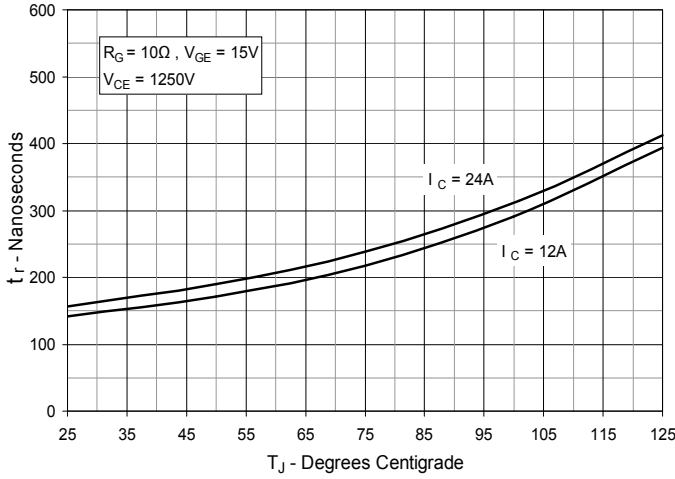
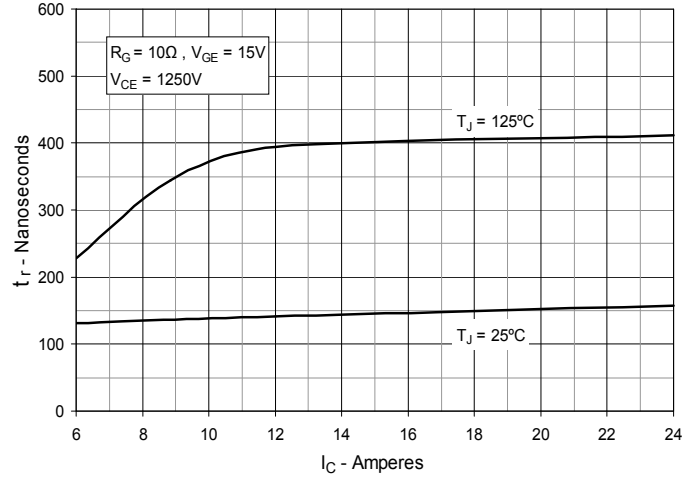
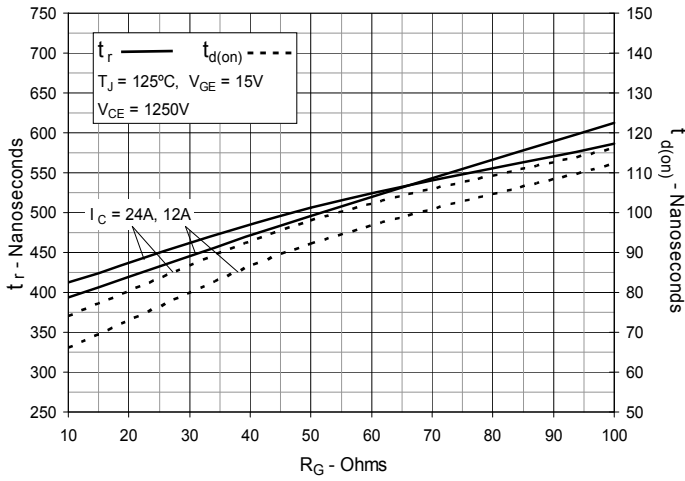
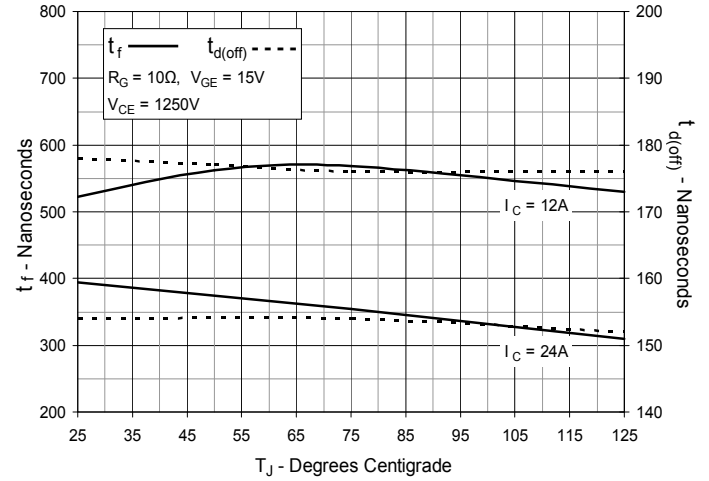
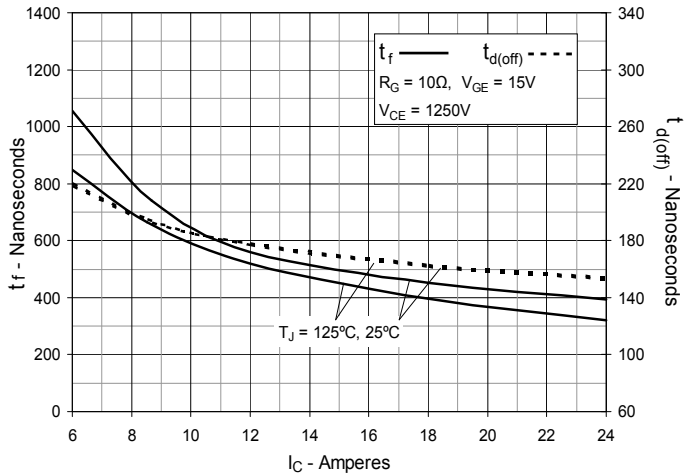
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2  
 4,860,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2  
 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

**Package Outline**


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.976	.994	24.80	25.25
E	.898	.915	22.80	23.25
E1	.543	.559	13.80	14.20
e	.079 BSC		2.00 BSC	
e1	.394 BSC		10.00 BSC	
e2	.315 BSC		8.00 BSC	
H	1.272	1.311	32.30	33.30
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.736	.760	18.70	19.30
T	.815	.839	20.70	21.30
α	0	4°	0	4°

**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 2. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 3. Output Characteristics @  $T_J = 125^\circ\text{C}$** 

**Fig. 4. Dependence of  $V_{CE(sat)}$  on Junction Temperature**

**Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage**

**Fig. 6. Input Admittance**


**Fig. 7. Transconductance**

**Fig. 8. Forward Voltage Drop of Intrinsic Diode**

**Fig. 9. Gate Charge**

**Fig. 10. Capacitance**

**Fig. 11. Reverse-Bias Safe Operating Area**

**Fig. 12. Maximum Transient Thermal Impedance**


**Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature**

**Fig. 14. Resistive Turn-on Rise Time vs. Collector Current**

**Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance**

**Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature**

**Fig. 17. Resistive Turn-off Switching Times vs. Collector Current**

**Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance**
