

HiPerFET™ Power MOSFET

H-Bridge Topology in ECO-PAC 2

N-Channel Enhancement Mode

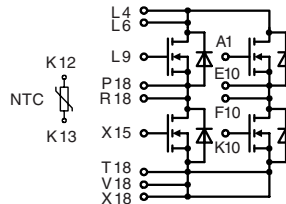
High dv/dt, Low t_{rr} , HDMOS™ Family

$$I_{D25} = 75 \text{ A}$$

$$V_{DSS} = 100 \text{ V}$$

$$R_{DS(on)} = 25 \text{ m}\Omega$$

$$t_{rr} \leq 200 \text{ ns}$$



Pin arrangement see outlines

MOSFETs					
Symbol	Conditions	Maximum Ratings			
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	100		V	
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	100		V	
V_{GS}	Continuous	± 20		V	
V_{GSM}	Transient	± 30		V	
I_{D25}	$T_C = 25^\circ\text{C}$	75		A	
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	300		A	
I_{AR}	$T_C = 25^\circ\text{C}$	75		A	
E_{AR}	$T_C = 25^\circ\text{C}$	30		mJ	
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 2 \Omega$	5		V/ns	
P_D	$T_C = 25^\circ\text{C}$	300		W	
Symbol	Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)			
		min.	typ.	max.	
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	100			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 4 \text{ mA}$	2.0		4	V
I_{GSS}	$V_{GS} = \pm 20 \text{ V}_{DC}$, $V_{DS} = 0$			± 100	nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$; $T_J = 25^\circ\text{C}$ $V_{GS} = 0 \text{ V}$; $T_J = 125^\circ\text{C}$			250 1	μA mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2\%$			25	m Ω
g_{fs}	$V_{DS} = 10 \text{ V}$; $I_D = I_{D25}$, pulse test	25	30		S
C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$		4500		pF
C_{oss}			1600		pF
C_{rss}			800		pF
$t_{d(on)}$	$V_{GS} = 10 \text{ V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 I_{D25}$ $R_G = 2 \Omega$, (External)		20	30	ns
t_r			60	110	ns
$t_{d(off)}$			80	110	ns
t_f			60	90	ns
$Q_{g(on)}$			180	260	nC
Q_{gs}	$V_{GS} = 10 \text{ V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 I_{D25}$		36	70	nC
Q_{gd}			85	160	nC
R_{thJC}	with heatsink compound (0.42 K/m.K; 50 μm)			0.5	K/W
R_{thCK}			0.25		K/W

Features

- HiPerFET™ technology
 - low $R_{DS(on)}$
 - low gate charge for high frequency operation
 - unclamped inductive switching (UIS) capability
 - dv/dt ruggedness
 - fast intrinsic reverse diode
- ECO-PAC 2 package
 - isolated back surface
 - enlarged creepage towards heatsink
 - application friendly pinout
 - low inductive current path
 - high reliability
 - solderable pins for PCB mounting

Applications

- drives and power supplies
- battery or fuel cell powered
- automotive, industrial vehicle etc.
- secondary side of mains power supplies

IXYS reserves the right to change limits, test conditions and dimensions.

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Source-Drain Diode

Characteristic Values

(T_J = 25°C, unless otherwise specified)

Symbol	Conditions	min.	typ.	max.	
I _S	V _{GS} = 0 V			75	A
I _{SM}	Repetitive;			300	A
V _{SD}	I _F = I _{D25} , V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2%			1.75	V
t _{rr}	I _F = 25 A, -di/dt = 100 A/μs, T _J = 25°C V _R = 25 V T _J = 125°C		300	200	ns ns

Temperature Sensor NTC

Symbol	Conditions	min.	typ.	max.	
R ₂₅	T = 25°C	4.75	5.0	5.25	kΩ
B _{25/50}			3375		K

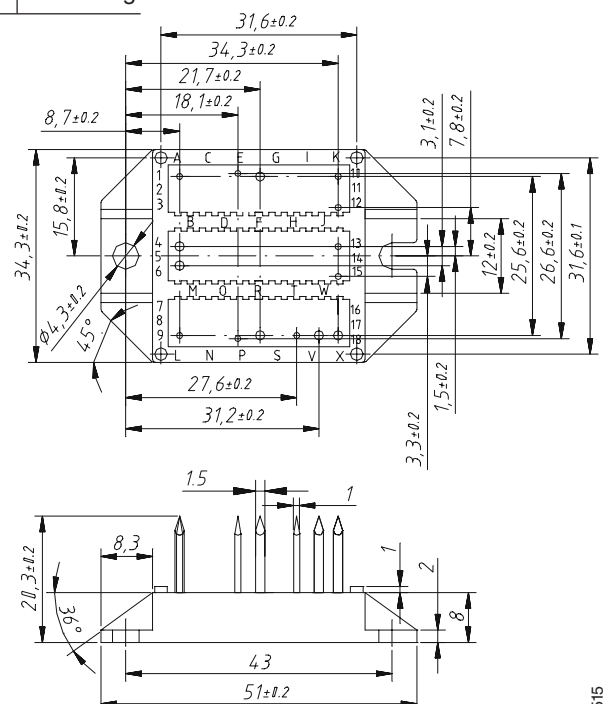
Module

Symbol	Conditions	Maximum Ratings	
T _{VJ}		-40...+150	°C
T _{stg}		-40...+125	°C
V _{ISOL}	I _{ISOL} ≤ 1 mA; 50/60 Hz; t = 1 s	3600	V~
M _d	mounting torque (M4)	1.5 - 2.0 14 - 18	Nm lb.in.
a	Max. allowable acceleration	50	m/s ²

Symbol	Conditions	min.	typ.	max.	
d _s	Creepage distance on surface (Pin to heatsink)	11.2			mm
d _A	Strike distance in air (Pin to heatsink)	11.2			mm
Weight		24			g

Data according to IEC 60747 refer to a single diode or transistor unless otherwise stated

Dimensions in mm (1 mm = 0.0394")



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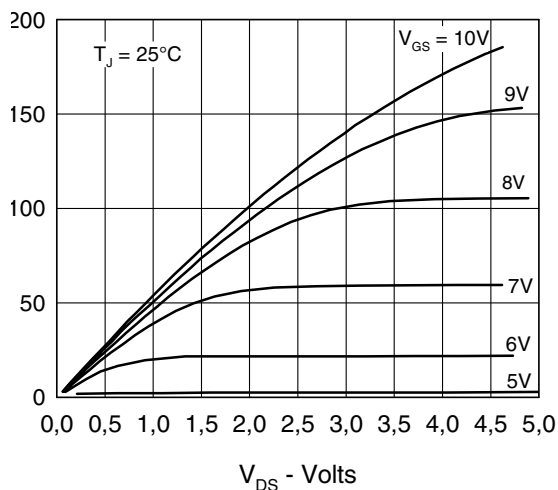


Fig. 1 Output Characteristics

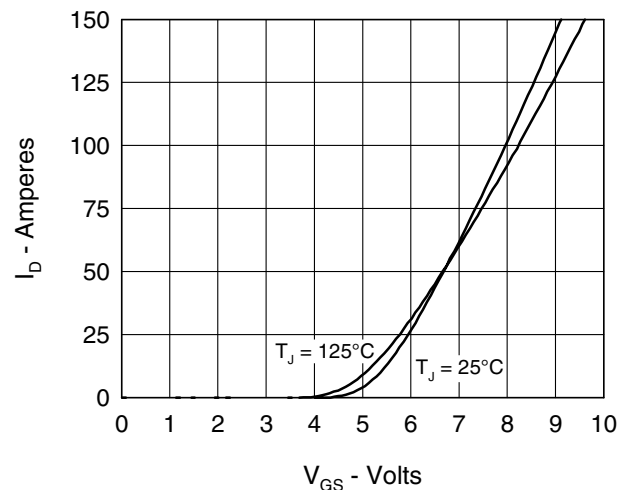


Fig. 2 Input Admittance

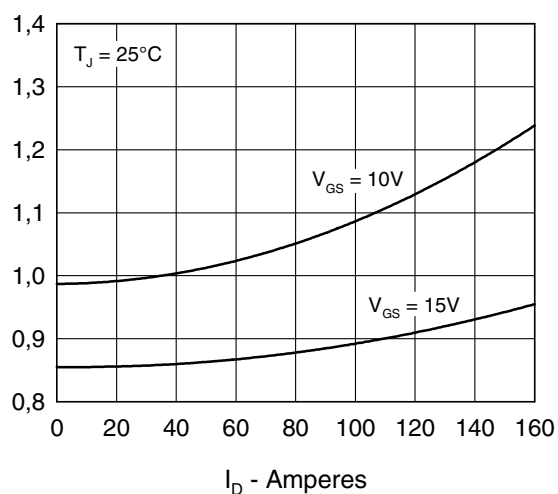


Fig. 3 $R_{DS(on)}$ vs. Drain Current

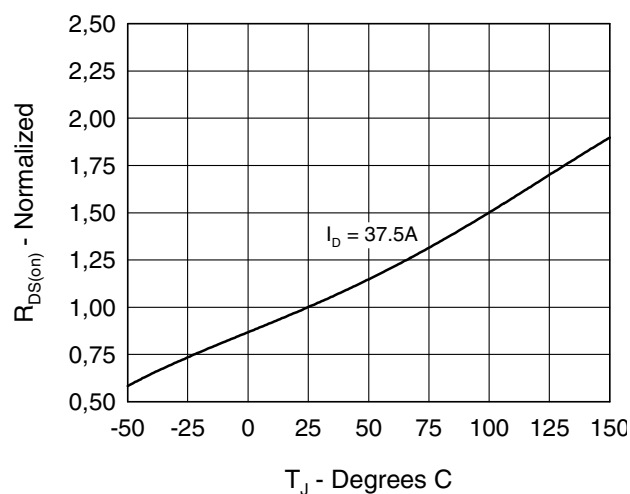


Fig. 4 Temperature Dependence of Drain to Source Resistance

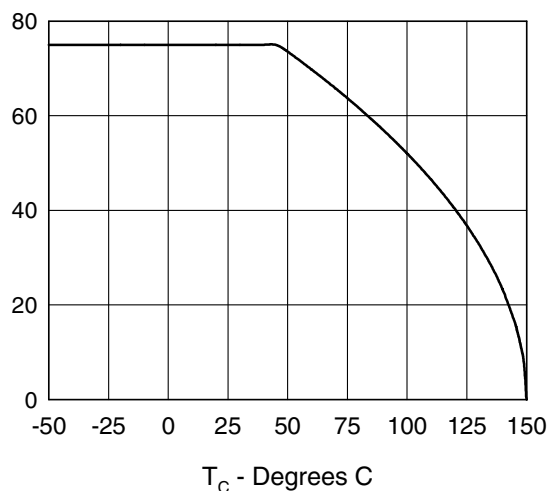


Fig. 5 Drain Current vs. Case Temperature

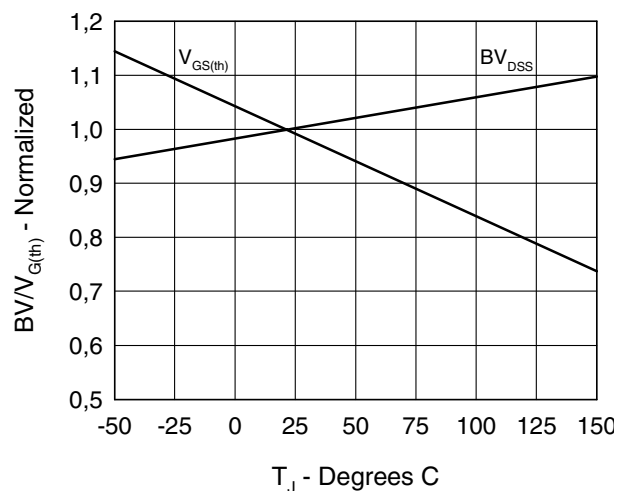


Fig. 6 Temperature Dependence of Breakdown and Threshold Voltage

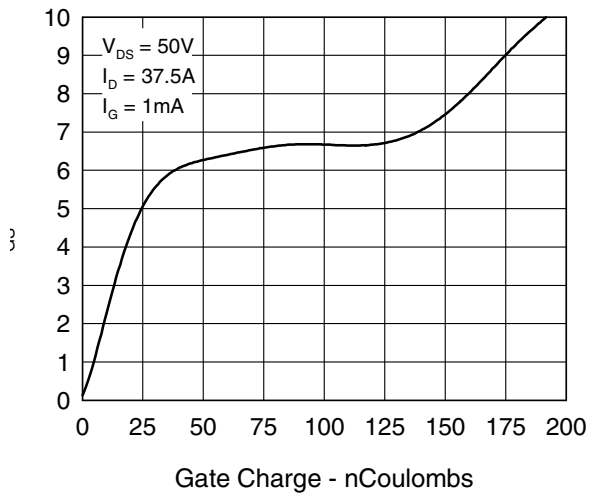


Fig.7 Gate Charge Characteristic Curve

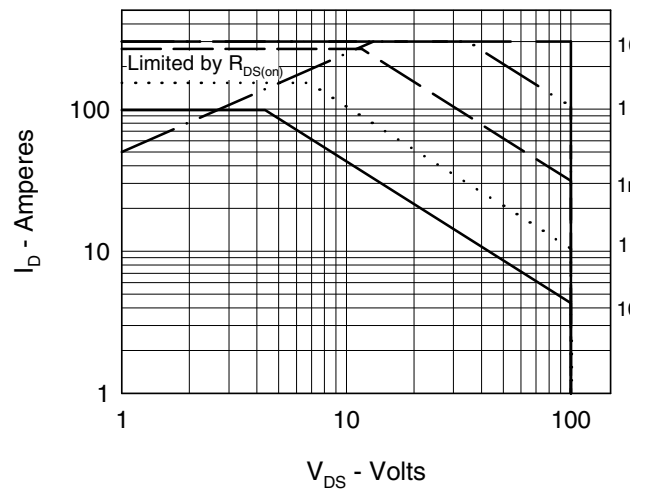


Fig.8 Forward Bias Safe Operating Area

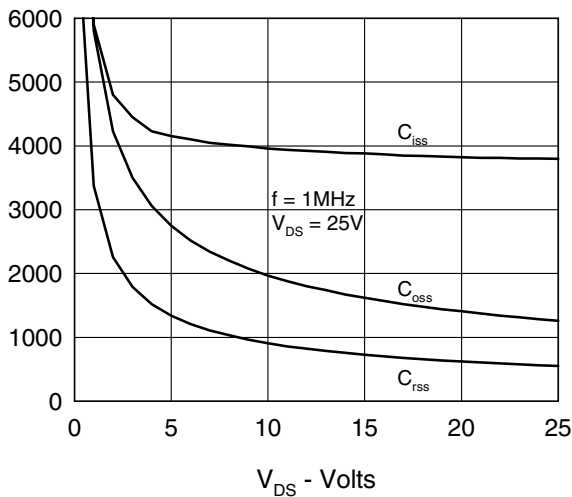


Fig.9 Capacitance Curves

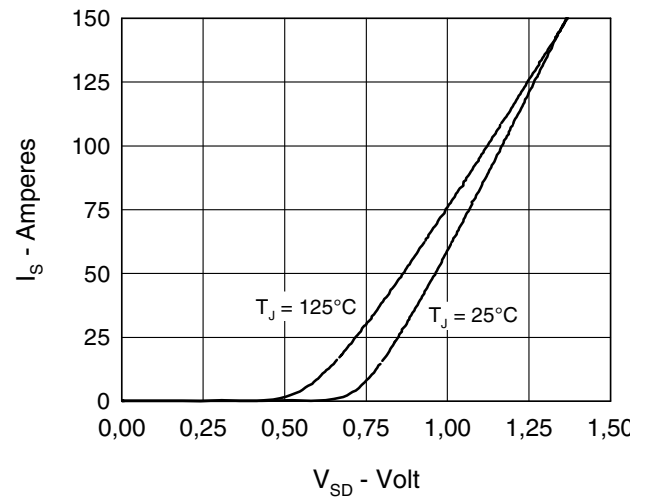


Fig.10 Source Current vs. Source to Drain Voltage

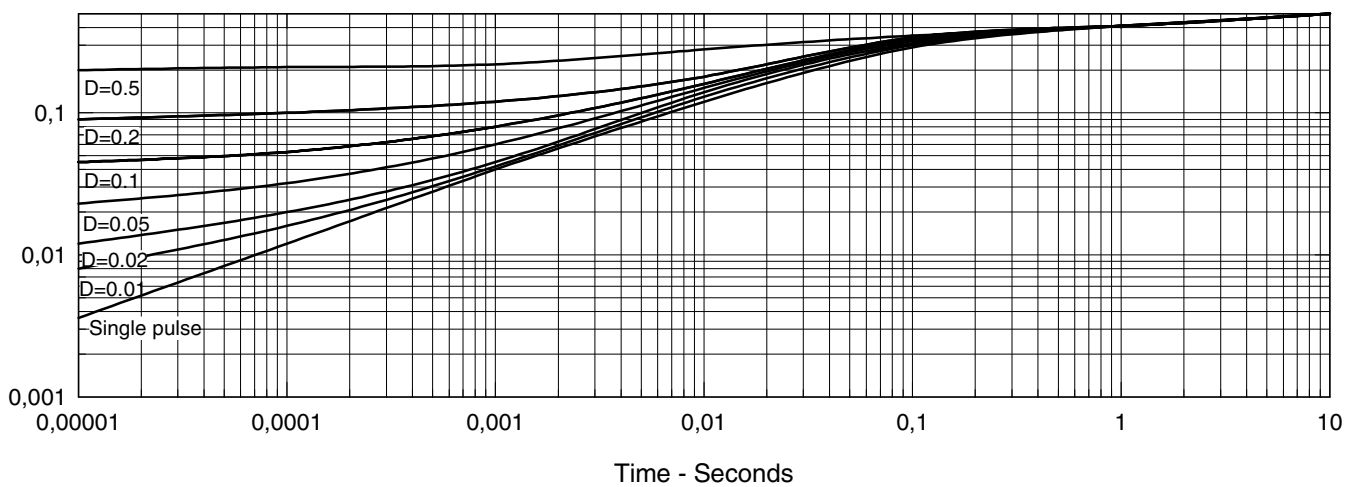


Fig.11 Transient Thermal Impedance