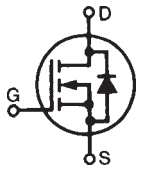
IXYS

Polar™ Power MOSFET HiPerFET™

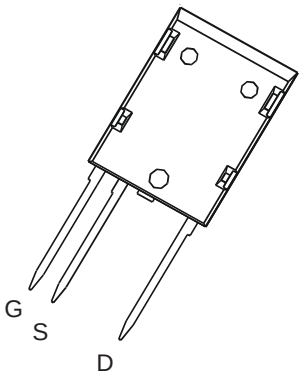
IXFL44N100P

V_{DSS} = 1000V
I_{D25} = 22A
$R_{DS(on)}$ ≤ 240mΩ
t_{rr} ≤ 300ns

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



ISOPLUS i5-Pak™ (HV)



G = Gate
S = Source D = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	1000	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	1000	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	T_C = 25°C	22	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	110	A
I_{AR}	T_C = 25°C	22	A
E_{AS}	T_C = 25°C	2	J
dV/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	15	V/ns
P_D	T_C = 25°C	357	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum lead temperature for soldering	300	°C
T_{SOLD}	Plastic body for 10s	260	°C
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
	$I_{ISOL} \le$ 1mA t = 1s	3000	V~
F_C	Mounting force	40..120/4.5..27	N/lb.
Weight		8	g

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 3mA	1000			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1mA	3.5		6.5	V
I_{GSS}	V_{GS} = ± 30V, V_{DS} = 0V			± 200	nA
I_{DSS}	$V_{DS} = V_{DSS}$			50	μA
	V_{GS} = 0V T_J = 125°C			3	mA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 22A, Note 1			240	mΩ

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Low drain to tab capacitance(<30pF)
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Fast intrinsic Rectifier

Applications

- Switched-mode and resonant-mode power supplies
- DC-DC converters
- Laser Drivers
- AC and DC motor controls
- Robotics and servo controls

Advantages

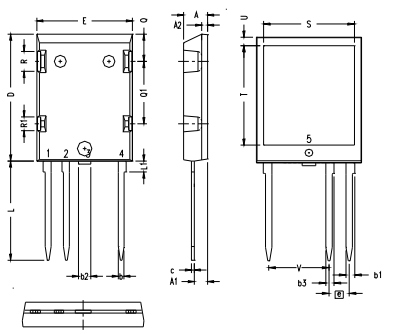
- Easy assembly
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 20V, I_D = 22A, Note 1	20	35		S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		19		nF
C_{oss}			1060		pF
C_{rss}			41		pF
R_{Gi}	Gate input resistance		1.70		Ω
$t_{d(on)}$	**Resistive Switching Times**		60		ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 22A		68		ns
$t_{d(off)}$	R_G = 1Ω (External)		90		ns
t_f			54		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 22A		305		nC
Q_{gs}			104		nC
Q_{gd}			125		nC
R_{thJC}				0.35	°C/W
R_{thCS}			0.15		°C/W

Source-Drain Diode (T_J = 25°C unless otherwise specified)		Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			44	A
I_{SM}	Repetitive, pulse width limited by T_{JM}			176	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			1.5	V
t_{rr}	I_F = 22A, -di/dt = 100A/μs			300	ns
Q_{RM}	V_R = 100V, V_{GS} = 0V		2.5		μC
I_{RM}			17		A

Note 1: Pulse test, t ≤ 300μs; duty cycle, d ≤ 2%.

ISOPLUS i5-Pak™ HV (IXFL) Outline



Note: Bottom heatsink meets 2500 Vrms isolation to the other pins.

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.055	1.17	1.40
b	.045	.055	1.14	1.40
b1	.063	.072	1.60	1.83
b2	.100	.110	2.54	2.79
b3	.058	.068	1.47	1.73
c	.020	.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
L	.780	.820	19.81	20.83
L1	.080	.102	2.03	2.59
Q	.210	.235	5.33	5.97
Q1	.490	.513	12.45	13.03
R	.150	.180	3.81	4.57
R1	.100	.130	2.54	3.30
S	.668	.690	16.97	17.53
T	.801	.821	20.34	20.85
U	.065	.080	1.65	2.03
V	.440	.460	11.18	11.68

Fig. 1. Output Characteristics @ 25ºC

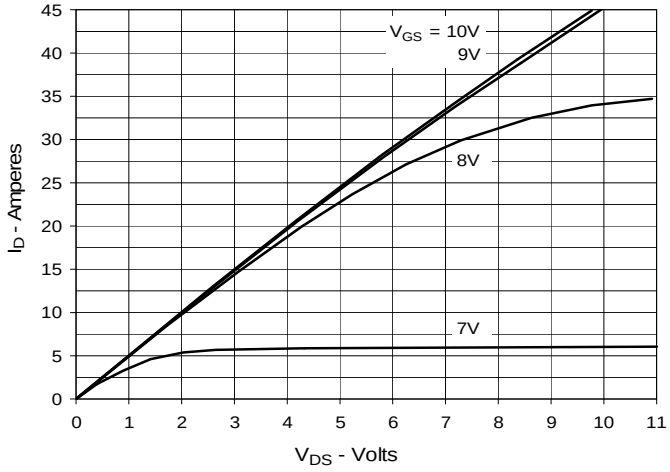


Fig. 2. Extended Output Characteristics @ 25ºC

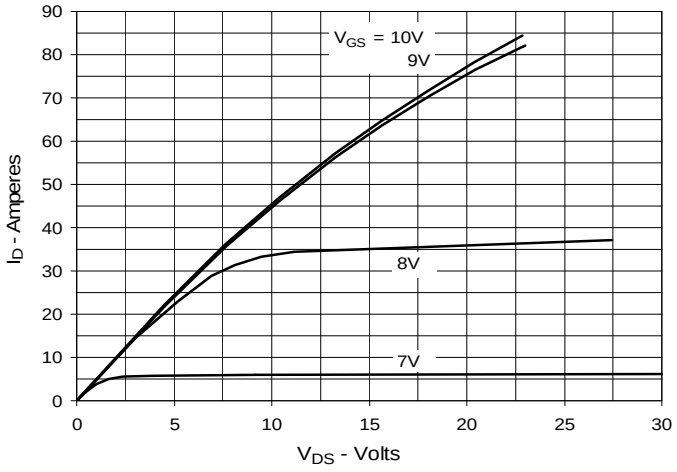


Fig. 3. Output Characteristics @ 125ºC

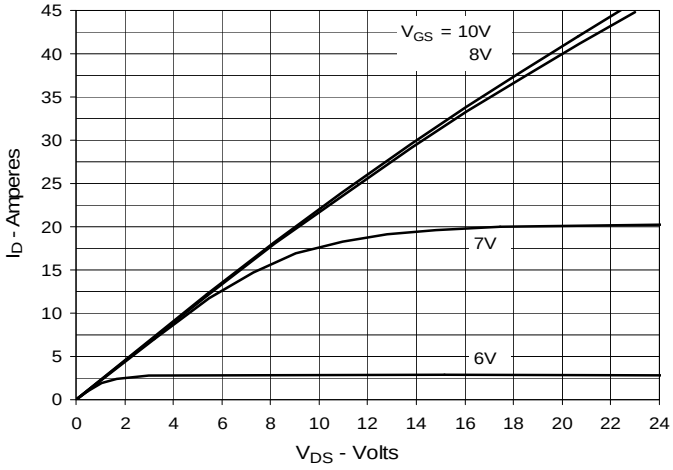


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 22A Value vs. Junction Temperature

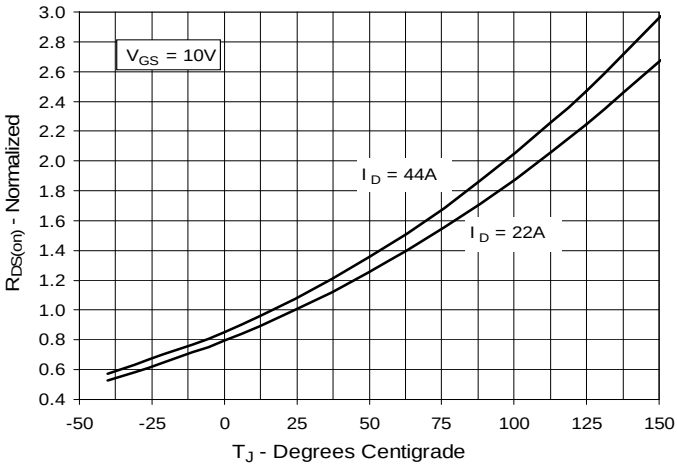


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 22A Value vs. Drain Current

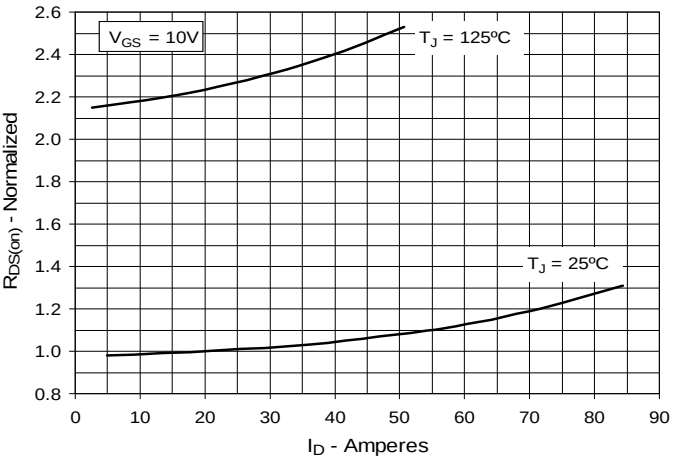


Fig. 6. Maximum Drain Current vs. Case Temperature

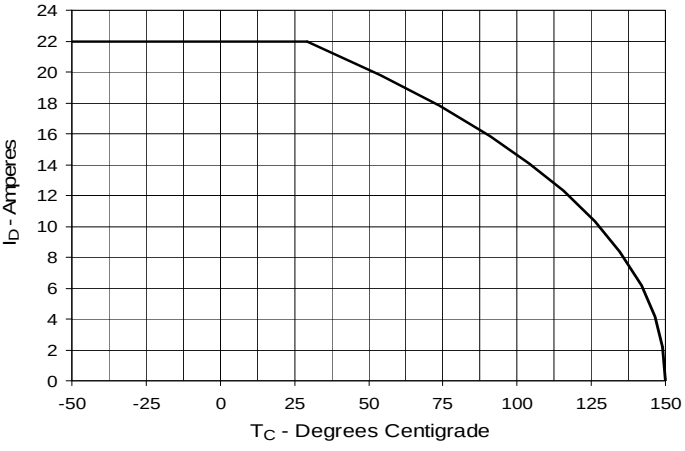


Fig. 7. Input Admittance

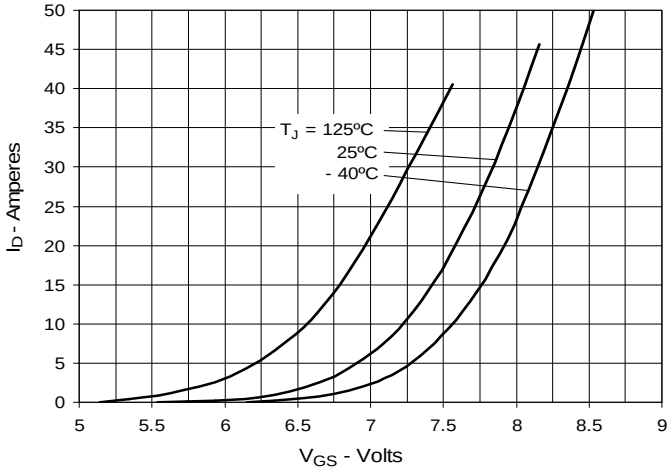


Fig. 8. Transconductance

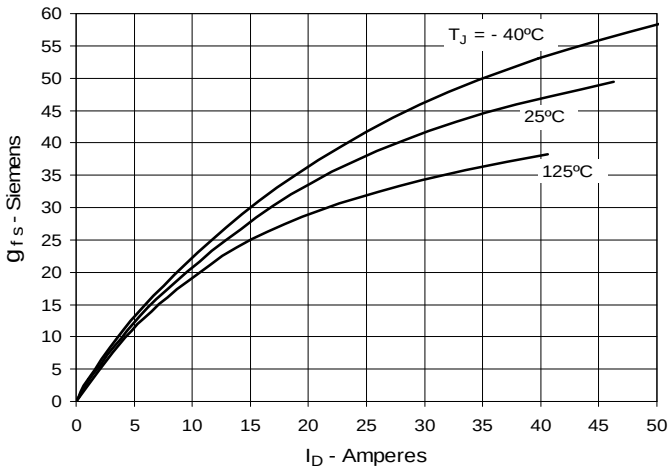


Fig. 9. Forward Voltage Drop of Intrinsic Diode

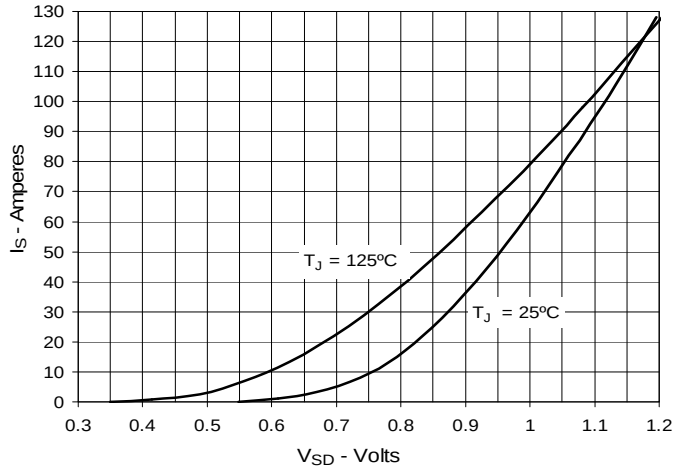


Fig. 10. Gate Charge

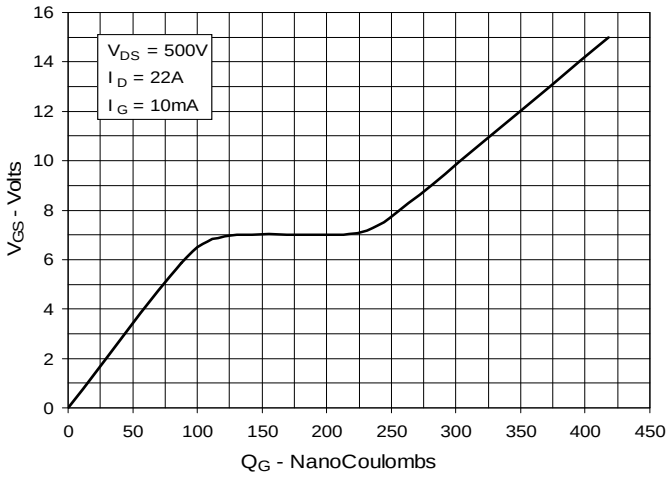


Fig. 11. Capacitance

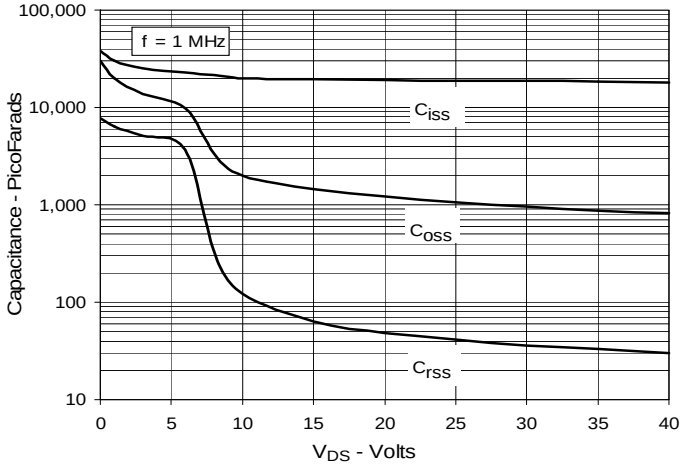


Fig. 12. Maximum Transient Thermal Impedance