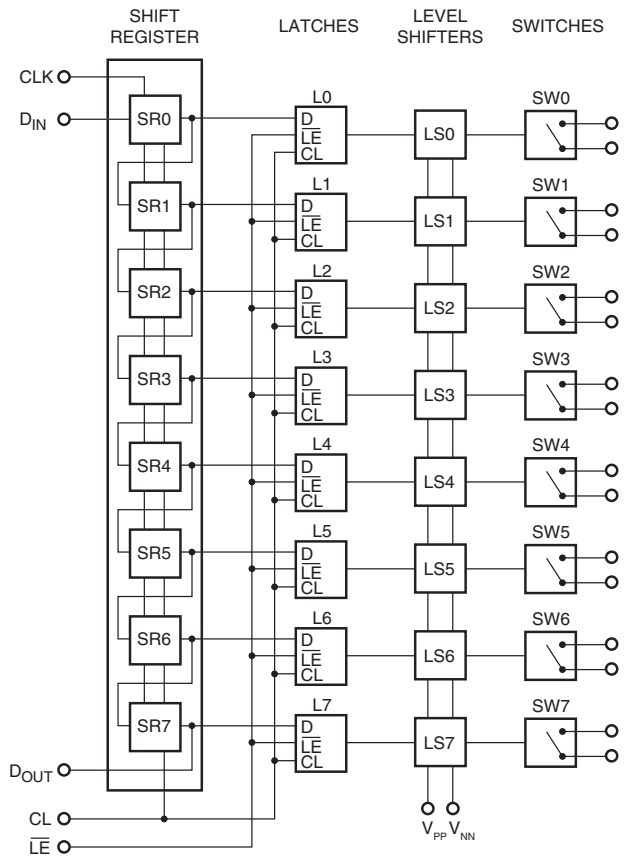
CPC7220
Low Charge Injection, 8-Channel High Voltage Analog Switch

Features
- Processed with BCDMOS on SOI (Silicon On Insulator)
- Flexible High Voltage Supplies up to V_{PP}-V_{NN}=200V
- DC to 10MHz Analog Signal Frequency
- -60dB Minimum Output-Off Isolation at 5MHz
- Low Quiescent Power Dissipation (< 1µA typical)
- Output On-Resistance Typically 20Ω
- TTL I/O's for 3.3V Interface
- Adjustable High Voltage Supplies
- Surface Mount Package

Applications
- Ultrasound Imaging
- Printers
- Industrial Controls and Measurement
- Piezoelectric Transducer Drivers

Figure 1. Block Diagram



Description
The CPC7220 is a low charge injection 8-channel high-voltage analog switch integrated circuit (IC) for use in applications requiring high voltage switching. Control of the high voltage switching is via low voltage TTL logic level compatible inputs for direct connectivity to the system controller.

Switch manipulation is managed by an 8-bit serial to parallel shift register whose outputs are buffered and stored by an 8-bit transparent latch. Level shifters buffer the latch outputs and operate the high voltage switches.

Because the CPC7220 is capable of switching high load voltages and has a flexible load voltage range, e.g. V_{PP}/V_{NN} : +40V/-160V or +100V/-100V, it is well suited for many medical and industrial applications such as medical ultrasound imaging, printers, and industrial measurement equipment.

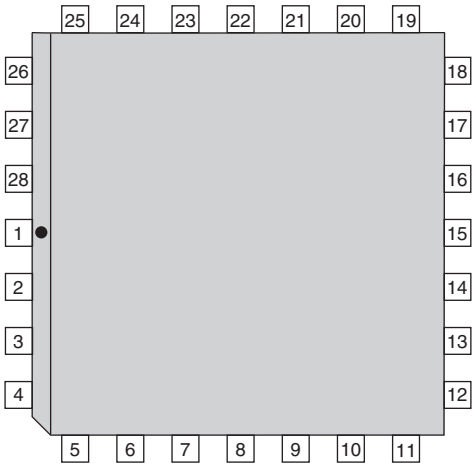
Construction of the high voltage switches using Clare's reliable BCDMOS process technology on SOI (Silicon On Insulator) allow the switches to be organized as solid state switches with direct gate drive.

Ordering Information

Part Number	Description
CPC7220W	28-Lead PLCC in Tubes (37/Tube)
CPC7220WTR	28-Lead PLCC Tape & Reel (500/Reel)
CPC7220K	48-Lead LQFP in Trays (250/Tray)
CPC7220KTR	48-Lead LQFP Tape & Reel (1000/Reel)

1. Specifications

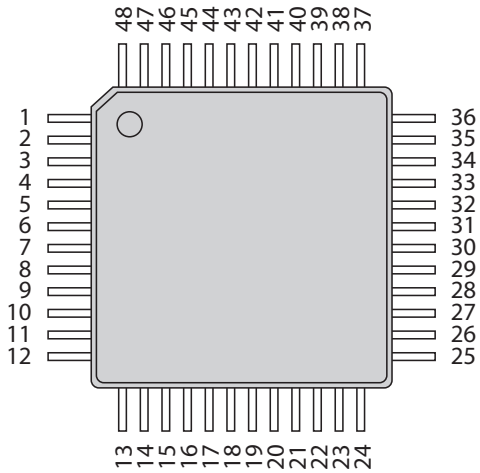
1.1 Package Pinout, PLCC-28



1.2 Pin Description

Pin	Name	Description
1	SW3	SW3 Output
2	SW3	SW3 Output
3	SW2	SW2 Output
4	SW2	SW2 Output
5	SW1	SW1 Output
6	SW1	SW1 Output
7	SW0	SW0 Output
8	SW0	SW0 Output
10	V_{PP}	Switch Positive High Voltage Supply
12	V_{NN}	Switch Negative High Voltage Supply
13	GND	Ground
14	V_{DD}	Logic Positive Voltage Supply
16	D_{IN}	Serial Data Input
17	CLK	Clock Input, Positive Edge Trigger
18	$\overline{LE}$	Latch Enable, Active Low
19	CL	Latch Clear, Active High Clears Latches And Opens Switches
20	D_{OUT}	Serial Data Output
21	SW7	SW7 Output
22	SW7	SW7 Output
23	SW6	SW6 Output
24	SW6	SW6 Output
25	SW5	SW5 Output
26	SW5	SW5 Output
27	SW4	SW4 Output
28	SW4	SW4 Output
9, 11, 15	N/C	No Connection

1.3 Package Pinout, LQFP-48



1.4 Pin Description

Pin	Name	Description
1	SW5	SW5 Output
3	SW4	SW4 Output
5	SW4	SW4 Output
8	SW3	SW3 Output
10	SW3	SW3 Output
12	SW2	SW2 Output
14	SW2	SW2 Output
16	SW1	SW1 Output
18	SW1	SW1 Output
20	SW0	SW0 Output
22	SW0	SW0 Output
24	V_{PP}	Switch Positive High Voltage Supply
25	V_{NN}	Switch Negative High Voltage Supply
28	GND	Ground
29	V_{DD}	Logic Positive Supply Voltage
33	D_{IN}	Serial Data Input
34	CLK	Clock Input, Positive Edge Trigger
35	$\overline{LE}$	Latch Enable, Active Low
36	CL	Latch Clear, Active High Clears Latches And Opens Switches
37	D_{OUT}	Serial Data Output
39	SW7	SW7 Output
41	SW7	SW7 Output
43	SW6	SW6 Output
45	SW6	SW6 Output
47	SW5	SW5 Output
2, 4, 6, 7, 9, 11, 13, 15, 17, 19, 21, 23, 26, 27, 30, 31, 32, 38, 40, 42, 44, 46, 48	N/C	No Connection

1.5 Absolute Maximum Ratings

Absolute maximum electrical ratings are at 25°C.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Parameter	Min	Max	Units
V_{DD} Logic Power Supply Voltage	-0.5	6	V
V_{PP} - V_{NN} Supply Voltage	-	220	V
V_{PP} Positive High Voltage Supply	-0.5	V_{NN}+200	V
V_{NN} Negative High Voltage Supply	+0.5	V_{PP}-200	V
Logic input voltages	-0.5	V_{DD}+0.3	V
Analog signal range	V_{NN}	V_{PP}	V
Peak analog signal current per channel	-	1	A
Power dissipation			W
28-Lead PLCC	-	2.5	
48-Lead LQFP	-	2.3	
Thermal Resistance, Junction to Ambient			°C/W
28-Lead PLCC	-	50	
48-Lead LQFP	-	53	
Storage temperature	-60	+150	°C

1.6 Operating Conditions

Parameter	Symbol	Value
Logic power supply voltage [1, 3]	V_{DD}	4.5V to 6V
Positive high voltage supply [1, 3]	V_{PP}	40V to V_{NN} + 200V
Negative high voltage supply [1, 3]	V_{NN}	-40V to -160V
Analog signal voltage, peak-to-peak [2]	V_{SIG}	V_{NN}+10V to V_{PP}-10V
Operating temperature	T_A	0°C to 70°C

[1] Power up/down sequence is arbitrary except that GND must be powered-up first and powered-down last.

[2] V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.

[3] Rise and fall times of power supplies, V_{DD} , V_{PP} , and V_{NN} , should not be less than 1ms.

1.7 Electrical Characteristics

1.7.1 Switch Characteristics (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	0°C		+25°C			+70°C		Units
			min	max	min	typ	max	min	max	
Small Signal Switch On-Resistance	R_{ONS}	V_{PP}=40V, V_{NN}=-160V, I_{SW}=5mA	-	30	-	20	38	-	48	Ω
		V_{PP}=40V, V_{NN}=-160V, I_{SW}=200mA	-	25	-	-	27	-	32	
		V_{PP}=100V, V_{NN}=-100V, I_{SW}=5mA	-	25	-	20	27	-	33	
		V_{PP}=100V, V_{NN}=-100V, I_{SW}=200mA	-	18	-	15	24	-	27	
		V_{PP}=160V, V_{NN}=-40V, I_{SW}=5mA	-	23	-	20	25	-	30	
		V_{PP}=160V, V_{NN}=-40V, I_{SW}=200mA	-	22	-	-	25	-	27	
Small Signal Switch On-Resistance Matching	ΔR_{ONS}	I_{SW}=5mA, V_{PP}=100V, V_{NN}=-100V	-	20	-	4	20	-	20	%
Large Signal Switch On-resistance	R_{ONL}	V_{SIG}=V_{PP}-10V, I_{SIG}=0.8A	-	-	-	16	-	-	-	Ω
Switch Off Leakage Per Switch	I_{SOL}	V_{SIG}=V_{PP}-10V and V_{NN}+10V	-	5	-	0.4	10	-	15	µA
DC Offset, Switch Off	-	R_L=100kΩ	-	100	-	0.2	100	-	100	mV
DC Offset, Switch On	-	R_L=100kΩ	-	100	-	0.2	100	-	100	
Switch Output Peak Current	-	V_{SIG} duty cycle = 0.1%	-	-	-	-	0.8	-	-	A
Output Switch Frequency	f_{SW}	Duty cycle = 50%	-	-	-	-	50	-	-	kHz
Maximum V_{SIG} Slew Rate	dV/dt	V_{PP}=160V, V_{NN}=-40V	-	20	-	-	20	-	20	V/ns
		V_{PP}=100V, V_{NN}=-100V								
		V_{PP}=40V, V_{NN}=-160V								
Off Isolation	K_O	f=5MHz, 1kΩ/15pF load	-30	-	-30	-	-	-30	-	dB
		f=5MHz, 50Ω load	-58	-	-58	-	-	-58	-	
Switch Crosstalk	K_{CR}	f=5MHz, 50Ω load	-60	-	-60	-	-	-60	-	dB
Output Switch Isolation Diode Current	I_{ID}	300ns pulse width, 2.0% duty cycle	-	300	-	-	300	-	300	mA
Off Capacitance, SW to GND	$C_{SG(OFF)}$	V_{SW}=0V, 1MHz	5	17	5	-	25	5	20	pF
On Capacitance, SW to GND	$C_{SG(ON)}$	V_{SW}=0V, 1MHz	25	40	20	-	40	25	50	
Output Voltage Spike	$+V_{SPK}$	V_{PP}=40V, V_{NN}=-160V, R_L=50Ω	-	-	-	37	150	-	-	mV
	$-V_{SPK}$					93				
	$+V_{SPK}$	V_{PP}=100V, V_{NN}=-100V, R_L=50Ω	-	-	-	35	150	-	-	
	$-V_{SPK}$					80				
	$+V_{SPK}$	V_{PP}=160V, V_{NN}=-40V, R_L=50Ω	-	-	-	46	150	-	-	
	$-V_{SPK}$					72				
Charge Injection	Q	V_{PP}=100V, V_{NN}=-100V, V_{SIG}=0V			-	880	-			pC

1.7.2 Logic DC Characteristics (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	0°C		+25°C			+70°C		Units
			min	max	min	typ	max	min	max	
D_{OUT} Source Capability	V_{OH}	I_{OUT}= - 400µA	-	-	V_{DD}-0.7	V_{DD}-0.1	-	-	-	V
D_{OUT} Sink Capability	V_{OL}	I_{OUT}= +400µA	-	-	-	0.04	0.7	-	-	
Logic Input Capacitance	C_{IN}	-	-	10	-	-	10	-	10	pF
Logic Input High	V_{IH}	4.75V < V_{DD} < 5.25V	2	-	2	-	-	2	-	V
Logic Input Low	V_{IL}	4.75V < V_{DD} < 5.25V	-	0.8	-	-	0.8	-	0.8	

1.7.3 Logic Timing Characteristics (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	0°C		+25°C			70°C		Units
			min	max	min	typ	max	min	max	
Setup Time Before $\overline{LE}$ Rises	t_{SD}	-	150	-	150	-	-	150	-	ns
Time Width of $\overline{LE}$	t_{WLE}	-	150	-	150	-	-	150	-	
Clock Delay Time to Data Out	t_{DO}	-	-	150	-	62	150	-	150	
Time Width of CL	t_{WCL}	-	150	-	150	-	-	150	-	
Setup Time, Data to Clock	t_{SU}	-	15	-	15	8	-	20	-	
Hold Time, Data from Clock	t_H	-	35	-	35	-	-	35	-	
Clock Frequency	f_{CLK}	50% duty cycle, f_{DATA}=f_{CLK}/2	-	5	-	-	5	-	5	MHz
Clock Rise and Fall Times	t_R, t_F	-	-	50	-	-	50	-	50	ns
Turn-On Time	t_{ON}	V_{SIG}=V_{PP}-10V, RL=10kΩ	-	5	-	2	5	-	5	µs
Turn-Off Time	t_{OFF}					3				

1.7.4 Supply DC Characteristics (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		0°C		+25°C			+70°C		Units
				min	max	min	typ	max	min	max	
V_{PP} Quiescent Supply Current	I_{PPQ}	All Switches OFF		-	-	-	0.1	10	-	-	µA
		All Switches ON, I_{SW}=5mA									
V_{NN} Quiescent Supply Current	I_{NNQ}	All Switches OFF		-	-	-	-0.1	-10	-	-	
		All Switches ON, I_{SW}=5mA									
V_{PP} Operating Supply Current	I_{PP}	V_{PP}=40V, V_{NN}=-160V	50kHz Output Switching Frequency with No Load	-	6.5	-	-	7	-	8	mA
		V_{PP}=100V, V_{NN}=-100V		-	5	-	-	5.5	-	5.5	
		V_{PP}=160V, V_{NN}=-40V		-	5	-	-	5	-	5.5	
V_{NN} Operating Supply Current	I_{NN}	V_{PP}=40V, V_{NN}=-160V	50kHz Output Switching Frequency with No Load	-	6.5	-	-	7	-	8	mA
		V_{PP}=100V, V_{NN}=-100V		-	5	-	-	5.5	-	5.5	
		V_{PP}=160V, V_{NN}=-40V		-	5	-	-	5	-	5.5	
V_{DD} Average Supply Current	I_{DD}	f_{CLK}=5MHz, V_{DD}=5V		-	4	-	-	4	-	4	mA
V_{DD} Quiescent Supply Current	I_{DDQ}	-		-	10	-	0.03	10	-	10	µA

2. Functional Description

The CPC7220 takes a serial stream of input data along with a synchronous clock signal. As the clock transits from low to high, the data at the input of each shift register is shifted through from SR(n) to SR(n+1). A high data bit, a "1," represents an ON switch; a low data bit, a "0," represents an OFF switch. Data is input and shifted through the internal shift register until all eight shift register positions, SR0 through SR7, are in the desired state.

DIN: The data-in line presents data bits to be shifted through the internal shift register.

CLK: The clock signal's rising edge is associated only with shifting data into and through the shift register.

CL: The clear line overrides all other inputs. When CL is high, the shift register is cleared to all 0s and all latches are set low, which causes all output switches to be turned OFF immediately. When CL is low, all output switches remain in whatever state they are in, ON or OFF, in response to CLK, latch inputs, and the LE signal.

LE: latch enable controls the state of the latches and thus the state of the eight switches. If LE is high, then the latches do not change states, but retain their most recent status: either ON or OFF. With LE high, input data and CLK have no effect on the state of the output switches. If LE is low, then all latch outputs and their switch states follow the inputs from the shift register. LE is overridden by CL: regardless of LE's state, CL clears the latches. See **"Truth Table" on page 10**.

DOUT: The data-out pin is the output of SR7. After eight clock pulses, the first bit of eight input data bits is shifted to SR7 and appears on DOUT.

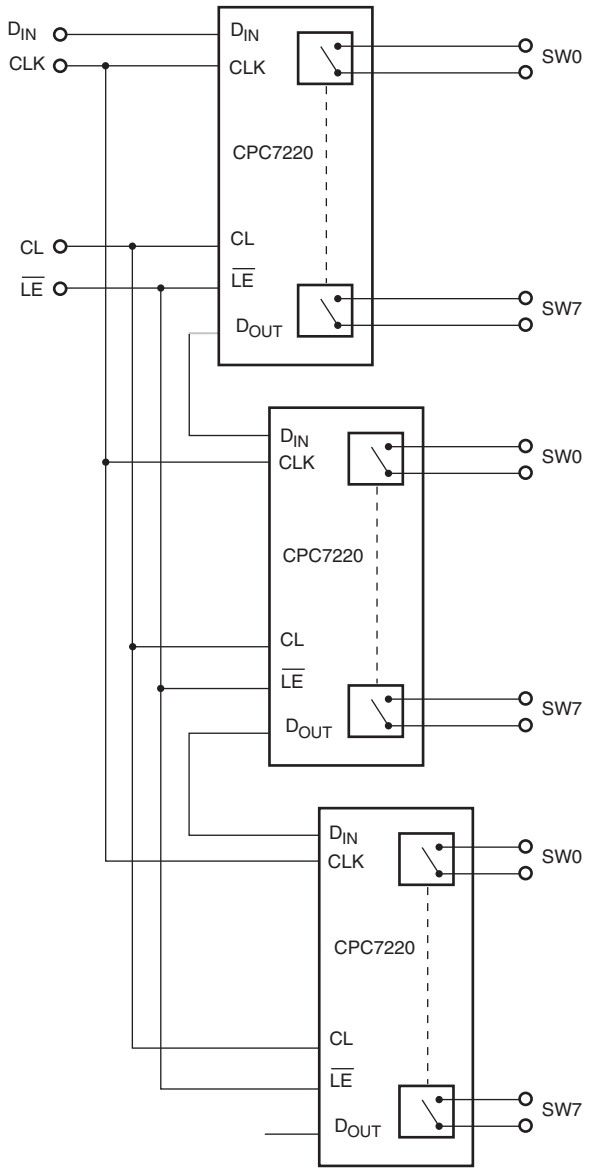
SW0 - SW7: The CPC7220 provides eight high-voltage SPST output switches with a typical on-resistance of 20Ω The two connections of each switch are not polarity-sensitive.

V_{PP} and V_{NN}: Voltage inputs to the level shifters for each switch channel that translate the voltage level of the latch output signals to an appropriate level for the voltages being switched.

The high-voltage output switches are turned on and off in response to the data sent into the latches from the shift register: data 0 turns a switch OFF, data 1 turns a switch ON.

Two or more CPC7220 devices can be cascaded to form an n-switch arrangement. The DOUT pin of the first is connected to the DIN pin of the next in the series. All devices are connected to the same clock (CLK) signal. LE of all devices would normally be connected, as would CL, but this is not necessary.

The first data bit applied to DIN of the CPC7220, whether it's a single device or several cascaded devices, ripples through to the last switch output in line after the application of a full clocking sequence of 8 clock pulses per CPC7220. Setting the serial I/O device to output the most significant bit (MSB) first, results in the MSB appearing on SW7 of the last device in line after a full clocking sequence..



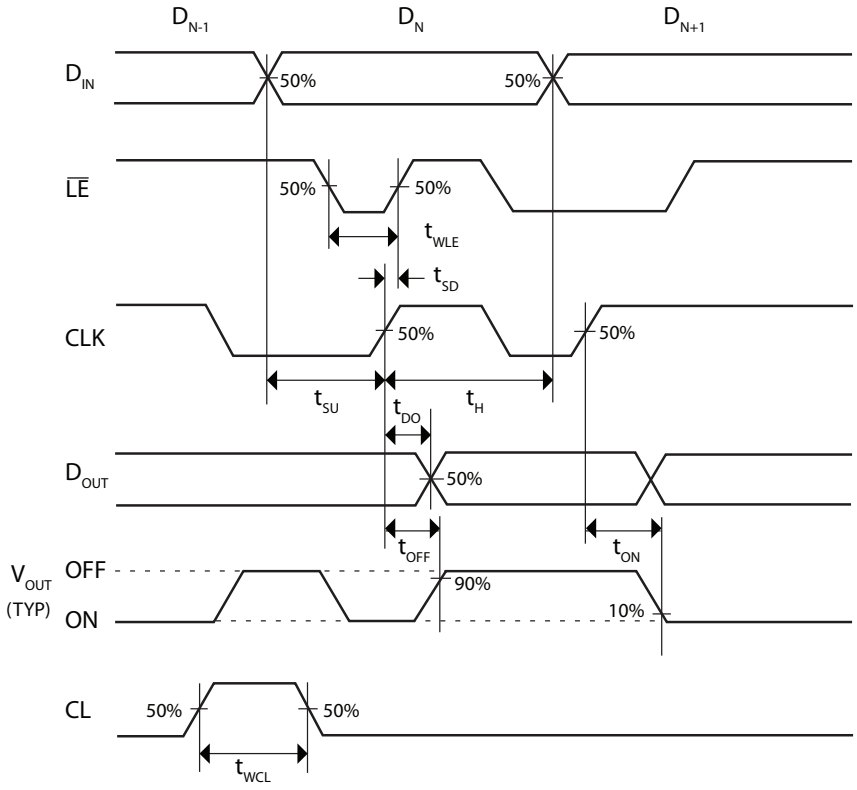
2.1 Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the rising edge of the CLK signal.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.
6. The clear input overrides all other inputs.

2.2 Logic Timing Waveforms

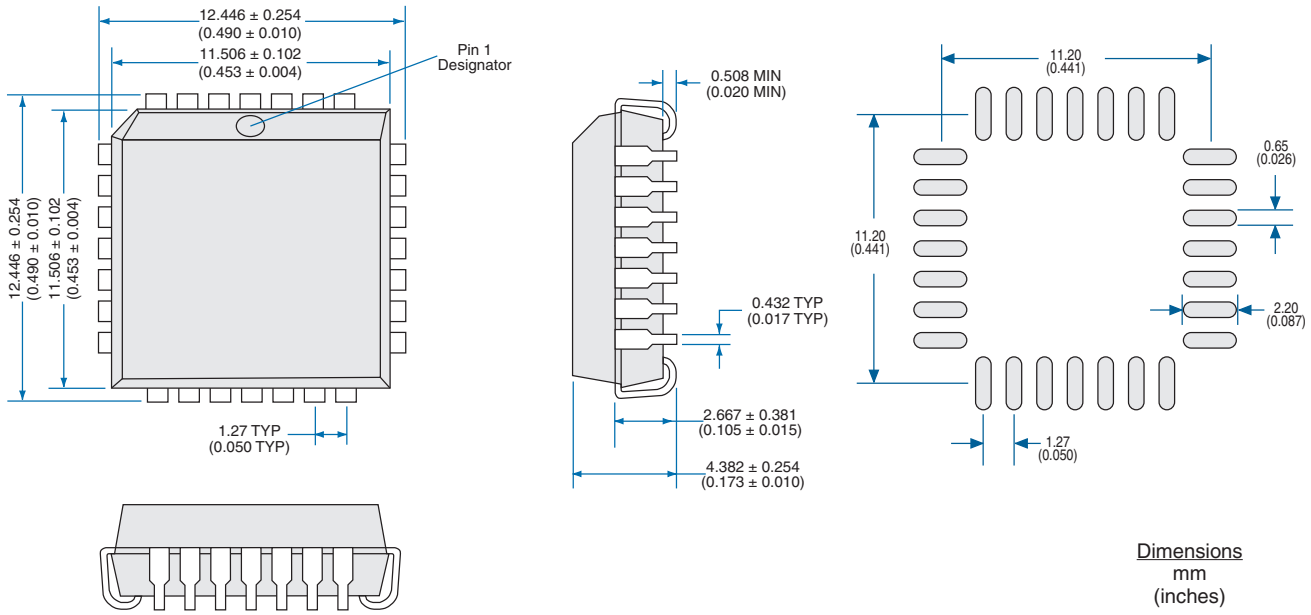


3. Manufacturing Information

3.1 Mechanical Dimensions

3.1.1 28-Pin PLCC Package

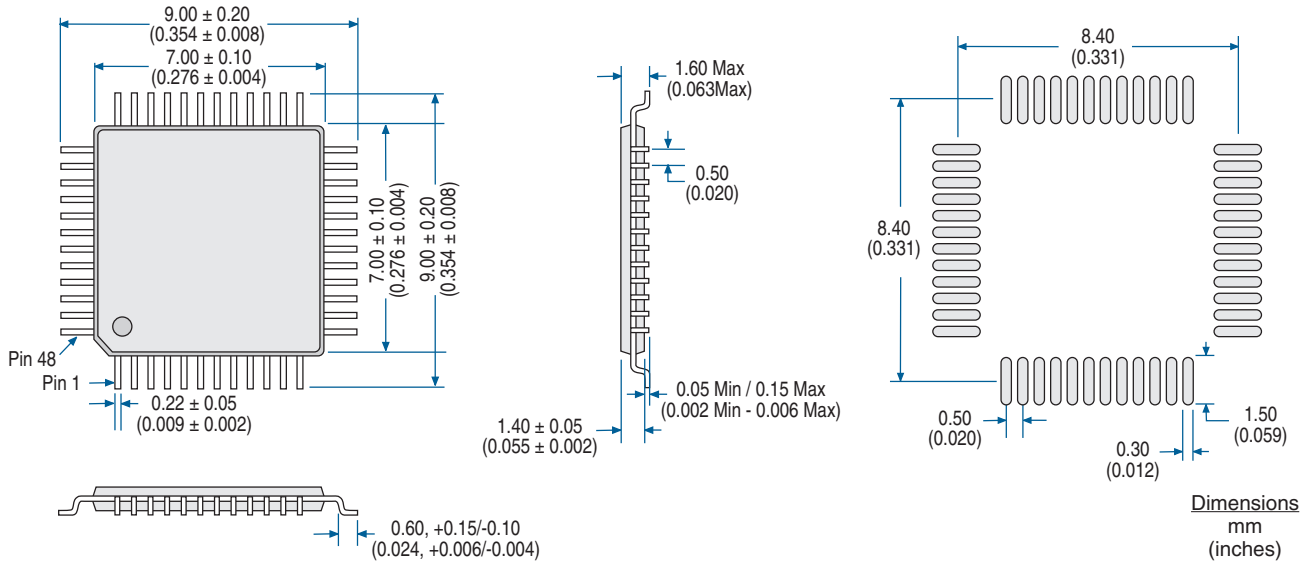
Recommended PCB Land Pattern



Dimensions
mm
(inches)

3.1.2 48-Pin LQFP Package

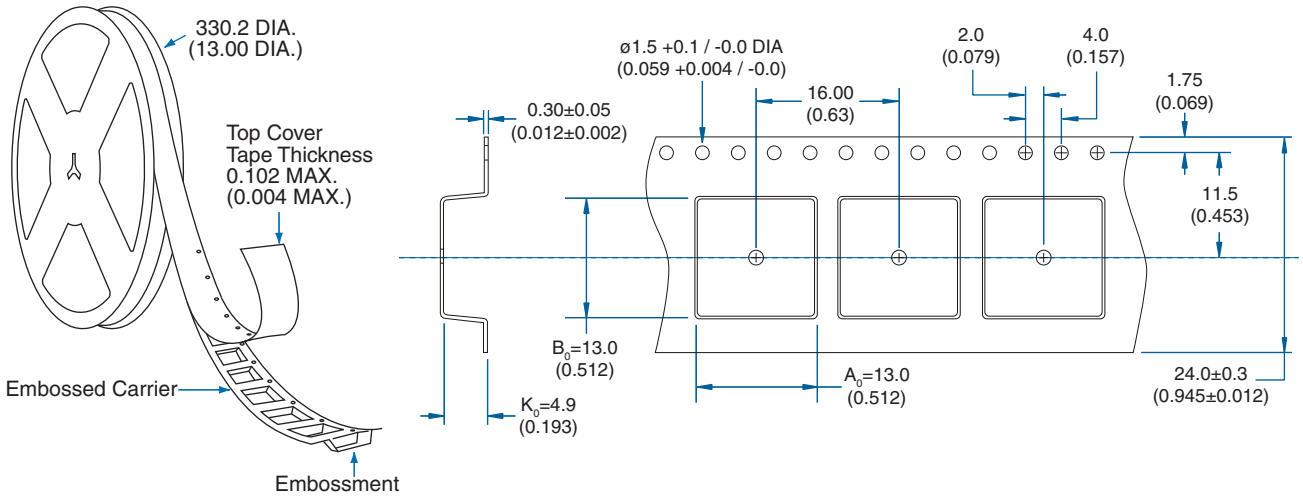
Recommended PCB Land Pattern



Dimensions
mm
(inches)

3.2 Tape and Reel Specifications

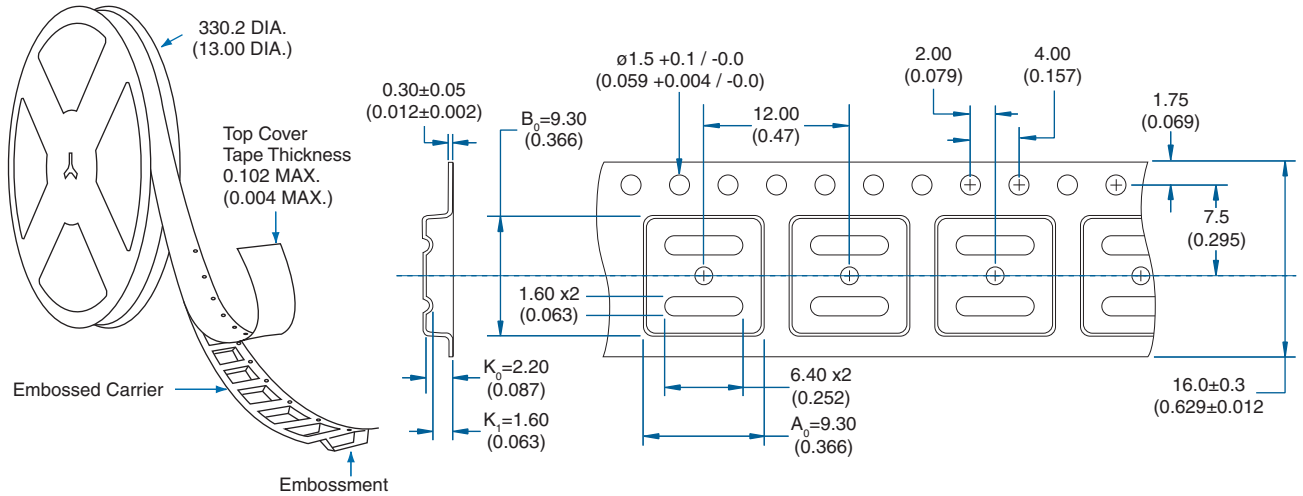
3.2.1 PLCC-28



NOTES:
1. 10 sprocket hole pitch cumulative tolerance ±0.2 (0.008)
2. Camber not to exceed 1mm in 100mm
3. Material: conductive black polystyrene
4. A_0 and B_0 measured on a plane 0.3mm above the bottom of the pocket
5. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole
7. Unless otherwise noted, tolerance ±0.1 (0.004)

Dimensions
mm
(inches)

3.2.2 LQFP-48



NOTES:
1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole
4. Unless otherwise specified, tolerance ±0.1 (0.004)

Dimensions
mm
(inches)

3.3 Soldering

For proper assembly, the component must be processed in accordance with the current revision of IPC/JEDEC standard, J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

3.4 Washing

Clare does not recommend ultrasonic cleaning of this part.

For additional information please visit www.clare.com

Specification: DS-DS-CPC7220-R00J

11/30/09