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Z86230

ADVANCED PROGRAM BLOCKING AND NTSC LINE 21 XDS DECODER

PRELIMINARY PRODUCT SPECIFICATION

PS000401-TVC0699

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1. ARCHITECTURAL OVERVIEW

The Z86230 is a stand-alone integrated circuit, capable of processing Extended Data Services (XDS) in Field 2 of the Vertical Blanking Interval (VBI) of a video frame. This device conforms to the transmission format defined in the Television Decoder Circuits Act of 1990, in accordance with the Electronics Industry Association specification EIA-608A and EIA-744A.

The XDS data is processed to provide either a Program Blocking signal (PB) or a recovered XDS data packet. The PB matches the contents of the recovered Content Advisory packet to the user selections input on the decoder. On-chip XDS filters in the Z86230 are fully-programmable, enabling recovery of only those XDS data packets selected for use in TVs, VCRs, and Set-Top boxes.

In addition, the Z86230 is ideally suited to monitor Picture-In-Picture (PiP) window video for violence blocking and other XDS data services.

Highlights of the Z86230 include:

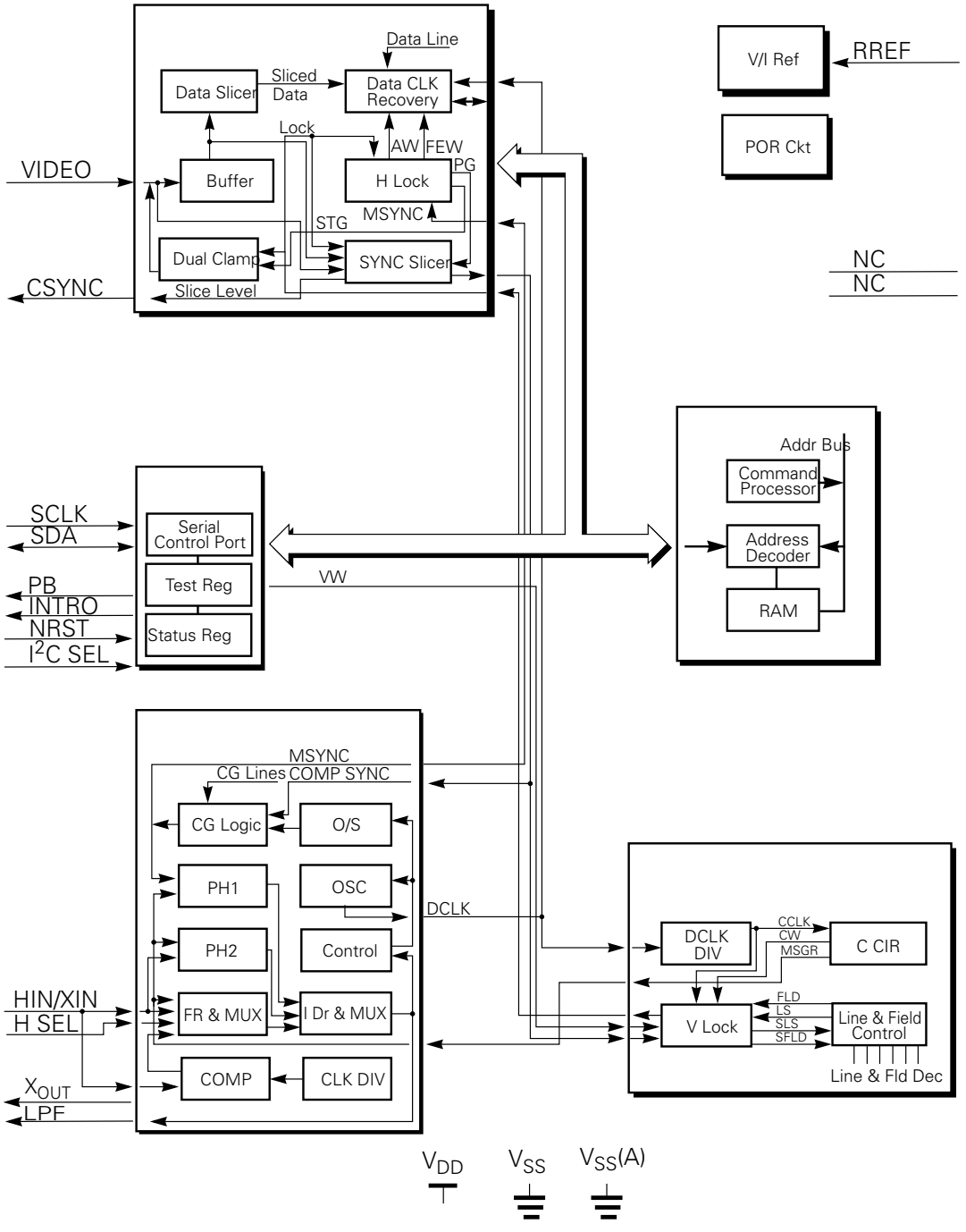
1. A stand-alone Line 21 Decoder for Extended Data Services (XDS).
2. Extractable XDS data from the input video.
3. Full output of a selectable V-Chip Program Blocking signal (PB).
4. Selectable XDS filter parameters from a list of preprogrammed values.
5. Minimal communications and control overhead that provides simple implementation of Violence Blocking and Auto Clock Set Features.
6. Full output of the recovered XDS data through the I^2C serial communication port.
7. Two different slave addresses that are selectable in the I^2C serial communication port.
8. Selectable NTSC or PAL operation.

1.1 BLOCK DIAGRAM AND OPERATIONAL OVERVIEW

The Z86230 is designed to process XDS data of the television VBI. The device requires both a Composite Video and a horizontal timing signal (HIN/XIN input). Several passive components are required for proper operation. Commands are input to enable the decoder to process and control the V-Chip response to the XDS Content Advisory packet. The Z86230 can also be configured to operate with PAL video signals. In PAL mode, the device decodes information encoded into VBI Line 22. The encoded data must conform to the waveform and command structure defined for NTSC Line 21 operation.

Figure 1 illustrates the Functional Block Diagram of the Z86230.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



1.1.1 Input Signals

The Composite Video input should be a signal which is nominally 1.0 Volt p-p, with sync tips negative and band limited to 600 kHz. The Z86230 operates with an input level variation of ±3 dB.

The HIN/XIN input signal is required to bring the voltage-controlled oscillator (VCO) close to the required operating frequency.

1.1.2 Video Input Signal Processing

The Composite Video input is AC-coupled to the device where the sync tip is internally clamped to a fixed reference voltage.

The Data Slicer extracts a clean CMOS-level data signal by slicing the signal at its midpoint. The slice level is established on an adaptive basis during Line 21.

The Sync Slicer processes the clamped Composite Video signal to extract Composite Sync. This signal is used to lock the internal logic to the incoming video. The slice level is stored on the sync slice capacitor, CSYNC.

The Data Clock Recovery circuit operates in conjunction with the Horizontal (H) Lock circuit. These circuits produce a data clock (DCLK) and, when Line 21 code appears, DCLK phase lock is achieved during the clock run-in burst (used to reclock the sliced data). When phase lock is established, DCLK is maintained until a change in the video signal occurs.

1.1.3 Voltage-Controlled Oscillator (VCO) and One-Shot

All internal timing and synchronizing signals are derived from the on-board 12-MHz VCO. Its output is the DCLK signal used to drive the Horizontal and Vertical counter chains.

The One-Shot circuit produces a horizontal timing signal derived from the incoming video.

The VCO exhibits stable gain characteristics and good power supply rejection.

1.1.4 Timing and Counting Circuits

The DCLK is divided to generate the horizontal timing signals H and 2H.The H signal is further divided in the line counter (LINE CNTR) and field counter (FLD CNTR) to produce the various decodes used to establish vertical lock and to time the control functions required for proper operation.

1.1.5 Command Processor

The Command Processor controls the manipulation of the data for storage. During the recovery time, the command processor, in conjunction with the data recovery circuits, recovers the XDS data.

1.1.6 Decoder Control Circuit

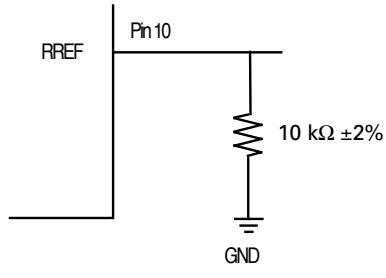
The Decoder Control circuit block is the users communications port. This circuit converts the information from the control port into the internal control signals required to establish the operating mode of the decoder.

The Z86230 responds to its slave address for both the READ and WRITE conditions. If the READ bit is Low (indicating a WRITE sequence), then the Z86230 responds with an Acknowledge. The master should then send an address byte followed by a data byte. If the READ bit is High (indicating a READ sequence), then the Z86230 responds with an Acknowledge followed sequentially by a status byte and a data byte. READ data is only available through indirect addressing. WRITE addressing exhibits both indirect and direct modes. The busy bit in the status byte indicates if the WRITE operation is completed or if READ data is available.

1.1.7 Voltage/Current Reference

The Voltage/Current reference circuit uses an externally connected resistor to establish the reference levels that are used throughout the Z86230. For a minimal investment, the use of an external resistor can also provide improved internal precision.

FIGURE 2. VOLTAGE/CIRCUIT REFERENCE



2. PIN DESCRIPTIONS

There are 2 different packages, 18-pin DIP and 18-pin SOIC, available in the Z86230.

FIGURE 3. 18-PIN DIP AND SOIC DEVICES

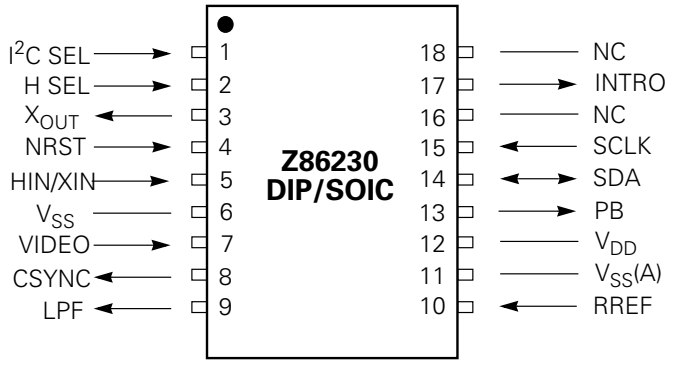


TABLE 1. PIN DESCRIPTIONS

Symbol	Pin #	Function	Direction	Description
I^2C SEL	1	I^2C Address Select	Input	Selects I^2C Address. Low(0) sets the slave address to 28h for WRITE and 29h for READ. HIGH(1) sets the slave address to 2Ah for WRITE and 2Bh for READ.
H SEL	2	HIN/XIN Select	Input	Selects the source of the horizontal frequency signal. Tying pin 2 HIGH(1) selects XIN mode. Tying pin 2 Low(0) selects HIN mode.
X_{OUT}	3	XTAL Output	Output	When operating in XIN mode this pin is the output pin for the XTAL circuit. In HIN mode, the X_{OUT} pin is a no connect (NC).
NRST	4	RESET	Input	Capable of being tied to an $\overline{\text{RESET}}$ signal if a Power-On Reset action is required. $\overline{\text{RESET}}$ must be held Low(0) for at least 100ns; otherwise, the pin must be tied HIGH(1).

TABLE 1. PIN DESCRIPTIONS

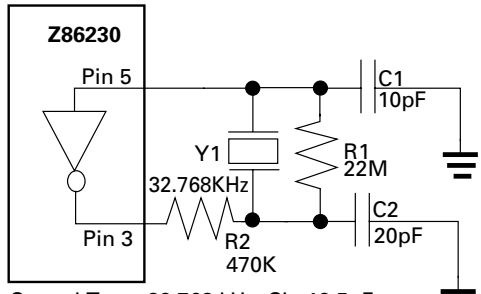
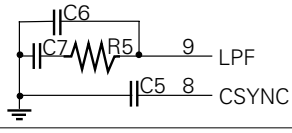
Symbol	Pin #	Function	Direction	Description
HIN/XIN	5	Horizontal In/XTAL In	Input	When XTAL mode is selected, the horizontal frequency signal may be generated on the chip using the external 32.768-kHz crystal circuit, as shown below. This circuit must be connected between pin 5 and 3.  Crystal Type: 32.768 kHz, CL=12.5pF Series Resistance < 35 kOhms (18 kOhms typ) Epson, C-001R 32.768 kHz or Fox, NC26, NC28 or equivalent When HIN mode is selected, a horizontal frequency signal must be supplied to the pin. This signal must be within +3% Fh; however, the frequency signal can exhibit any polarity and duty cycle. Alternatively, an external horizontal frequency signal may be used in XIN mode operation. In this case, the signal must exhibit a frequency of 32.768 KHz.
V_{SS}	6	Power Supply (digital) GND	N/A	This pin is the lowest potential power pin for the digital circuit that is typically tied to system ground.
VIDEO	7	Composite Video	Input	Composite NTSC video input, 1.0V p-p (nom), band limited to 600 kHz. The circuit operates with signal variation between 0.7–1.4V p-p. The polarity is sync tips negative. This signal pin should be AC-coupled through a 0.1 µF capacitor and driven by a source impedance of 470 ohms or less.
CSYNC	8	Composite Sync	Output	Sync slice level. A 0.1 µmF capacitor must be tied between this pin and analog ground V_{SS}(A). This capacitor stores the sync slice level voltage.

TABLE 1. PIN DESCRIPTIONS

Symbol	Pin #	Function	Direction	Description
LPF	9	Loop Filter	Output	Loop Filter. A series RC low-pass filter must be tied between this pin and analog ground V_{SS}(A). There must also be second capacitor from the pin to V_{SS}(A). 
RREF	10	Resistor Reference	Input	Reference setting resistor. This resistor must be 10 kOhms, ±2%.
V_{SS}(A)	11	Power Supply (Anlalog) GND	N/A	This pin is the lowest potential power pin for the analog circuit that is typically tied to system ground.
V_{DD}	12	Power Supply +5V	N/A	The voltage on this pin is nominally 5.0 Volts, and may range between 4.75 to 5.25 Volts with respect to the V_{SS} pins.
PB	13	Program Blocking	Output	This pin is HIGH(1) when the received Content Advisory packet matches the viewers selection as entered into the Content Advisory Rating Select registers.
SDA	14	Serial Data	In/Output	This pin is the bidirectional data line for sending and receiving serial data.
SCLK	15	Serial Clock	Input	This pin acts as an input pin for the serial clock signal from the I^2C master. The clock rate is expected to be within I^2C limits.
NC	16	No Connect	N/A	No Connect
INTRO	17	Interrupt Output	Output	This pin provides an interrupt signal to the master control device in accordance with the settings in the Interrupt Mask Register.
NC	18	No Connect	N/A	No Connect

3. Z86230 FEATURE SET

The primary features of the Z86230 are briefly described below. More complete descriptions can be found in later sections of this document.

3.1 VBI DATA PROCESSING

The Z86230 extracts the XDS data in Line 21 of the incoming video. Processing includes:

1. Extracting XDS data from the input video.
2. Outputting the V-Chip Program Blocking signal (PB).
3. Outputting the XDS data through the serial port (raw or filtered).
4. Selecting the XDS filter parameters from a list of preprogrammed values.
5. Selecting either NTSC or PAL operation.

3.2 SERIAL COMMUNICATIONS INTERFACE

Communications and control of the Z86230 is possible through the I^2C serial control interface, composed of:

1. A 2-wire I^2C interface.
2. Two available slave addresses.

TABLE 2. Z86230 SERIAL CONTROL SIGNALS

Signal	I^2C SEL	SCLK	SDA
Pin #	1	15	14
I/O	I	I	I/O
1^{st} I^2C Address (28h(W)/29h(R))	0	CLK	Data
2^{nd} I^2C Address(2Ah(W)/2Bh(R))	1	CLK	Data

3.3 SETUP AND OPERATIONAL CONTROL

The Z86230 is fully programmable through its flexible I^2C serial communication port. The following tables provide a *partial list* of User-Programmable Features and Default Conditions upon RESET.

TABLE 3. USER PROGRAMMABLE FEATURES

Feature	Parameters	RESET Condition
Video Standard	NTSC/PAL	NTSC
VCO Lock	Video/External HIN	Video
H Lock	Video/External HIN	Video
XDS Data Output	Raw/Filtered	OFF
Contents Advisory Rating Select	ON/OFF	OFF
Program Blocking	ON/OFF	ON
Blocking *No Rating* Programs	ON/OFF	OFF
Program Unblock Hold Off	Up to 254 Vertical Frames	0

4. SERIAL COMMUNICATIONS INTERFACE

Commands and data are sent to and from the Z86230 through its I²C serial communications interface. This port is the path for setting the configuration and operational modes of the device. The interface is also used as the port for outputting the recovered XDS data.

4.1 I²C BUS OPERATION

The Z86230 supports a bidirectional 2-wire bus and data transmission protocol. The bus is controlled by the master device, which generates the serial clock (SCLK), controls the bus access, and generates the START and STOP conditions. The serial data (SDA) pin is the bidirectional data line. The Z86230 is a slave device with two possible slave addresses. When the I²C SEL pin is Low, the slave address is 28h for WRITE and 29h for READ. When the I²C SEL pin is High, the slave address is 2Ah for WRITE and 2Bh for READ.

The Z86230 can receive or transmit data under control of the master device. Communication is initiated when the master device sends the START condition followed by the Z86230 Slave Address READ byte or Slave Address WRITE byte. The Z86230 responds with an Acknowledge.

The I²C RD/$\overline{WR}$ bit is the Least Significant Bit (LSB) of the I²C addresses listed below in Table 4.

TABLE 4. Z86230 I²C SLAVE ADDRESSES

	READ	WRITE
1st I²C Address	29h	28h
2nd I²C Address	2Bh	2Ah

NOTE: Low(0) on pin 1 selects the 1st I²C Address; HIGH(1) on pin 1 selects the 2nd I²C Address.

4.1.1 The I²C Bus Protocol

The Bus Protocol requires that:

1. Data transfer can only be started when the bus is not busy.
2. During data transfer, data transitions must not occur while the clock is High.

4.1.2 Bus Conditions

Bus Conditions are defined as:

Not Busy. Data and Clock lines are both High.

START. A High-to-Low transition of the SDA line while the SCLK line is High.

STOP. A Low-to-High transition of the SDA line while the SCLK line is High.

Acknowledge. When addressed, the receiving device must output an Acknowledge after the reception of each byte. The master device must generate the clock for the Acknowledge bit. Acknowledge is SDA = Low. Not Acknowledge (NACK) is SDA = High.

Data. The data (SDA) is output by the transmitting device on the falling edge of SCLK, MSB first. The receiving device interprets the data, MSB first, on the rising edge of SCLK.

Communication with the Z86230 is initiated when the master device sends the Z86230 slave address following a START condition. The Z86230 has a preset, single, seven-bit slave address. The Z86230 responds with an Acknowledge. The eighth bit of the slave address is driven High for READ operations and Low for WRITE operations.

4.1.3 Writing to the I2C Bus

Commands and data are written to the Z86230 using the I^2C bus interface. The device is enabled when an I^2C START condition, followed by its Slave Address WRITE byte, is received. A WRITE operation is ended and the bus is disabled upon the receipt of an I^2C STOP condition. Any number of command bytes, up to 32, may be sent after the device is WRITE-enabled. Each of these commands is either 1 or 2 bytes in length. The device executes the commands in order of receipt.

Overflowing the 32 byte buffer causes improper operation. The RDY bit of the Serial Status Register (SSR) may be read to determine if there is room in the command buffer for at least 2 bytes of command data. The Status register data is output immediately following the receipt of the Slave Address READ.

The first byte of a 2-byte command is always written first. The master's sequence for writing a 2-byte command, followed by a 1-byte command is displayed in the following example:

Start

Slave_Address_Write/Slave ACK

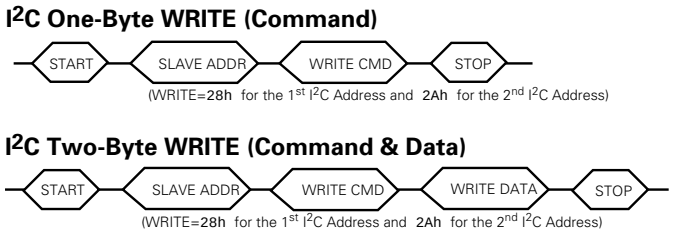
CMD1_Write/Slave ACK

DATA1_Write/Slave ACK

CMD2_Write/Slave ACK

Stop

FIGURE 4. I2C BUS WRITE (COMMAND)



NOTE: The Status Register RDY bit must be read and checked prior to the START condition of either WRITE sequence above. Refer to the One Byte READ (Status Only) in Figure 5 for more information on reading the Status Register.

4.1.4 Reading Data Using the I2C Bus

The Z86230 I2C bus supports READ sequences up to 34 bytes in length. All READ sequences output the Serial Status Register (SSR) as the first output byte. The data to be read is selected by sending the READ BANK SELECT (RBS) command. Four READ bank modes are available in the Z86230:

TABLE 5. Z86230 I2C READ BANK SELECT (RBS) COMMAND

RBS Command	Descriptions
Bank 0	A general-purpose bank used to read the Z86230-defined internal registers. The register to be read from Bank 0 is set up manually using the READ SELECT commands, RDS1 and RDS2. These commands load the selected data byte (or pair of bytes) into the first location(s) of Bank 0, and set the DAV bit to indicate the availability of data.
Bank 1	A special purpose bank provided to facilitate the reading of commonly accessed data. This bank contains the Program Blocking registers and permits direct, multibyte reading of internal registers 08h through 11h. These registers are described in the internal register section. When it is selected, the sequence of bytes read is SSR, followed by internal registers 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h, and 11h.
Bank 2	A special purpose bank provided to facilitate the reading of commonly accessed data. This bank contains the XDS Program Name data from the most recently received current class type 3 packet.
Bank 3	A special purpose bank provided to facilitate the reading of commonly accessed data. This bank contains the XDS Network Name and Call Letter data. The first 26 bytes has the XDS Network Name from the most recently received XDS channel class type 1 packet. Bytes 26 through 31 has the XDS Call Letters data from the most recently received XDS channel class type 2 packet

NOTE: Banks 2 and 3 are 33 bytes in length. Byte 32 of these banks contains an 8 bit checksum. The checksum is calculated such that the addition of the 32 data bytes and the checksum modulo 256 equals zero. The checksum should always be evaluated after reading this data to ensure that the XDS data is not being updated during the READ operation. The result is a meaningless combination of two unrelated XDS data packets. If a bad checksum is encountered, the READ operation should be repeated.

All READ sequences output the SSR first. If the Serial Status register DAV bit is set, a 2- or multiple-byte READ sequence can be initiated, beginning with a START condition. If the DAV bit is not set, the I²C master device should not attempt to read any data bytes or the required data can be lost from the Z86230 output registers. The I²C master device should end the READ sequence by failing to acknowledge the received byte. This sequence is repeated until the DAV bit becomes true.

NOTE: In all I²C READ operations (1-, 2- and 3-byte reads are illustrated in Figure 5), the most recent byte read from the Z86230 should be acknowledged by the master with a Not Acknowledge (NACK). The DAV bit of the Serial Status Register (SSR) is cleared by the master clocking out the eighth bit of the first data byte read. The DAV bit is never cleared by just reading the SSR (One Byte READ) alone. All data is output MSB first.

The master's sequence for reading two *data bytes* (total of 3 bytes including SSB) from the Z86230 is:

Start

Slave_Address_Read/Slave_ACK

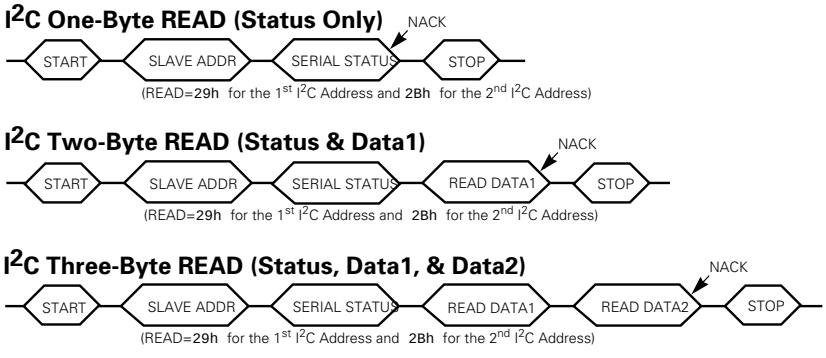
SS_Byte/Master ACK

First_Byte/Master ACK

Second_Byte/Master_NACK

Stop

FIGURE 5. I²C BUS READ (COMMAND)



NOTE: In all I²C READ operations, the most recent byte read from the Z86230 must be acknowledged by the master with a NACK (Not ACKnowledge).

4.1.5 Clock and Data Transitions

The SCLK and SDA bus lines are normally pulled High with a resistor. Data on the SDA bus may only change during SCLK Low time periods. Data changes during SCLK High periods indicate a START or STOP condition as defined in Table 6.

4.1.6 START Condition

A High-to-Low transition of SDA with SCLK High is a START condition which must precede any other command.

4.1.7 STOP Condition

A Low-to-High transition of SDA with SCLK High is a STOP condition which terminates all communications.

4.1.8 Acknowledge

All address and data words are serially transmitted to and from the Z86230 in eight bit words. A ninth bit time is used for the Acknowledge. The acknowledging device pulls the SDA bus Low during the ninth bit. A Not Acknowledge (NACK) is returned by SDA = High during the ninth clock time.

FIGURE 6. I²C SERIAL TIMING

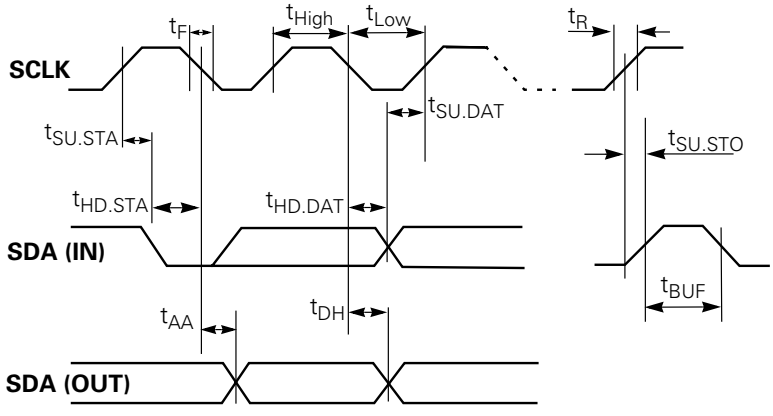


TABLE 6. I²C SERIAL TIMING MIN/MAX

Symbol	Parameter	Min	Max	Units
f_{SCLK}	Clock Frequency		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7	–	ms
t_{High}	Clock Pulse Width High	4.0	–	ms
t_R	SDA and SCL Rise Time	–	1.0	ms
t_F	SDA and SCL Fall Time	–	300	ns
t_{AA}	Clock Low to Data Out Valid	0.1	3.5	ms
t_{BUF}	Bus Free Time	4.7	–	ms
$t_{HD.STA}$	Start Hold Time	4.0	–	ms
$t_{SU.STA}$	Start Set-up Time	4.7	–	ms
$t_{HD.DAT}$	Data In Hold Time	0	–	ms
$t_{SU.DAT}$	Data In Set-up Time	250	–	ns
$t_{SU.STO}$	Stop Set-up Time	4.7	–	ms
t_{DH}	Data Out Hold Time	100	–	ns
t_I	Input Filter Time Constant		100	ns

5. COMMANDS

5.1 SERIAL PORT COMMANDS

The commands must be contained within the Start–Slave Address–etc. sequence.

NOTE: In the following Command descriptions, the letter h following a command code designates hexadecimal notation.

5.1.1 RESET = FBh

RESET is a 1-byte command. The RESET command establishes all of the specified default settings in the device, but it does not reset the serial port itself. The RESET command must be followed by a no operation (NOP) command, because RESET stays active until deactivated by the NOP. This sequence can be entered without the RDY bit being set.

5.1.2 NOP = 00h

NOP is a 1-byte command. The NOP command does not affect the status of the RDY bit in the Serial Status Register (SSR) and can be executed independent of the RDY status.

TABLE 7. BASIC SERIAL COMMANDS

Serial Command	Command Code
RESET	FBh
NOP	00h

5.2 READ AND WRITE COMMANDS

All register diagrams indicated in this section incorporate the following conventions, unless otherwise noted:

- R = Read, W = Write, X = Indeterminate, and *res* = Reserved
- All register bits marked as *res* must be set to Low(0)

5.2.1 READ Bank Select (RBS = FDh)

RDS1 is a 2-byte command to select the read data bank. The lower 2 bits of the second data byte select one of four banks of up to 33 bytes. A subsequent I^2C READ deciphers data from the specified bank.

5.2.2 READ SELECTs (RDS1 = 40h–51H)

RDS1 is a 1-byte command used to initiate a 1-byte READ sequence. This activity is performed by moving the contents of the register identified by the address field (AD00:04) of the command to the first location of READ bank 0. Addresses 00h–11h are valid in the RDS1 command field AD00:04.

TABLE 8. RDS1–READ ONE BYTE (RDS1 = 40h–51h)

Bit	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	0	1	0	AD04	AD03	AD02	AD01	AD00
R/W	W	W	W	W	W	W	W	W

5.2.3 RDS2 = 60h–70h

RDS2 is a 1-byte command which is used to initiate a 2-byte READ sequence by moving the contents of the two consecutive registers, starting with the one identified by the address portion of the command (AD00:AD04), to the first 2 locations of read bank 0. Only Addresses 00h–10h are valid in the RDS2 command field AD00:04.

NOTE: For XDS data recovery, when the XDS Filter Register (see Control Registers) is enabled for the required packets, the Z86230 automatically establishes the 2-byte recovery mode and moves the recovered data bytes to the first 2 locations of bank 0.

TABLE 9. RSD2–READ TWO BYTES (RDS2 = 60h–70h)

Bit	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	0	1	1	AD04	AD03	AD02	AD01	AD00
R/W	W	W	W	W	W	W	W	W

5.3 WRITING TO THE Z86230

5.3.1 WRxx = C0h–D1h

TABLE 10. WRXX–WRITE REGISTER XX (WRX = C0h–D1h)

Bit	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
	1	1	0	AD04	AD3	AD2	AD1	AD0
R/W	W	W	W	W	W	W	W	W

The WRITE commands require 2 bytes to execute. The first byte is the write command and includes the Z86230 register address (AD00:04) being written. The second byte is the data to be written.

6. CONTROL REGISTERS

Information controlling the setup and operation of the Z86230 are maintained in several registers. The user may read or alter the contents of these registers as required.

All register diagrams indicated in this section incorporate the following conventions, unless otherwise noted:

- R = Read, W = Write, X = Indeterminate, and *res* = Reserved
- All register bits marked as *res* must be set to Low(0)

6.1 REGISTERS SUMMARY

6.1.1 Serial Status Register

TABLE 11. SERIAL STATUS REGISTER (ADDRESS NOT REQUIRED)

Bit	7	6	5	4	3	2	1	0
	RDY	DAV	res	WOVR	INTR	ROVR	FLD	LOCK
R/W	R	R	R	R	R	R	R	R

D_0–LOCK. Active High, indicating that the internal sync circuits are locked. May be used as an indication of the presence of a video signal.

D_1–FLD. Signals the current video field. Low = Field 2, High = Field 1.

D_2–ROVR. Active High, indicating that the data available in the output buffer is not read out and new data is written over it.

D_3–INTR. Active High, indicating that an interrupt other than DAV is pending. Reserved.

D_4–WOVR. Active High, indicating a serial input data overrun.

D_5-Res. Reserved.

D_6-DAV. Active High, indicating that data is available to be read out.

D_7–RDY. Active High, indicating that the port input buffer is empty. Only the NOP, RESET and READ instructions may be sent if RDY is Low.

6.1.2 Configuration Register

TABLE 12. CONFIGURATION REGISTER (ADDRESS = 00h)

Bit	7	6	5	4	3	2	1	0
	res	res	res	res	res	res	res	TVS
R/W	R	R	R	R	R	R/W	R	R/W

D_0–TVS. Selects the television standard. High selects PAL and Low selects NTSC. The default is NTSC. When PAL is selected, the display defaults to 15 TV scan lines per display row.

D_1-Res. Reserved

D_2-D_7-Res. Reserved.

6.1.3 XDS Data Activity Register

TABLE 13. XDS DATA ACTIVITY REGISTER (ADDRESS = 04h)

Bit	7	6	5	4	3	2	1	0
	res	res	res	res	res	res	XDS	res
R/W	R	R	R	R	R	R	R	R

D_0-Res. Reserved.

D_1–XDS. Indicates XDS data is being processed. This bit becomes inactive if no XDS data is received within the previous 16 seconds: High = Active, Low = Inactive. The RESET state is Low.

D_2-D_7-Res. Reserved.

6.1.4 XDS Filter Register

TABLE 14. XDS FILTER REGISTER (ADDRESS = 05h)

Bit	7	6	5	4	3	2	1	0
	s_2	s_1	s_0	PUBL	MISC	CHAN	FUTR	CURR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D_0–CURR. Selects Current Class packets for output through the Serial Control port when XDS recovery is enabled.

D_1–FUTR. Selects Future Class packets for output through the Serial Control port when XDS recovery is enabled.

D_2–CHAN. Selects Channel Information Class packets for output through the Serial Control port when XDS recovery is enabled.

D_3–MISC. Selects Miscellaneous Class packets for output through the Serial Control port when XDS recovery is enabled.

D_4–PUBL. Selects Public Service Class packets for output through the Serial Control port when XDS recovery is enabled.

D_5-D_7–s_0–s_2. Selects a set of secondary parameters, tabulated below, to be used in filtering the XDS data when XDS recovery is enabled.

TABLE 15. XDS SECONDARY FILTER SETTINGS

Secondary Filter	Filter Value (s0:s2)
All	0h
Time Information	1h
In Band Only	2h
Content Advisory	3h
VCR Information	4h
Reserved	5h
Reserved	6h
Reserved	7h

Notes:
1. Setting this register to 00h turns XDS data recovery off. Setting bits D_0 through D_4 enables XDS data recovery for the Classes selected as qualified by the Secondary Filter (bits D_5–D_7). If Bits D_0–D_4 are all set to 1, all Classes of XDS data are output (even Reserved and Undefined).
2. The Time Information Only selection includes the Time of Day (TOD) and Local Time Zone (LTZ) packets.
3. VCR Information selects TOD, LTZ, Net ID, Local Call Letters, Impulse Capture, Tape Delay, Composite 2, and Out-of-Band Channel Number packets for recovery.

6.1.5 Interrupt Request Register

TABLE 16. INTERRUPT REQUEST REGISTER (ADDRESS = 06h)

Bit	7	6	5	4	3	2	1	0
	res	res	dXDS	res	dLOK	EOF	DLE	res
R/W	R/W	R/W	R/W	R/W	R/W	R	R	—

D_0-Res. Reserved.

D_1-DLE. Active High, indicating that the data line has ended. This bit sets two lines after the data line, and clears about 20 lines before the end of the field.

D_2–EOF. Active High, indicating that the video signal is currently at the end of a field. This bit sets during line 262 in Field 1 and line 524 in Field 2. This bit clears about 2 lines before the end of the field.

D_3–dLOK. Active High, indicating that the state of the LOCK signal has changed. The SSR must be read to determine the current state.

D_4-Res. Reserved.

D_5–dXDS. Active High, indicating that a change in XDS activity has occurred. The Line 21 Activity Register must be read to determine if XDS data is active.

D_6-D_7-Res. Reserved.

NOTE: Except as noted for the case of D1 and D2 above, the master device must write a 1 to the appropriate bit in the Interrupt Request Register to clear the Interrupt. Writing a 1 to

any valid bit position the Interrupt Request Register is equivalent to CLEARing an interrupt request on that bit.

6.1.6 Interrupt Mask Register

TABLE 17. INTERRUPT MASK REGISTER (ADDRESS = 07h)

Bit	7	6	5	4	3	2	1	0
	res	res	dXDS	res	dLOK	EOF	DLE	DAV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register identifies which activities in the Interrupt Request Register is used to cause an interrupt. Setting the bit to 1 enables the interrupt when the corresponding event becomes active. Setting all bits of this register to zero disables interrupts.

6.1.7 Content Advisory Ratings Select Register 1

This register holds the MPAA Content Advisory selections made by the viewer.

TABLE 18. CONTENT ADVISORY RATINGS SELECT REGISTER 1 (ADDRESS = 08h)

Bit	7	6	5	4	3	2	1	0
	res	Not Rated	X	NC-17	R	PG-13	PG	G
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D_0–G. The Z86230 outputs High on pin 13 when the incoming video program is *G-rated* according to the MPAA Ratings standards, and this bit is set to High.

D_1–PG. The Z86230 outputs High on pin 13 when the incoming video program is *PG-rated* according to the MPAA Ratings standards, and this bit is set to High.

D_2-PG-13. The Z86230 outputs High on pin 13 when the incoming video program is *PG-13-rated* in MPAA Ratings standards, and this bit is set to High.

D_3-R. The Z86230 outputs High on pin 13 when the incoming video program is *R-rated* according to the MPAA Ratings standards, and this bit is set to High.

D_4-NC-17. The Z86230 outputs High on pin 13 when the incoming video program is *NC-17-rated* according to the MPAA Ratings standards, and this bit is set to High.

D_5-X. The Z86230 outputs High on pin 13 when the incoming video program is *X-rated* according to EIA-744A and EIA-608A specifications. MPAA no longer recognizes the X rating.

D_6-Not Rated. The Z86230 outputs High on pin 13 when the incoming video program is *Not Rated* according to the MPAA Ratings standards, and this bit is set to High.

D_7-Res. Reserved. This bit must be kept Low(0).

NOTE: The Z86230 outputs Low when a bit in this register is set to Low, and the incoming video program possesses the corresponding MPAA Rating. The device outputs High onto pin 13 only when a bit is set to High; it recovers the corresponding MPAA Rating in the incoming video program.

6.1.8 Content Advisory Ratings Select Register 2

This register holds the TV Parental Guidelines (Base Content) Content Advisory selections made by the viewer.

TABLE 19. CONTENT ADVISORY RATINGS SELECT REGISTER 2 (ADDRESS = 09h)

Bit	7	6	5	4	3	2	1	0
	res	NONE	TV-MA	TV-14	TV-PG	TV-G	TV-Y7	TV-Y
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

D_0-TV-Y. The Z86230 outputs High on pin 13 when the incoming video program is *TV-Y-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_1-TV-Y7. The Z86230 outputs High on pin 13 when the incoming video program is *TV-Y7-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_2-TV-G. The Z86230 outputs High on pin 13 when the incoming video program is *TV-G-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_3-TV-PG. The Z86230 outputs High on pin 13 when the incoming video program is *TV-PG-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_4-TV-14. The Z86230 outputs High on pin 13 when the incoming video program is *TV-14-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_5-TV-MA. The Z86230 outputs High on pin 13 when the incoming video program is *TV-MA-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_6-TV-MA. The Z86230 outputs High on pin 13 when the incoming video program is *TV-NONE-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_7-Res. Reserved. This bit must be kept Low(0).

NOTE: The Z86230 outputs Low when a bit in this register is set to Low, and the incoming video program possesses the corresponding TV Parental Guidelines Rating. The device outputs High onto pin 13 only when a bit is set to High; it recovers the corresponding TV

Parental Guidelines Ratings in the incoming video program. This control register is for the base rating of TV Parental Guidelines.

6.1.9 Content Advisory Ratings Select Register 3

This register holds the TV Parental Guidelines (V and S Contents) Content Advisory selections made by the viewer.

TABLE 20. CONTENT ADVISORY RATINGS SELECT REGISTER 3 (ADDRESS = 0Ah)

Bit	7	6	5	4	3	2	1	0
	TV-MA-V	TV-14-V	TV-PG-V	TV-Y7-FV	res	TV-MA-S	TV-14-S	TV-PG-S
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D_0-TV-PG-S. The Z86230 outputs High on pin 13 when the incoming video program is *TV-PG-S-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_1-TV-14-S. The Z86230 outputs High on pin 13 when the incoming video program is *TV-14-S-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_2-TV-MA-S. The Z86230 outputs High on pin 13 when the incoming video program is *TV-MA-S-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_3-Res. Reserved. This bit must be kept Low(0).

D_4-TV-Y7-FV. The Z86230 outputs High on pin 13 when incoming video program is *TV-Y7-FV-rated* in TV Parental Guidelines Ratings standards, and this bit is set to High.

D_5-TV-PG-V. The Z86230 outputs High on pin 13 when the incoming video program is *TV-PG-V-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_6-TV-14-V. The Z86230 outputs High on pin 13 when the incoming video program is *TV-14-V-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_7-TV-MA-V. The Z86230 outputs High on pin 13 when the incoming video program is *TV-MA-V-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

NOTE: The Z86230 outputs Low when a bit in this register is set to Low and the incoming video program possesses the corresponding TV Parental Guidelines Rating. The device outputs High onto pin 13 only when a bit is set to High; it recovers the corresponding TV Parental Guidelines Rating in the incoming video program. This control register is for the S- and V-rated programs in TV Parental Guidelines Rating.

6.1.10 Content Advisory Ratings Select Register 4

This register holds the TV Parental Guidelines (L and D Content) Content Advisory selections made by the viewer.

TABLE 21. CONTENT ADVISORY RATINGS SELECT REGISTER 4 (ADDRESS = 0Bh)

Bit	7	6	5	4	3	2	1	0
	res	TV-MA-L	TV-14-L	TV-PG-L	res	res	TV-14-D	TV-PG-D
R/W	R	R/W	R/W	R/W	R	R	R/W	R/W

D_0-TV-PG-D. The Z86230 outputs High on pin 13 when the incoming video program is *TV-PG-D-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_1-TV-14-D. The Z86230 outputs High on pin 13 when the incoming video program is *TV-14-D-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_2-D_3. Reserved. These bits must kept Low(0).

D_4-TV-PG-L. The Z86230 outputs High on pin 13 when the incoming video program is *TV-PG-L-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_5-TV-14-L. The Z86230 outputs High on pin 13 when the incoming video program is *TV-14-L-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_6-TV-MA-L. The Z86230 outputs High on pin 13 when the incoming video program is *TV-MA-L-rated* according to the TV Parental Guidelines Ratings standards, and this bit is set to High.

D_7-Res. Reserved. This bit must be kept Low(0).

NOTE: The Z86230 outputs Low when a bit in this register is set to Low and the incoming video program possesses the corresponding TV Parental Guidelines Rating. The device outputs High onto pin 13 only when a bit is set to High and it recovers the corresponding TV Parental Guidelines Rating in the incoming video program. This control register is for the D- and L-rated programs in TV Parental Guidelines Rating.

6.1.11 Content Advisory Register 1

TABLE 22. CONTENT ADVISORY REGISTER 1 (ADDRESS = 0Ch)

Bit	7	6	5	4	3	2	1	0
	B	1	D	a1	a0	r2	r1	r0
R/W	R	R	R	R	R	R	R	R

D_0-D_6. These bits hold the corresponding information recovered from the first byte of the received Content Advisory Ratings packet.

D_7-B. This bit indicates the blocking status. When this bit is High, it indicates that the data from the received Content Advisory packet matches the user selection contained in one of the Content Advisory Ratings registers, and the PB pin is in the blocking status.

6.1.12 Content Advisory Register 2

TABLE 23. CONTENT ADVISORY REGISTER 2 (ADDRESS = 0Dh)

Bit	7	6	5	4	3	2	1	0
	P	1	(F)V	S	L	g2	g1	g0
R/W	R	R	R	R	R	R	R	R

D_0-D_6. These bits hold the corresponding information recovered from the second byte of the received Content Advisory Ratings packet.

D_7-P. This bit indicates the validity of the data in the recovered Content Advisory packet. When this bit is High, it indicates that the data from the received Content Advisory packet is valid. This bit clears if no Content Advisory packet is received after 5 seconds.

6.1.13 Blocking Control Register 1

TABLE 24. BLOCKING CONTROL REGISTER 1 (ADDRESS = 0Eh)

Bit	7	6	5	4	3	2	1	0
	BLEN	BTE						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D_0-D_6-BTE. These bits set the Block Timer which controls the duration of the hold of the blocking signal on a change of channel. The default value of 0 has a hold time of 2 seconds. The time is extended in 2 frames with each binary step.

D_7-BLEN. These bits enable the blocking capability. BLEN=0 enables blocking; BLEN=1 disables blocking.

6.1.14 Content Advisory Ratings Select 5

This register holds the Canadian English Language Content Advisory selections made by the viewer.

TABLE 25. CONTENT ADVISORY RATINGS SELECT REGISTER 5 (ADDRESS = 0Fh)

Bit	7	6	5	4	3	2	1	0
	res	18+	14+	PG	G	C8+	C	E
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D_0-E. The Z86230 outputs High on pin 13 when the incoming video program is *E-rated* according to the Canadian English Language Ratings standards, and this bit is set to High.

D_1-C. The Z86230 outputs High on pin 13 when the incoming video program is *C-rated* according to the Canadian English Language Ratings standards, and this bit is set to High.

D_2-C8+. The Z86230 outputs High on pin 13 when the incoming video program is *C8+-rated* according to the Canadian English Language Ratings standards, and this bit is set to High.

D_3-G. The Z86230 outputs High on pin 13 when the incoming video program is *G-rated* according to the Canadian English Language Ratings standards, and this bit is set to High.

D_4-PG. The Z86230 outputs High on pin 13 when the incoming video program is *PG-rated* according to the Canadian English Language Ratings standards, and this bit is set to High.

D_5-14+. The Z86230 outputs High on pin 13 when the incoming video program is *14+-rated* according to the Canadian English Language Ratings standards, and this bit is set to High.

D_6-18+. The Z86230 outputs High on pin 13 when the incoming video program is *18+-rated* according to the Canadian English Language Ratings standards, and this bit is set to High.

D_7-Res. Reserved. This bit must be kept Low(0).

NOTE: The Z86230 outputs Low when a bit in this register is set to Low and the incoming video program possesses the corresponding Canadian French Language Rating. The device outputs High onto pin 13 only when a bit is set to High and it recovers the corresponding Canadian English Language Rating in the incoming video program.

6.1.15 Content Advisory Ratings Select Register 6

This register holds the Canadian French Language Content Advisory selections made by the viewer.

TABLE 26. CONTENT ADVISORY RATINGS SELECT REGISTER 6 (ADDRESS = 10h)

Bit	7	6	5	4	3	2	1	0
	res	res	18ans+	16ans+	13ans+	8ans+	G	E
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

D_0-E. The Z86230 outputs High on pin 13 when the incoming video program is *E-rated* according to the Canadian French Language Ratings standards, and this bit is set to High.

D_1-G. The Z86230 outputs High on pin 13 when the incoming video program is *G-rated* according to the Canadian French Language Ratings standards, and this bit is set to High.

D_2-8ans+. The Z86230 outputs High on pin 13 when incoming video program is *8ans+-rated* in Canadian French Language Ratings standards, and this bit is set to High.

D_3-13ans+. The Z86230 outputs High on pin 13 when incoming video program is *13ans+-rated* in Canadian French Language Ratings standards, and this bit is set to High.

D_4-16ans+. The Z86230 outputs High on pin 13 when incoming video program is *16ans+-rated* in Canadian French Language Ratings standards, and this bit is set to High.

D_5-18ans+. The Z86230 outputs High on pin 13 when the incoming video program is *18ans+-rated* according to the Canadian French Language Ratings and this bit is set to High.

D_6-D_7-Res. Reserved. These bits must be kept Low(0).

NOTE: The Z86230 outputs Low when a bit in this register is set to Low and the incoming video program possesses the corresponding Canadian French Language Rating. The device outputs High onto pin 13 only when a bit is set to High and it recovers the corresponding Canadian French Language Rating in the incoming video program.

6.1.16 Blocking Control Register 2

TABLE 27. BLOCKING CONTROL REGISTER 2 (ADDRESS = 11AH)

Bit	7	6	5	4	3	2	1	0
	res	res	res	res	res	res	res	BNR
R/W	R	R	R	R	R	R	R	R/W

D_0-BNR. The Z86230 outputs High on pin 13 when the incoming video program has *No Rating* and this bit is set to Low. Setting this bit to High disables blocking on *No Rating*.

D_1-D_7-Res. Reserved. These bits must be kept Low(0).

6.2 XDS DATA RECOVERY

The Z86230 is able to recover Extended Data Services (XDS) information from the input video signal. This data, formatted according to EIA-608A, can contain a wide variety of information about current and future programs, the channel currently tuned, other channels, and miscellaneous data, including time of day.

XDS data packets are tagged according to a Class/Type system defined by EIA-608A. The Z86230 can be programmed to filter the XDS data stream to extract only the classes of interest to the application. An additional level of filtering is provided that permits selection of certain groups of packets that are of use in specific applications. XDS filtering reduces the traffic on the serial bus, reduces the load of the TV/VCR control processor, and simplifies external XDS decoding.

XDS data recovery is enabled by selecting one or more classes in the XDS Filter Register. Optionally, a secondary filter code can be specified which further limits the packets to be recovered. When XDS recovery is enabled, filtered data pairs are loaded into the first two data locations of Bank 0 immediately upon receipt. The DAV bit of the Serial Status Register (SSR) then goes High, indicating the availability of two output bytes.

When the XDS Filter Register is set to `00h` (the default state), XDS recovery is disabled.

CAUTION: When XDS data recovery is enabled, the external controller should never perform any other read operation, except SSR reads, in the beginning of Field 2. Commands other than READ SELECTs do not interfere with XDS data recovery regardless of their position in the video frame.

Some examples of Z86230 WRITE commands that could be used to set the XDS Filter Register are indicated in Table 28. The XDS Filter Register bit assignments are defined in Table 30.

TABLE 28. XDS DATA EXTRACTION EXAMPLE FILTER SETTINGS

{WRITE Command, Filter Code}	XDS Filter Output
{C5,41}	All In Band; Current Class packets recovered.
{C5,61}	Program Rating; Current Class packets recovered. This filter may be used for Program Blocking Data Packet Recovery.
{C5,1F}	All XDS packets recovered.
{C5,01}	All Current Class packets recovered.
{C5,28}	Time information recovered. This filter extracts the Time of Day (TOD) and Local Time Zone (LTZ) packets from the Miscellaneous Class data. This filter may be used to implement Auto Clock-Setting in TVs, and VCRs.
{C5,9F}	VCR Information recovered. This filter selects TOD, LTZ, Net ID, Local Call Letters, Impulse Capture, Tape Delay, Composite 2, and Out-of-Band Channel Number packets for recovery.

6.2.1 Filtered XDS Data Format

Filtered XDS data is output from the Z86230 in the order it is received on Line 21. In other words, think of the Z86230 XDS filter function as creating a new, smaller stream of XDS data packets. This new data stream looks exactly as though the Class and Type specified in the XDS Filter Register (05h) are *the only data* encoded on Line 21 of Field 2. The filtered data output from the Z86230 is in full compliance with EIA-608 specifications for XDS data streams (headers and control codes intact). Refer to the **NOTE** paragraph on the next page for a special exception to this rule.

XDS data and header information (including START, CONTINUE, and END commands) are passed through the filter for the XDS Class and Type specified in the XDS Filter Register. All other Line 21 data is filtered out. This data does not output or generate a data available flag (DAV) in the Serial Status Register (SSR).

To properly read filtered XDS data from the Z86230, the master device must first write the XDS Filter Register (05h) with its required XDS Class and Type information. For example, in the Z86230, in order to extract ONLY the Line 21 Program Rating information, the master must write the value 61h to the XDS Filter Register. The master should then poll the state of the DAV bit in the SSR until DAV = 1.

As soon as DAV = 1, the master may initiate a 3-byte READ in RBS Read Bank 0 mode (XDS data bytes always arrive in pairs, so it is safe to read the first 2 bytes of read bank 0 when DAV = 1 in the SSB). A 3-byte READ always yields two data bytes, which in this case are the first 2 bytes of the Current Class, Program Rating Type XDS data stream encountered on Line21, Field 2. The master device must then interpret those 2 bytes according to EIA-608 specifications for Current Class, Program Rating Type data. Refer to EIA-608 for the appropriate data formats.

The XDS filters on the Z86230 greatly reduce the amount of Field 2 data passed on to the master device for further processing and interpretation; however, the master device must still interpret the filtered data stream in accordance with EIA-608A. In other words, only the selected XDS data Class and Type packets are chosen. The filtered data stream contains all of the XDS command and data packets. Though the Z86230 filtered data stream is in full compliance with the EIA-608 specification, the master device must still interpret the necessary packets to ensure full compliance with EIA-608A.

NOTE: The Z86230 XDS filter for Program Rating information functions differently than all other Z86230 predefined XDS filters. This change has been made to minimize the amount of data passed through the Program Rating XDS filter, thereby minimizing the interpretation and communications load on the master device. When the XDS Filter Register is set to 61h (Class=01h (Current), Type=05h (Program Rating) the only data from Line 21 Field 2 that passes through the filter is:

1. Program Rating Packet: [xxh,xxh]. The Current Class Program Rating data byte pair as defined in EIA-608. The program's rating is encoded per EIA-608 in the xxh byte pair.
2. The END Packet [0Fh,CHKSUM]. A 2-byte packet that includes a CHKSUM computed per EIA-608A. The checksum calculation includes the START packet [01h,05h] even though this value was not passed through the filter.

6.3 Z86230 COMMANDS AND REGISTERS SUMMARY

TABLE 29. Z86230 SUMMARY OF CONTROL COMMANDS

Name	Code	Function
RESET	FBh	RESET is 1-byte command sequence serial communication. The RESET command establishes all of the specified default settings in the device; however, it does not reset the serial port itself. This sequence can be entered without RDY being set.
NOP	00h	NOP is a 1-byte command for use in serial communication. The NOP command does not affect the status of the RDY bit in the Serial Status Register (SSR) and can be executed independent of the RDY status.
RDS1	40h–51h	RDS1 is a 1-byte command used to initiate a 1-byte READ sequence by moving the contents of the register identified by the address field (AD00:04) of the command to the output register. Addresses 00h–11h are valid in the RDS1 command field AD00:04.
RDS2	60h–70h	RDS2 is a 1-byte command which is used to initiate a 2-byte READ sequence. This activity is accomplished by moving the contents of the two consecutive registers, starting with the one identified by the address portion of the command (AD00:AD04), to the output registers. Only Addresses 00h–10h are valid in the RDS2 command field AD00:04.
WRxx	C0h–D1h, XXh	The WRITE commands require 2 bytes to execute. The first byte is the WRITE command includes the Z86230 register address (AD00:04) being written. The second byte (XXh) is the data to be written.
RBS	FDh, 0Xh	RBS is 2-byte command to select the READ data bank. The 2 LSBs of the second byte (0Xh) select one of four banks of up to 33 bytes. Subsequent I^2C READs interpret data from this bank.

TABLE 30. SUMMARY OF Z86230 INTERNAL REGISTERS

Register Name	Addr	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Serial Status Register (SSR)	None	RDY	DAV	res	WOVR	INTR	ROVR	FLD	LOCK
Configuration	00h	res	res	res	res	res	res	res	TVS
XDS Data Activity	04h	res	res	res	res	res	res	XDS	res
XDS Filter	05h	s_2	s_1	s_0	PUBL	MISC	CHAN	FUTR	CURR
Interrupt Request Register	06h	res	res	dXDS	res	dLOK	EOF	DLE	res
Interrupt Mask Register	07h	res	res	dXDS	res	dLOK	EOF	DLE	DAV
Content Advisory Rating Select 1	08h	res	Not Rated	X	NC-17	R	PG-13	PG	G
Content Advisory Rating Select 2	09h	res	NONE	TV-MA	TV-14	TV-PG	TV-G	TV-Y7	TV-Y
Content Advisory Rating Select 3	0Ah	TV-MA V	TV-14 V	TV-PG V	TV-Y7 FV	res	TV-MA S	TV-14 S	TV-PG S
Content Advisory Rating Select 4	0Bh	res	TV-MA L	TV-14 L	TV-PG L	res	res	TV-14 D	TV-PG D
Content Advisory1	0Ch	B	1	D	a1	a0	r2	r1	r0
Content Advisory 2	0Dh	P	1	(F)V	S	L	g2	g1	g0
Blocking Control 1	0Eh	BLEN				BTE			
Content Advisory Rating Select 5	0Fh	res	18+	14+	PG	G	C8+	C	E
Content Advisory Rating Select 6	10h	res	res	18ans+	16ans+	13ans+	8ans+	G	E
Blocking Control 2	11h	res	res	res	res	res	res	res	BNR

NOTE: All register bits marked as *res* must be set to Low(0).

6.4 PROGRAM BLOCKING MAP

The following matrices demonstrate the program-blocking response of the Z86230. The first column lists the possible entries into the Content Advisory Rating registers. The first row lists the ratings that might be recovered from the received Content Advisory packet. Blocking action is indicated by the black boxes.

Each matrix shows the response to the possible user selections entered into the Content Advisory Rating registers when programs having specific Content Advisory packets are received. For example, as shown in the TV Parental Guidelines Rating matrix, entering the viewer selection from TV-PG D in register 09B causes blocking whenever the received Content Advisory packet is TV-PG D, TV-PG VD, TV-PG SD, TV-PG LD, TV-PG VSD, TV-PG VLD, TV-PG SLD or TV-PG VSLD.

Table 31. MPAA Matrix (Use Content Advisory Rating Register 08h)

	G	PG	PG-13	R	NC-17	X	NR
G	■						
PG		■					
PG-13			■				
R				■			
NC-17					■		
X						■	
NR							■

TABLE 32. TV PARENTAL GUIDELINES MATRIX (USE CONTENT ADVISORY RATING REGISTER 09h, 0Ah, 0Bh)

	Y	Y7		G	PG															
	–	–	FV	–	–	V	S	L	D	VS	VL	VD	SL	SD	LD	VSL	VSD	VLD	SLD	VSLD
Y	■																			
Y7		■																		
Y7-FV			■																	
G				■																
PG					■															
PG-V						■				■	■	■				■	■	■		■
PG-S							■			■			■	■		■	■		■	■
PG-L								■			■		■		■	■		■	■	■
PG-D									■			■		■	■		■	■	■	■
14																				
14-V																				
14-S																				
14-L																				
14-D																				
MA																				
MA-V																				
MA-S																				
MA-L																				

	14															
	–	V	S	L	D	VS	VL	VD	SL	SD	LD	VSL	VSD	VLD	SLD	VSLD
Y																
Y7																
Y7-FV																
G																
PG																
PG-V																
PG-S																
PG-L																
PG-D																
14	■															
14-V		■				■	■	■				■	■	■		■
14-S			■			■			■	■		■	■		■	■
14-L				■			■		■		■	■		■	■	■
14-D					■			■		■	■		■	■	■	■
MA																
MA-V																
MA-S																
MA-L																

	MA							
	–	V	S	L	VS	VL	SL	VSL
Y								
Y7								
Y7-FV								
G								
PG								
PG-V								
PG-S								
PG-L								
PG-D								
14								
14-V								
14-S								
14-L								
14-D								
MA	■							
MA-V		■			■	■		■
MA-S			■		■		■	■
MA-L				■		■	■	■

NOTE: “–” denotes a base rating.

TABLE 33. CANADIAN ENGLISH MATRIX (USE CONTENT ADVISORY RATING REGISTER 0Fh)

	E	C	C8+	G	PG	14+	18+
E	■						
C		■					
C8+			■				
G				■			
PG					■		
14+						■	
18+							■

TABLE 34. CANADIAN FRENCH MATRIX (USE CONTENT ADVISORY RATING REGISTER 10h)

	E	G	8ans+	13ans+	16ans+	18ans+
E	■					
G		■				
8ans+			■			
13ans+				■		
16ans+					■	
18ans+						■

7. DEMONSTRATION PROGRAMS

7.1 COMMUNICATING WITH THE Z86230

Communications with the Z86230 is accomplished using its serial communications interface (it is assumed that the user is familiar with the serial protocol requirements).

NOTE: In the following descriptions, <ENTER> means "press the Enter key".

7.2 I^2C OPERATION

The Z86230 is configurable as an I^2C slave device. The PC communicates with the Z86230 through its parallel port. Though these programs are not intended as examples of how to program the application they do provide a means of illustrating the serial control process and capability of the Z86230.

The three programs available are titled IICO, SCRIPTI and XDSCAP. These programs compile and run satisfactorily with the Z86230 in a test board. Compiled versions are available on disk. Contact your local ZiLOG sales office for further information on these programs.

7.3 IICO PROGRAM

This program sends 1 byte to the Z86230 without checking the status of the RDY bit. The program returns the contents of the Serial Status Register (SSR) after the command is entered. When the program is active the screen displays:

IIC Command Byte >

The user may enter any valid 1-byte command such as FBh (RESET) or 00h (NOP) and then hit the ENTER key. The screen then displays the byte entered and the SSR contents as follows:

IIC Byte = 00

IIC Status = 83h

This example shows that the NOP command was entered. The SSR contents, 83h, indicate that the RDY, FLD, and LOCK bits are High, which implies that the serial port is ready for further input, that the input video signal was in Field 1 at the time the status was read, and that the part is operating in video lock mode.

The IICO program is exited by entering a Control+C (^C) character.

For example, entering the following two 1-byte commands displays the following:

Reset the part FB, 00

7.4 GENERAL COMMANDS

Serial Command	Command Code
RESET	FBh, FCh, 00h
NOP	00h
SSB	FFh,...FFh,FEh

7.5 SCRIPTI PROGRAM

This program is designed to send any number of 1 or 2-byte commands to the Z86230. The list of commands to be executed are contained in Script files that have the extension .SER. For example, a file called FILFA.SER contains the 1-byte command:

{C5, 02} * Set xds filter to all future class

The program is invoked by typing: SI File_name <ENTER>

NOTE: File_name without the .SER extension.

The screen displays:

EEG CCD2 Serial Interface Script Player Version x.xx

Slave Address is 28h

Script File Done

The responding slave address is reported to the screen. When all of the commands in the file are successfully sent to the Z86230, the PC returns to the system prompt.

The program checks the RDY status before sending each byte. If, during the entry of a command, the RDY bit is not found to be a 1 after an extended wait, the program reports the contents of the SSR and then continues checking for RDY.

7.6 SCRIPT FILES

Script files can be generated to perform all of the setup and control functions required to use the part in an application. The script files shown in the following pages are examples used to set up the Z86230 for different operating conditions. Some of the files contain only a single command while others include several commands. The user should refer to Z86230 Commands and Registers Summary for details. Although the following examples are organized according to a particular register, some of the files contain information for several registers.

7.6.1 Configuration Register Script Files

TABLE 35. CONFIGURATION REGISTER SCRIPT FILES

File Name	Command	Function
FIGVH	{C7,00}	Set INT Mask register clear
	{83,12}	Bit set ext V pulse for pos
FIGN	{C0,00}	Set config back to default state
FIGPAL	{C0,01}	Set config register to TVS=1. Changes VBI line to L22 PAL.

7.6.2 XDSCAP Program

This program performs the task of XDS data recovery. XDS recovery must first be enabled through the appropriate XDS Filter command. Script file examples for setting the XDS Filter are shown below.

The program is invoked by typing: SI File_name <ENTER>

When the program is invoked, the PC screen displays:

EEG CCD2 XDS Data Recovery Test Program Version x.xx

Slave Address is 28h

The responding slave address is reported to the screen.

When communication is acknowledged, the program displays all XDS data recovered from those packets that were enabled through the XDS Filter command:

{01,03}Current Program{00}{0F,7F}....etc

The ASCII characters are displayed as ASCII characters, while the nonprinting characters are displayed by their Hex values within curly braces. Byte pairs, such as Class, Type, are shown as pairs within the curly braces, separated by a comma, for example: {01,03}.

If no data is received within approximately 45 seconds, the program times out, reports Data Not Available, and exits.

NOTE: The XDSCAP program can also be exited by entering a Control+C (^C) character.

7.6.3 XDS Filter Register Script Files

File Name	Command	Function
FILA	{C5,1F}	Set XDS filter to all
FIL0	{C5,00}	Set XDS filter to none; turns off XDS recovery
FILCA	{C5,01}	Set XDS filter to all current class
FILC	{C5,41}	Set XDS filter to current, in band class
FILFA	{C5,02}	Set XDS filter to all future class
FILCH	{C5,04}	Set XDS filter to channel class
FILM	{C5,08}	Set XDS filter for misc. info
FILTIME	{C5,28}	Set XDS filter time only
FILVCR	{C5,9E}	Set XDS filter vcr info

8. ELECTRICAL CHARACTERISTICS

8.1 ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to 6.0	V
V_{IN}	DC Input Voltage	–0.5 to V_{DD} +0.5	V
V_{OUT}	DC Output Voltage	–0.5 to V_{DD} +0.5	V
I_{IN}	**CAUTION:** DC Input Current per Pin	+10	mA
I_{OUT}	DC Output Current per Pin	+20	mA
I_{DD}	DC Supply Current	+30	mA
P_D	Power Dissipation per Device	300	mW
T_{STG}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

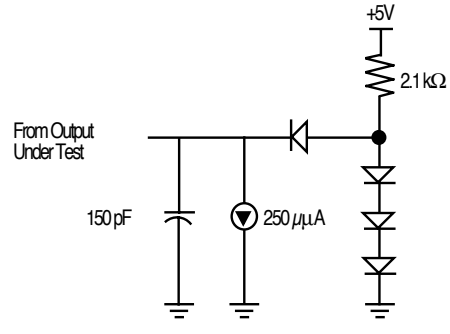
Notes:

1. Voltages referenced to V_{SS} (A).
   Maximum ratings are those values beyond which damage to the device may occur.
   Functional operation should be restricted to the limits specified in the DC and AC Characteristics tables or Pin Description section.

8.2 STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

FIGURE 7. STANDARD TEST LOAD



8.3 DC CHARACTERISTICS

TABLE 36. DC CHARACTERISTICS—T_A = 0°C to +70°C; V_{DD} = +4.75V to +5.25V

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{IL}	Input Voltage Low		0	0.2 V_{DD}	V
V_{IH}	Input Voltage High		0.7 V_{DD}	V_{DD}	V
V_{OL}	Output Voltage Low	I_{OL} = 1.00 mA	–	0.4	V
V_{OH}	Output Voltage High	I_{OH} = 0.75 mA	V_{DD} –0.4V	–2	V
I_{IL}	Input Leakage	0V, V_{DD}	–3.0	3.0	mA
I_{DD}	Supply Current			30	mA
Kf	VCO Gain		–	TBD	MHz/V
I_{LP}	Loop Filter Current		–	TBD	mA

8.4 AC AND TIMING CHARACTERISTICS

8.4.1 Composite Video Input

TABLE 37. COMPOSITE VIDEO INPUT

Parameter	Conditions
Amplitude	1.0V p-p ±3 dB
Polarity	Sync tips negative
Bandwidth	600 kHz
Signal Type	Interlaced
Max Input R	470 ohms
DC Offset	Signal must be AC-coupled with a minimum series capacitance of 0.1 µF

8.5 ELECTRICAL CHARACTERISTICS

8.5.1 Non-Standard Video Signals

Non-standard video signals must have the following characteristics:

TABLE 38. NON-STANDARD VIDEO SIGNALS

Parameter	Conditions
Sync Amplitude	200 mV minimum
Vertical Pulse Width	3H ±0.5H
Vertical Pulse Tilt	20 mV maximum

TABLE 38. NON-STANDARD VIDEO SIGNALS

Parameter	Conditions
H Timing	Phase Step (Head Switch) ±10 µs maximum Fh Deviation (long term) ±0.5% maximum Fh p-p Deviation (short term) ±0.3% maximum
Vertical Sync Signal	The internal sync circuits lock to all 525- or 625-line signals that exhibit a vertical sync pulse that meets the following conditions: 1. It is at least 3H ±0.5H wide. 2. It starts at the proper 2H boundary for its field. 3. If equalizing pulse serrations are present, they must be less than 0.125H in width.
Minimum Signal-to-Noise	The Z86230 functions down to a 25 dB signal-to-noise ratio (CCIR-weighted) with one error per row or better at that level.
Ratio to Composite Video	Input

8.5.2 HIN/XIN Signal Input

Table 39. HIN/XIN Signal Input

Mode		Parameter	Conditions
1. HIN Input	(Video Lock Mode)	Amplitude	CMOS level signal where Low ≤ 0.2 V_{CC}
		Polarity	Any
		Frequency	15,734.263 Hz @ 3%
	(HIN Lock Mode)	Amplitude	CMOS level signal where Low ≤ 0.2 V_{CC}
		Polarity	Any
		Frequency	Same as Display Horizontal Flyback (HFB) pulse
2. XIN Input	(XTAL)	Frequency	32.768 KHz
		Frequency tolerance	±20ppm @ T_A = 25C, CL = 12.5pF
	(Clock)	Amplitude	CMOS level signal where Low ≤ 0.2 V_{CC}
		Frequency	32.768 kHz ±2%

8.5.3 Line 21 Input Parameters (at 1.0V p-p)

Line 21 must be in its proper position to the leading edge of the Vertical Sync signal.

TABLE 40. LINE 21 INPUT PARAMETERS

Parameter	Conditions
Code Amplitude	50 IRE*
Code Zero Level	5 IRE, +15 IRE relative to Back Porch
Start of Code	10.5 ±0.5 µs (measure from the midpoint of the leading edge of the composite video Hsync pulse to the midpoint of the rising edge of the first clock run-in cycle.)
Start of the Data	3.972 ms, –0.00 µs, +0.30 µs (measure from the midpoint of the falling edge of the most recent clock run-in cycle to the midpoint of the rising edge of the start bit.)

NOTE: *A relative unit of measure developed by the Institute of Radio Engineers (IRE). One IRE equals 1/140th of the composite video signal's peak-to-peak voltage. IRE is the former name of what is now known as the Institute of Electrical and Electronics Engineers (IEEE).

9. APPLICATION INFORMATION

The recommended schematic, component placement, and PCB layout for a single-sided DIP design are provided in the following figures. I^2C communication and XTAL mode are chosen in the reference circuit design. EMI and noise in the video frequency range is kept to an absolute minimum by running the ground plane underneath the entire Z86230 package length. This design is recommended for both SOIC and DIP package styles.

9.1 REFERENCE DESIGNS

FIGURE 8. Z86230 REFERENCE CIRCUIT

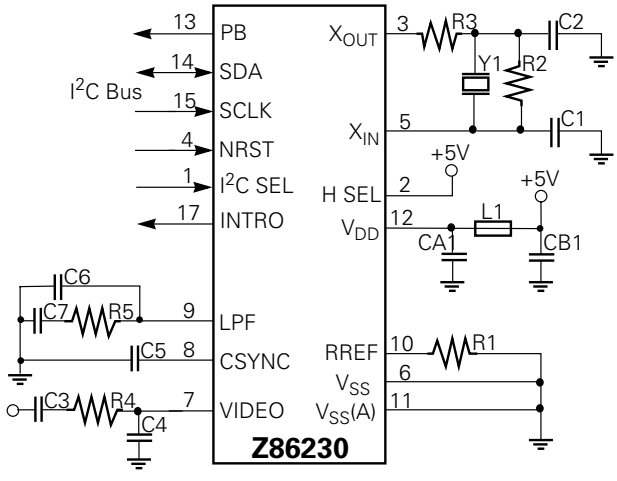
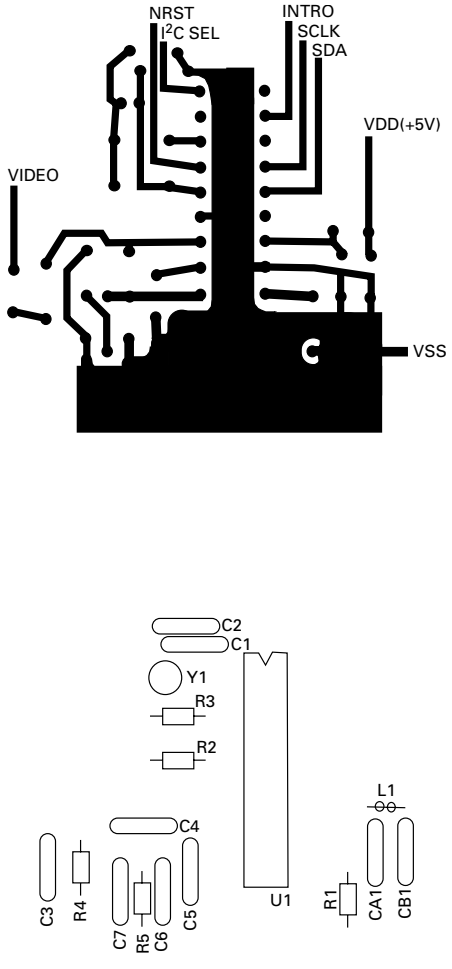


TABLE 41. RECOMMENDED COMPONENT VALUES FOR Z86230 REFERENCE CIRCUIT

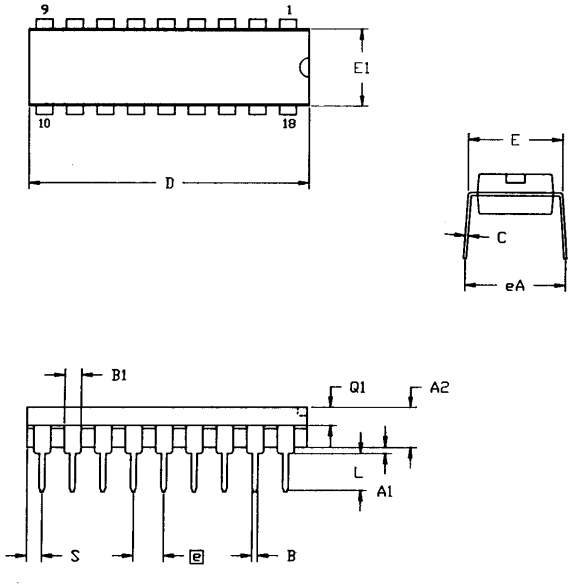
Component	Value	Units
R1	10	KΩ
R2	22	MΩ
R3	470	KΩ
R4	470	Ω
R5	6.8	KΩ
C1	10	pF
C2	20	pF
C3	0.1	µF
C4	560	pF
C5	0.1	µF
C6	6800	pF
C7	0.068	µF
CA1	0.1	µF
CB1	0.1	µF
L1	bead	N/A
Y1	32.768	kHz
U1	Z86230	N/A

FIGURE 9. PCB DESIGN OF Z86230 REFERENCE CIRCUIT



10. PACKAGING

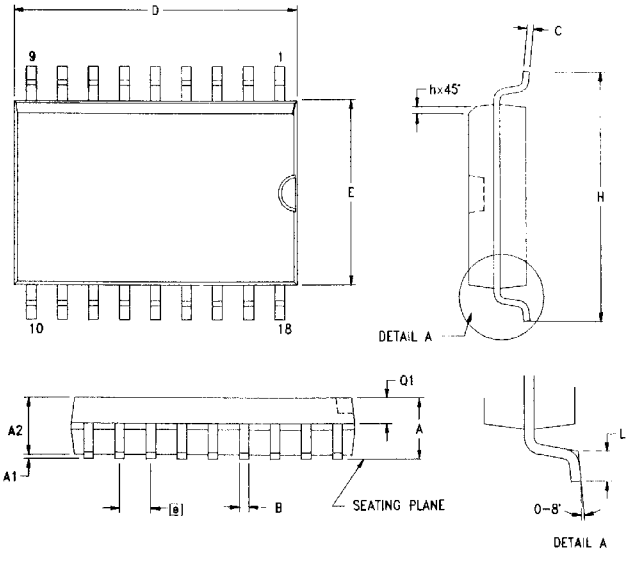
FIGURE 10. 18-LEAD DIP PACKAGE DIAGRAM



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

FIGURE 11. 18-LEAD SOIC PACKAGE DIAGRAM



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

11. ORDERING INFORMATION

Z86230 (12 MHz)	
Standard Temperature	
18-Pin DIP	18-Pin SOIC
Z8623012PSC	Z8623012SSC

For fast results, contact your local ZiLOG sale offices for assistance in ordering the part(s) required.

11.1 PART NUMBER DESCRIPTION

The ZiLOG part numbers consist of a number of components.

EXAMPLE: Part number Z86230 12 P S C is a Z86230, 12-MHz DIP, 0ºC to +70ºC, Plastic Standard Flow, and consists of the codes indicated in the following table.

Z	ZiLOG prefix
86230	Product Number
12	Speed (in MHz)
P	Package
S	Temperature
C	Environmental Flow

12. PRECHARACTERIZATION PRODUCT

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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Campbell, CA 95008
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Internet: http://www.zilog.com

CUSTOMER FEEDBACK FORM

Z86230 PRODUCT SPECIFICATION

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see Return Information, below). We also welcome your suggestions!

CUSTOMER INFORMATION

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

PRODUCT INFORMATION

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

RETURN INFORMATION

ZiLOG
System Test/Customer Support
910 E. Hamilton Avenue, Suite 110, MS 4–3
Campbell, CA 95008
Fax: (408) 558-8536
Email: tools@zilog.com

PROBLEM DESCRIPTION OR SUGGESTION

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

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