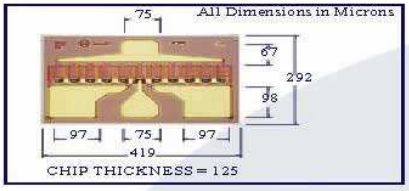
MwT-A9

18 GHz High Gain, Low Noise GaAs FET

DOWNLOAD ADDITIONAL DATA WWW.MWTINC.COM



FEATURES

- IDEAL FOR HIGH DYNAMIC RANGE RECEIVER APPLICATIONS
- 1.6 dB NOISE FIGURE AT 12 GHz
- +24.5 dBm OUTPUT POWER AT 12 GHz
- 9 dB SMALL SIGNAL GAIN AT 12 GHz
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- 750 MICRON GATE WIDTH
- AVAILABLE IN CHIP AND PACKAGES

DESCRIPTION

The MwT-A9 is a GaAs MESFET device whose nominal quarter-micron gate length and 750 micron gate width make it ideally suited to applications requiring high-gain in the 500 MHz to 18 GHz frequency range with moderate power output while exhibiting low noise figure. The chip is produced using MwT's reliable metal system and devices from each wafer are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability, Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

DC SPECIFICATIONS AT Ta = 25°C

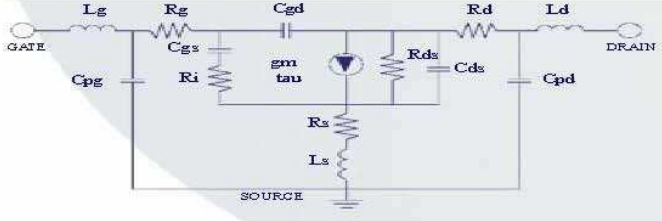
SYMBOL	PARAM. & CONDITIONS	UNITS	MIN	TYP	MAX
IDSS	Saturated Drain Current Vds= 4.0 V VGS= 0.0 V	mA	78		282
Gm	Transconductance Vds= 2.0 V VGS= 0.0 V	mS	95	120	
Vp	Pinch-off Voltage Vds= 3.0 V IDS= 5.0 mA	V		-2.0	-5.0
BVGSO	Gate-to-Source Breakdown Volt. Igs= -1.0 mA	V	-5.0	-10.0	
BVGDO	Gate-to-Drain Breakdown Volt. Igd= -1.0 mA	V	-6.0	-10.0	
Rth	Thermal Resistance MwT-A9 Chip, A971 / MwT-A970, A973	°C/W		70 175*	

*Overall Rth depends on case mounting.

RF SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1 dB Compression VDS= 5.0 V Idss= 0.6 IDS=120mA	12 GHz	dBm	23.0	24.5
SSG	Small Signal Gain VDS= 5.0 V Idss= 0.6 IDS=120mA	12 GHz	dB	8.5	9.0
NFopt	Optimum Noise Figure VDS= 3.0V IDS= 30mA	12 GHz	dB		1.8
GA	Gain at Optimum Noise Figure VDS= 3.0V IDS= 30mA	12 GHz	dB	6.0	6.5

DEVICE EQUIVALENT CIRCUIT MODEL



PARAMETER		VALUE	
Source Resistance	Rs	0.80	Ω
Source Inductance	Ls	0.04	nH
Drain-Source Resistance	Rds	100.0	Ω
Drain-Source Capacitance	Cds	0.08	pF
Drain Resistance	Rd	1.0	Ω
Drain Pad Capacitance	Cpd	0.10	pF
Drain Inductance	Ld	0.28	nH
Gate Bond Wire Inductance	Lg	0.10	nH
Gate Pad Capacitance	Cpg	0.03	pF
Gate Resistance	Rg	0.50	Ω
Gate-Source Capacitance	Cgs	0.78	pF
Channel Resistance	Ri	0.8	Ω
Gate-Drain Capacitance	Cgd	0.10	pF
Transconductance	gm	120.0	mS
Transit Time	tau	1.0	psec

ORDERING INFORMATION

Chip	MwT-A9
Package 70	MwT-A970
Package 71	MwT-A971
Package 73	MwT-A973

NOTE:
For Package information, please see supplimentary application note from our website at www.mwtinc.com. When placing an order or inquiry, please specify BIN range, wafer no. if known, and screening level required.

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MwT-A9
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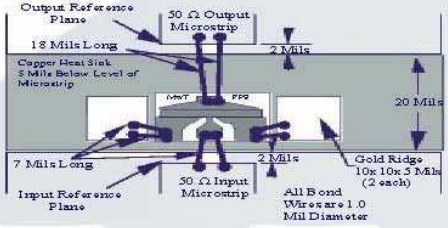
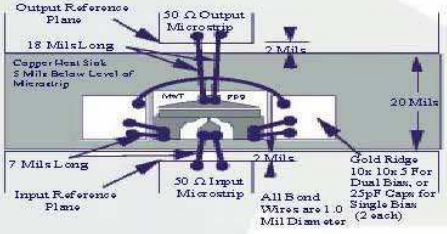
MwT-9 And A9
DUAL BIAS



MwT-9 And A9
OPTIONAL BONDING



SAFE OPERATING LIMITS vs. BACKSIDE CHIP

Absolute Maximum Continuous Maximum

MAXIMUM RATINGS AT Ta = 25°C

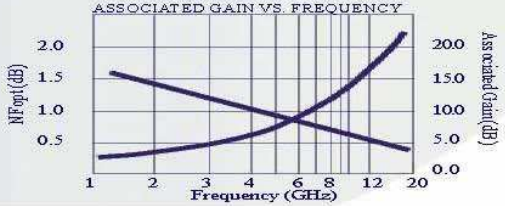
SYMBOL	PARAMETER	UNITS	CONT MAX'	ABSOLUTE MAX'
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	240	360

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

TYPICAL NOISE PARAMETERS
MwT-A9LN Chip: VDS= 3.0V IDS= 35mA

FREQUENCY GHz	NF MIN dB	GAMMA OPT MAG	GAMMA OPT ANGLE	Rn/50
1.00	0.30	0.85	4.5	0.19
2.00	0.33	0.69	36.8	0.18
4.00	0.62	0.56	73.4	0.19
6.00	0.93	0.52	106.3	0.19
10.00	1.48	0.57	152.0	0.17
12.00	1.73	0.61	167.3	0.17
16.00	2.19	0.68	-169.8	0.16
18.00	2.40	0.71	-160.8	0.15

NOISE FIGURE AND
ASSOCIATED GAIN VS. FREQUENCY



Bin Selection Guide

Bin No.	A	B	C	D	E
Idss Range	78-114mA	114-150mA	150-198mA	198-234mA	234-294mA

BIN ACCURACY STATEMENT

When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

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