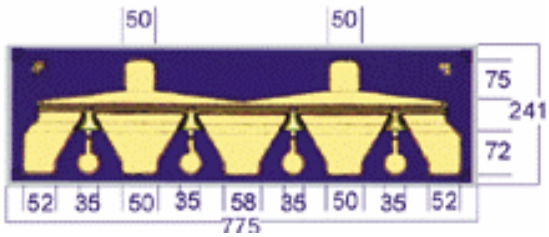
# MwT-PH15

**28 GHz Medium Power AlGaAs/InGaAs PHEMT**
**June 2006**

## Features:

- **+28.5 dBm typical Output Power at 12 GHz**
- **12 dB typical Small Signal Gain at 12 GHz**
- **60% typical PAE at 12 GHz**
- **0.3 x 630 Micron Refractory Metal/Gold Gate**
- **Sorted into 10 mA Idss Bin Ranges**
- **Excellent for High Power, Gain, and High Power Added Efficiency**
- **Ideal for Commercial, Military, Hi-Rel Space Applications**




**Chip Dimensions: 775 x 241 microns**
**Chip Thickness: 100 microns**

## Description:

The MwT-PH15 is a AlGaAs/InGaAs PHEMT (Pseudomorphic-High-Electron-Mobility-Transistor) device whose nominal 0.3 micron gate length and 630 micron gate width make it ideally suited for applications requiring high-gain and power up to 28 GHz frequency range with power outputs ranging from 500 to 700 milli-watts. The device is equally effective for either wideband (e.g. 6 to 18 GHz) or narrow-band applications. The chip is produced using MwT's reliable metal systems and all devices from each wafer are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability.

## Electrical Specifications:

- ***at Ta= 25 ℃***

| SYMBOL | PARAMETERS & CONDITIONS | FREQ | UNITS | MIN | TYP |
|---|---|---|---|---|---|
| **P1dB** | Output Power at 1dB Compression<br>Vds=7.0 V Ids=0.75xIDSS=150 mA | 12 GHz<br>18 GHz | dBm | 27.0 | 28.5<br>28.5 |
| **SSG** | Small Signal Gain<br>Vds=7.0 V Ids=0.75xIDSS=150 mA | 12 GHz<br>18 GHz | dB | 10.0 | 12.0<br>9.5 |
| **PAE** | Power Added Efficiency at P1dB<br>Vds=7.0 V Ids=0.75xIDSS=150 mA | 12 GHz | % | | 60 |
| **IDSS** | Recommended IDSS Range<br>for Optimum P1dB | | mA | | 140 - 220 |

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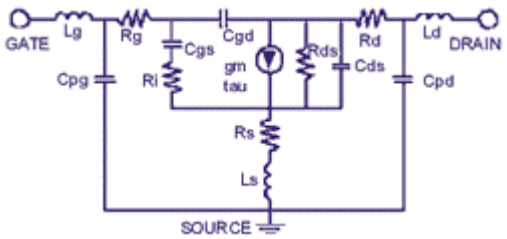
## DC Specifications:

- *at Ta= 25 ℃*

| SYMBOL | PARAMETERS & CONDITIONS | UNITS | MIN | TYP | MAX |
|---|---|---|---|---|---|
| **IDSS** | Saturated Drain Current<br>Vds=4.0 V Vgs=0.0 V | mA | 120 | | 240 |
| **Gm** | Transconductance<br>Vds=2.5 V Vgs=0.0 V | mS | 130 | 200 | |
| **Vp** | Pinch-off Voltage<br>Vds=3.0 V Ids=2.0 mA | V | | -1.2 | -2.5 |
| **BVGSO** | Gate-to-Source Breakdown Voltage<br>Igs= -0.7 mA | V | -6.0 | -10.0 | |
| **BVGDO** | Gate-to-Drain Breakdown Voltage<br>Igd= -0.7 mA | V | -10.0 | -13.0 | |
| **Rth** | Chip Thermal Resistance | C/W | | 65* | |

* Overall Rth depends on case mounting

**DEVICE EQUIVALENT CIRCUIT**




| PARAMETER | | VALUE | |
|---|---|---|---|
| Source Resistance | Rs | 0.10 | ohm |
| Source Inductance | Ls | 0.03 | nH |
| Drain-Source Resistance | Rds | 200 | ohm |
| Drain-Source Capacitance | Cds | 0.12 | pF |
| Drain Resistance | Rd | 0.84 | ohm |
| Drain Pad Capacitance | Cpd | 0.05 | pF |
| Drain Inductance | Ld | 0.10 | nH |
| Gate Bond Wire Inductance | Lg | 0.07 | nH |
| Gate Pad Capacitance | Cpg | 0.20 | pF |
| Gate Resistance | Rg | 0.10 | ohm |
| Gate-Source Capacitance | Cgs | 1.30 | pF |
| Channel Resistance | Ri | 2.30 | ohm |
| Gate-Drain Capacitance | Cgd | 0.07 | pF |
| Transconductance | gm | 200 | mS |
| Transit Time | tau | 2.60 | psec |

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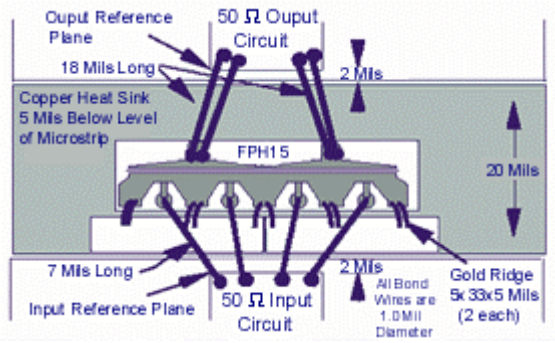
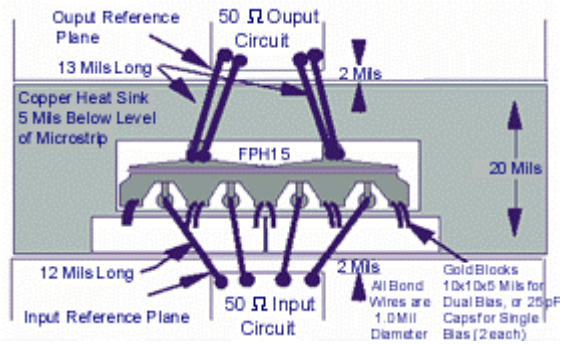
MwT-PH15
DUAL BIAS




MwT-PH15
SELF BIAS




### MAXIMUM RATINGS AT Ta = 25 °C

| Symbol | Parameter | Units | Cont Max1 | Absolute Max2 |
|---|---|---|---|---|
| VDS | Drain to Source Volt. | V | 7.5 | 8.0 |
| Tch | Channel Temperature | °C | +150 | +175 |
| Tst | Storage Temperature | °C | -65 to+150 | +175 |
| Pin | RF Input Power | mW | 200 | 300 |
| Pt | Total Power Dissipation | mW | 1900 | 2300 |

**Notes:**

**1.** Exceeding any one of these limits in continuous operation may reduce the mean-time- to-failure below the design goal.

**2.** Exceeding any one of these limits may cause permanent damage.

### BIN SELECTION

| BIN# | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IDSS (mA) | 120-130 | 130-140 | 140-150 | 150-160 | 160-170 | 170-180 | 180-190 | 190-200 | 200-210 | 210-220 | 220-230 | 230-240 |

**BIN ACCURACY STATEMENT:** Due to the effects of temperature, dc loading and probe tip varnishing, the IDSS from the "on wafer" probing of any MwT device may differ After it has been attached to a proper heat sink and tested in an RF or DC circuit. Because of the aforementioned effects, the IDSS distribution may deviate as much as +/- 1 bin within the range identified on the label of Each die shipping container, and +/- 2 bins within the selected range.

### ORDERING INFORMATION:

When placing order or inquiring, please specify BIN range, wafer number, if known, and visual screening level required. For details of BIN Selection and Safe Handling Procedure please see supplementary information in available PDF on our website www.mwtinc.com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