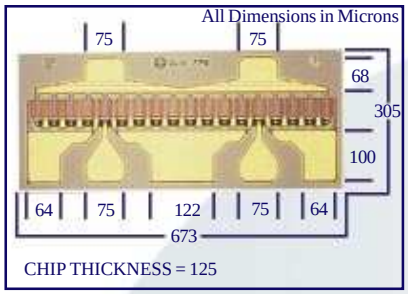
MwT-8

16 GHz High Power GaAs FET

DOWNLOAD ADDITIONAL DATA WWW.MWTINC.COM



FEATURES

- 0.6 WATT POWER OUTPUT AT 12 GHz
- +40 THIRD ORDER INTERCEPT
- HIGH ASSOCIATED GAIN
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- 1200 MICRON GATE WIDTH
- CHOICE OF CHIP AND ONE PACKAGE TYPE

DESCRIPTION

The MwT-8 is a GaAs MESFET device which is ideally suited to narrow-band applications such as cellular telephone, PCN, point-to-point communications links, and other wireless applications as the driver transistor for the output power amplifier. The third-order intercept performance of the MwT-8 is excellent, typically 12 dB above the 1 dB compression point. The chip is produced using MwT's reliable metal system and devices from each wafer are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability, Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

DC SPECIFICATIONS AT Ta = 25°C

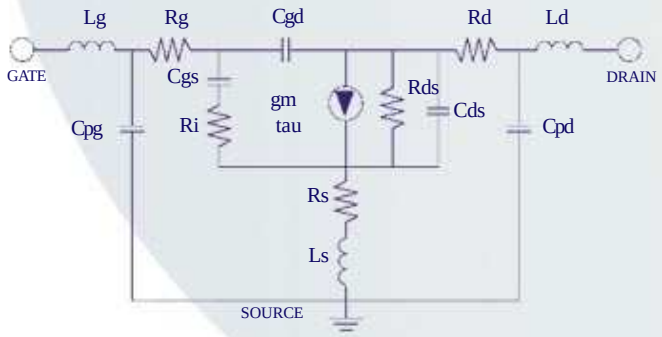
SYMBOL	PARAM. & CONDITIONS	UNITS	MIN	TYP	MAX
IDSS	Saturated Drain Current Vds= 4.0 V VGS= 0.0 V	mA	120		480
Gm	Transconductance Vds= 2.0 V VGS= 0.0 V	mS	144	160	
Vp	Pinch-off Voltage Vds= 3.0 V IDS= 5.0 mA	V		-2.0	-5.0
BVGSO	Gate-to-Source Breakdown Volt. Igs= -0.8 mA	V	-6.0	-12.0	
BVGDO	Gate-to-Drain Breakdown Volt. Igd= -0.8 mA	V	-8.0	-12.0	
Rth	Thermal Resistance MwT-8 Chip, MwT-871,	°C/W		45 60*	

*Overall Rth depends on case mounting.

RF SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1 dB Compression VDS= 6.0 V IDS=180mA	12 GHz	dBm	27.0	28.0
PAE	Power Added Efficiency VDS= 6.0 V IDS=180mA	12 GHz	%	25	35
SSG	Small Signal Gain VDS= 6.0V IDS= 180mA	12 GHz	dB	7	7.5
IDSS	Recommended IDSS Range for Optimum P1dB		mA		320-440

DEVICE EQUIVALENT CIRCUIT MODEL



PARAMETER		VALUE	
Source Resistance	Rs	0.3	Ω
Source Inductance	Ls	0.055	nH
Drain-Source Resistance	Rds	60.0	Ω
Drain-Source Capacitance	Cds	0.1	pF
Drain Resistance	Rd	0.3	Ω
Drain Pad Capacitance	Cpd	0.2	pF
Drain Inductance	Ld	0.1	nH
Gate Bond Wire Inductance	Lg	0.12	nH
Gate Pad Capacitance	Cpg	0.25	pF
Gate Resistance	Rg	0.2	Ω
Gate-Source Capacitance	Cgs	1.4	pF
Channel Resistance	Ri	1.0	Ω
Gate-Drain Capacitance	Cgd	0.05	pF
Transconductance	gm	150.0	mS
Transit Time	tau	1.0	psec

ORDERING INFORMATION

Chip	MwT-8
Package 71	MwT-871

NOTE:
For Package information, please see supplimentary application note from our website at www.mwtinc.com. When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

4268 Solar Way Fremont California 94538 Phone: (510) 651-6700 Fax: (510) 651-2208

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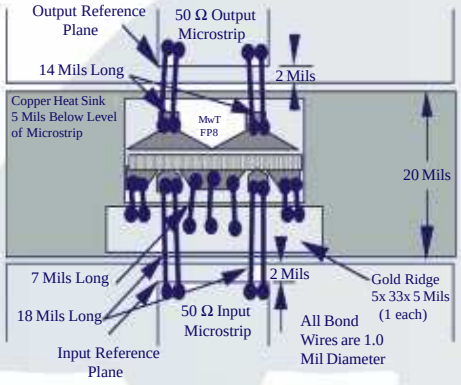
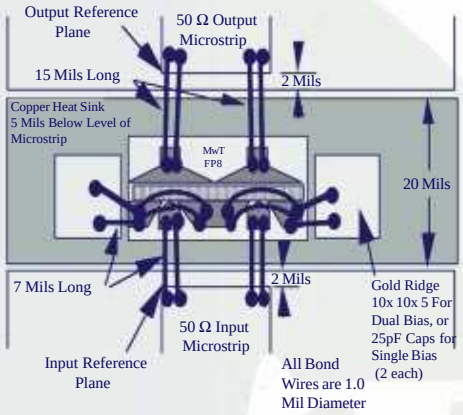
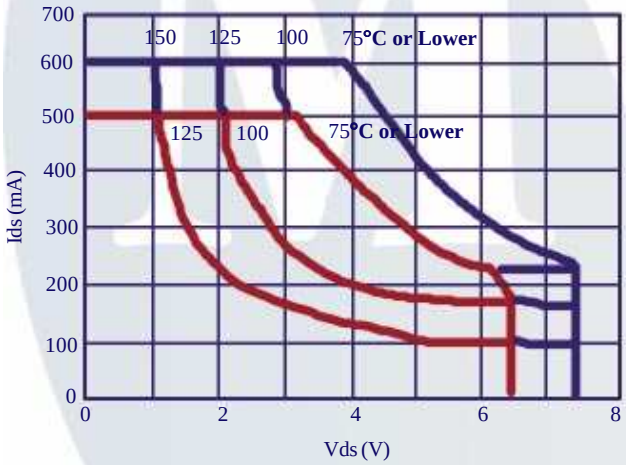
DUAL BIAS



MwT-8
OPTIONAL BONDING



SAFE OPERATING LIMITS vs. BACKSIDE CHIP



Absolute Maximum Continuous Maximum

MAXIMUM RATINGS AT Ta = 25°C

SYMBOL	PARAMETER	UNITS	CONT MAX[1]	ABSOLUTE MAX[2]
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	480	720

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

BIN SELECTION

BIN#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
IDSS (mA)	120-140	140-160	160-180	180-200	200-220	220-240	240-260	260-280	280-300	300-320	320-340	340-360	360-380	380-400	400-420	420-440	440-460	460-480

BIN ACCURACY STATEMENT

When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

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