



Features

- Very Low Noise 1.1 dB Typ.
- High +44 dBm Typ. IP3
- 14.5 dB Typical Gain
- 7.5 Volt Bias
- 26% High Power Added Efficiency

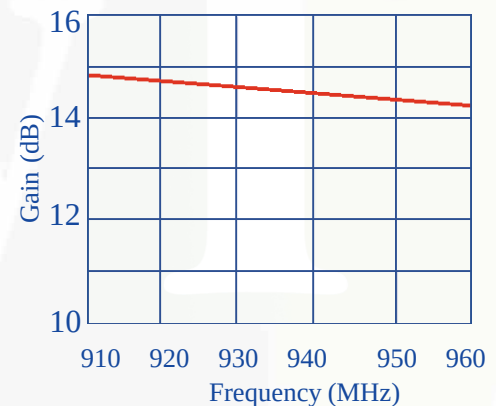
The MPS-090917P-85 is a low noise , high dynamic range amplifier designed for PDC receiver applications. The circuit is matched to 50 ohm and employs a single stage GaAs FET with internal matching to provide exceptional noise figure, 1.1 dB combined with extremely high IP3, +44 dBm. Typical applications are cellular base station receivers, Tower mounted LNA's, smart antenna systems, picocell repeaters and receiver multi-couplers.

Specifications

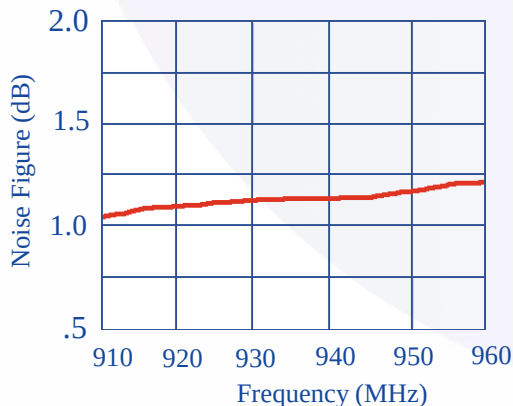
- Electrical at 25°C, Vdd= 7.5 V, Zo= 50 Ω

Symbol	Parameter	Min.	Typical	Max	Unit
Freq	Frequency Range	925		960	MHz
SSG	Small Signal Gain	13	14.5		dB
P1dB	P out at 1 dB Compression		+28.0		dBm
IP3	Third-order Intercept	+42	+44.0		dBm
NF	Noise Figure		1.1	1.5	dB
VSWR	Input VSWR		2.0:1	2.5:1	
ΔGOF	Gain Variation over Freq.		+/-0.2	+/-0.5	dB
ΔGOT	Gain Variation over Temp.		-.015		dB/°C
I _{dd}	DC Current		330	400	mA
PAE	Power Added Efficiency		26		%

Gain vs. Frequency



Noise Figure vs. Frequency



• Absolute Maximum Ratings

Maximum Bias Voltage	8.0 V
Maximum Continuous RF Input Power	950 mW
Maximum Peak Input Power	1400 mW
Maximum Case Operating Temperature	+85°C
Maximum Storage Temperature	-65°C to +150°C



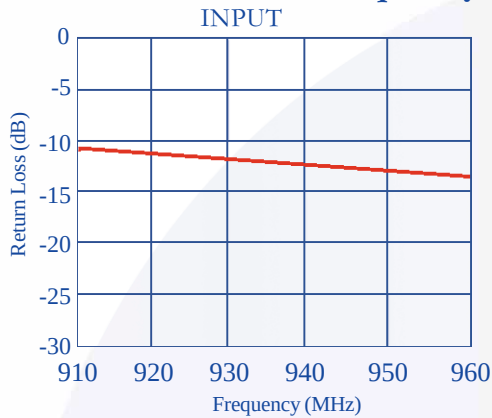
MPS-090917P-85

925 to 960 MHz Low Noise Receiver Amplifier

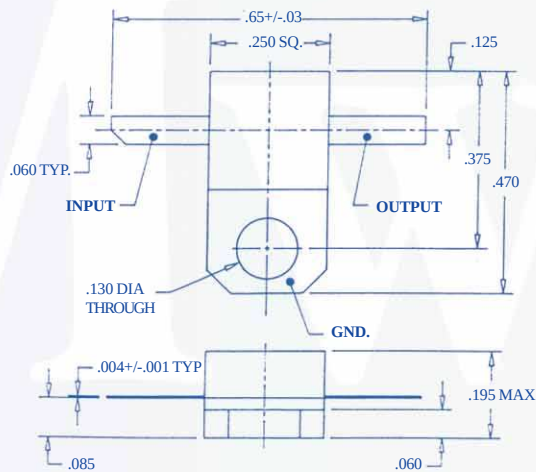
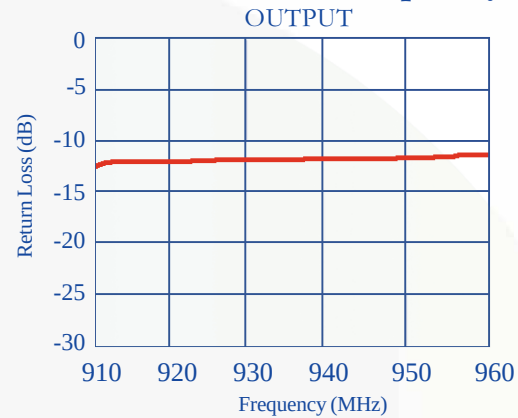
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Return Loss vs. Frequency



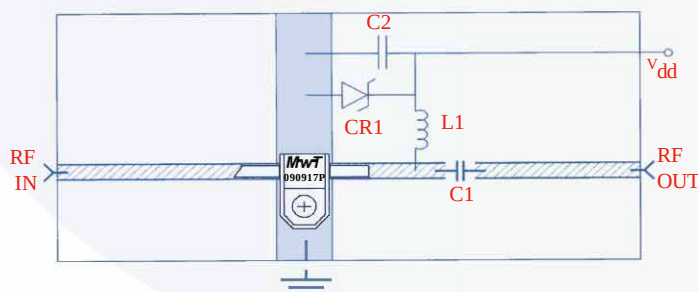
Return Loss vs. Frequency



Pin	Connection
1	N/C
2	N/C
3	RF Input
4	NC
5	N/C
6	N/C
7	N/C
8	RF Output, Vdd
9	N/C
10	N/C
Case	Ground

Outline Diagrams

Application Circuit



C1	100 pF	Chip Capacitor
C2	.22 μ F	Capacitor
L1	160 nH	Printer or Wound Coil
CR1	8.0 V	Zener Diode
		50 Ω Microstrip Line