CPC75282
Line Card Access Switch

Features
- Improved Switch dV/dt Immunity of 1500V/µs
- Smart logic for power-up/hot-plug state control
- Small 44-pin TQFP Package
- Monolithic IC reliability
- Low, matched R_{ON}
- Eliminates the need for zero-cross switching
- Flexible switch timing to transition from ringing mode to talk mode.
- Clean, bounce-free switching
- Tertiary protection consisting of integrated current limiting, voltage clamping, and thermal shutdown for SLIC protection
- 5V operation with very low power consumption
- Intelligent battery monitor
- Latched logic-level inputs, no external drive circuitry required

Applications
- VoIP Gateways
- Central Office (CO)
- Digital Loop Carrier (DLC)
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)
- Fiber In The Loop (FITL)
- Pair Gain System
- Channel Banks

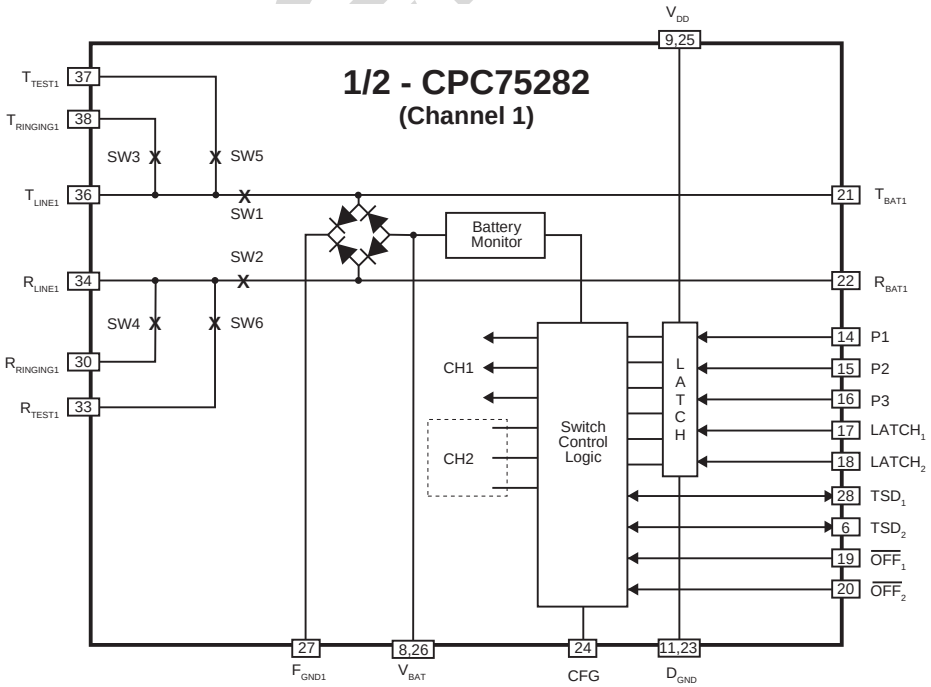
Description
The CPC75282 Dual Line Card Access Switch (LCAS), a member of Clare's next generation Line Card Access Switch family, is a monolithic solid state device that provides the switching functionality of four 2-Form-C relays in a single, small, economical package.

The CPC75282 Dual LCAS device is designed to provide ringing and test access to the telephone loop in Central Office, Digitally Added Main Line, Private Branch Exchange, Digital Loop Carrier, and Hybrid Fiber Coax/Fiber-In-The-Loop analog line card applications. Test access switches provide access to the telephone loop for line (drop) test or message waiting in the PBX application.

Ordering Information

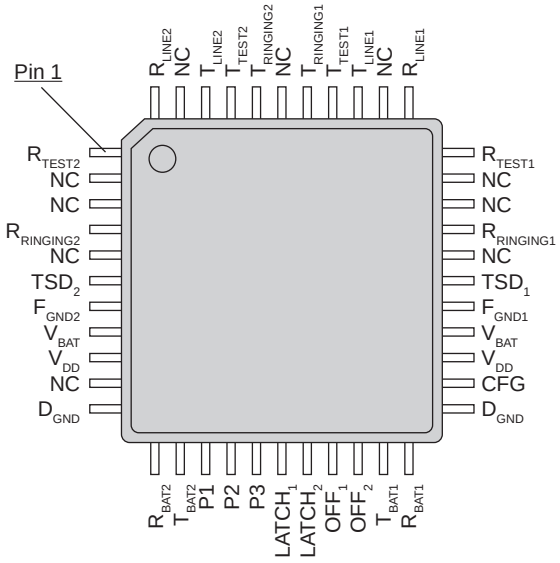
Part #	Description
CPC75282KATR	44-Pin TQFP, Tape & Reel (1000/Reel)

Figure 1. CPC75282 Block Diagram



1. Specifications

1.1 Package Pinout



1.2 Pinout by Channel

CH1	CH2	Name	Description
27	7	F_{GNDx}	Fault Ground [1]
21	13	T_{BATx}	Tip Lead to the SLIC
36	42	T_{LINEx}	Tip Lead of the Line Side
38	40	$T_{RINGINGx}$	Ringing Generator Return
37	41	T_{TESTx}	Tip Lead of the Test Bus
9, 25		V_{DD}	+5V Supply
33	1	R_{TESTx}	Ring Lead of the Test Bus
30	4	$R_{RINGINGx}$	Ringing Generator Source
34	44	R_{LINEx}	Ring Lead of the Line Side
22	12	R_{BATx}	Ring Lead to the SLIC
8, 26		V_{BAT}	Battery Supply
17	18	$LATCH_x$	Data Latch Enable Control Input
28	6	TSD_x	Temperature Shutdown Pin
19	20	$\overline{OFF}_x$	All Off Logic Level Input Switch Control [2]
11, 23		D_{GND}	Digital Ground
14		P1	Logic Control Input
15		P2	Logic Control Input
16		P3	Logic Control Input
24		CFG	Operating States Configuration
2, 3, 5, 10, 29, 31, 32, 35, 39, 43		NC	Not Connected

[1] "x" denotes channel number

[2] An internal pull-down device is included on this node to set Off as the power-up default state. These pins can also be used as a device reset. If these pins are not used, tie to V_{DD}

1.3 Pinout by Pin Number

Pin	Name	Description
1	R_{TEST2}	Ring Lead of the Test Bus
4	$R_{RINGING2}$	Ringing Generator Source
6	TSD_2	Temperature Shutdown Pin
7	F_{GND2}	Fault Ground
9	V_{DD}	+5V Supply
12	R_{BAT2}	Ring Lead to the SLIC
13	T_{BAT2}	Tip Lead to the SLIC
14	P1	Logic Control Input
15	P2	Logic Control Input
16	P3	Logic Control Input
17	$LATCH_1$	Data Latch Enable Control Input
18	$LATCH_2$	Data Latch Enable Control Input
19	$\overline{OFF}_1$	All Off Logic Level Input Switch Control
20	$\overline{OFF}_2$	All Off Logic Level Input Switch Control
21	T_{BAT1}	Tip Lead to the SLIC
22	R_{BAT1}	Ring Lead to the SLIC
24	CFG	Operating States Configuration
25	V_{DD}	+5V Supply
27	F_{GND1}	Fault Ground
28	TSD_1	Temperature Shutdown Pin
30	$R_{RINGING1}$	Ringing Generator Source
32	NC	Not Connected
33	R_{TEST1}	Ring Lead of the Test Bus
34	R_{LINE1}	Ring Lead of the Line Side
35	NC	Not Connected
36	T_{LINE1}	Tip Lead of the Line Side
37	T_{TEST1}	Tip Lead of the Test Bus
38	$T_{RINGING1}$	Ringing Generator Return
39	NC	Not Connected
40	$T_{RINGING2}$	Ringing Generator Return
41	T_{TEST2}	Tip Lead of the Test Bus
42	T_{LINE2}	Tip Lead of the Line Side
43	NC	Not Connected
44	R_{LINE2}	Ring Lead of the Line Side
9, 25	V_{DD}	+5V Supply
11, 23	D_{GND}	Digital Ground
8, 26	V_{BAT}	Battery Supply
2, 3, 5, 10, 29, 31, 32, 35, 39, 43	NC	Not Connected

1.4 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
+5V power supply (V_{DD})	-0.3	7	V
Battery Supply	-	-85	V
D_{GND} to F_{GND} Separation	-5	+5	V
Logic input voltage	-0.3	V_{DD} + 0.3	V
Logic input to switch output isolation	-	320	V
Switch open-contact isolation (SW1, SW2, SW3, SW5, SW6)	-	320	V
Switch open-contact Isolation (SW4)	-	465	V
Operating relative humidity	5	95	%
Operating temperature	-40	+110	°C
Storage temperature	-40	+150	°C

Absolute maximum electrical ratings are at 25°C.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.5 ESD Rating

ESD Rating (Human Body Model)
1000V

1.6 General Conditions

Unless otherwise specified, minimum and maximum values are production testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. They are provided for information purposes only and are not part of the testing requirements.

Specifications cover the operating temperature range T_A = -40°C to +85°C. Also, unless otherwise specified, all testing is performed with $V_{DD} = 5V_{DC}$, logic low input voltage is $0V_{DC}$ and logic high voltage is $5V_{DC}$.

1.7 Switch Specifications

1.7.1 Break Switches, SW1 and SW2

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW1} (differential) = T_{LINE} to T_{BAT} V_{SW2} (differential) = R_{LINE} to R_{BAT} All-Off state.					
	+25°C, V_{SW} (differential) = -320V to gnd V_{SW} (differential) = +260V to -60V	I_{SW}	-	-	1	µA
	+85° C, V_{SW} (differential) = -330V to gnd V_{SW} (differential) = +270V to -60V					
	-40°C, V_{SW} (differential) = -310V to gnd V_{SW} (differential) = +250V to -60V					
On Resistance	I_{SW}(on) = ±10mA, ±40mA, R_{BAT} and T_{BAT} = -2V					
	+25°C	R_{ON}	-	14.5	-	Ω
	+85°C			-	31	
	-40°C			10.5	-	
On Resistance Matching	Per SW1 & SW2 On Resistance test conditions.	ΔR_{ON}	-	0.02	1.0	Ω
ON-State Voltage [1]	Maximum Differential Voltage (V_{max})	ΔV_{ON}	-	-	320	V
	Foldback Voltage Breakpoint 1 (V_1)		60	-	-	
	Foldback Voltage Breakpoint 2 (V_2)		V_1 + 0.5	-	-	
DC current limit 1 (I_{LIM1})	V_{SW} (on) = ±10V, +25°C	I_{SW}	-	300		mA
	V_{SW} (on) = ±10V, +85°C		80			
	V_{SW} (on) = ±10V, -40°C		-		425	
DC current limit 2 ($I_{LIM}2$)		I_{SW}	1	-	-	
Dynamic current limit (t = <0.5 µs)	Break switches on, all other switches off. Apply ±1 kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	2.5	-	A
Logic Input to Switch Output Isolation	+25° C, $\overline{OFF}_x$ = 0, V_{SW} (T_{LINE}, R_{LINE}) = ±320V	I_{SW}	-	-	1	µA
	+85° C, $\overline{OFF}_x$ = 0, V_{SW} (T_{LINE}, R_{LINE}) = ±330V		-	-		
	-40° C, $\overline{OFF}_x$ = 0, V_{SW} (T_{LINE}, R_{LINE}) = ±310V		-	-		
Transient Immunity [2]		dV/dt	1500	2100	-	V/µs

[1] *Choice of secondary protector should ensure this rating is not exceeded.*

[2] *Applied voltage is 100V_{P-P} square wave at 100Hz.*

1.7.2 Ringing Return Switch, SW3

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW3} (differential) = T_{LINE} to $T_{RINGING}$ All-Off state.					
	+25° C, V_{SW} (differential) = -320V to gnd V_{SW} (differential) = +260V to -60V	I_{SW}	-	-	1	µA
	+85° C, V_{SW} (differential) = -330V to gnd V_{SW} (differential) = +270V to -60V			-		
	-40° C, V_{SW} (differential) = -310V to gnd V_{SW} (differential) = +250V to -60V			-		
On Resistance	I_{SW}(on) = ±0mA, ±10mA, +25°C	R_{ON}	-	60	-	Ω
	I_{SW}(on) = ±0mA, ±10mA, +85°C			85	100	
	I_{SW}(on) = ±0mA, ±10mA, -40°C			45	-	
ON-State Voltage [1]	Maximum Differential Voltage (V_{max})	ΔV_{ON}	-	-	320	V
	Foldback Voltage Breakpoint 1 (V_1)		200	-	-	
	Foldback Voltage Breakpoint 2 (V_2)		V_1 + 0.5	-	-	
DC current limit 1 (I_{LIM1})	V_{SW} (on) = ±10V, +25°C	I_{SW}	-	135	-	mA
	V_{SW} (on) = ±10V, +85°C		70	85		
	V_{SW} (on) = ±10V, -40°C		-	210		
DC current limit 2 (I_{LIM2})			1	-	-	
Dynamic current limit (t = <0.5 µs)	Ringing switches on, all other switches off. Apply ±1kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	2.5	-	A
Logic Input to Switch Output Isolation	+25°C, $\overline{OFF}_x$ = 0, V_{SW} ($T_{RINGING}$, T_{LINE}) = ±320V	I_{SW}	-	-	1	µA
	+85°C, $\overline{OFF}_x$ = 0, V_{SW} ($T_{RINGING}$, T_{LINE}) = ±330V			-		
	-40°C, $\overline{OFF}_x$ = 0, V_{SW} ($T_{RINGING}$, T_{LINE}) = ±310V			-		
Transient Immunity [2]	-	dV/dt	1500	2100	-	V/µs

[1] *This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

[2] *Applied voltage is 100V_{P-P} square wave at 100Hz.*

1.7.3 Ringing Switch, SW4

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW4} (differential) = R_{LINE} to $R_{RINGING}$ All-Off state.					
	+25°C V_{SW} (differential) = -255V to +210V V_{SW} (differential) = +255V to -210V	I_{SW}	-	-	1	µA
	+85° C V_{SW} (differential) = -270V to +210V V_{SW} (differential) = +270V to -210V			-		
	-40° C V_{SW} (differential) = -245V to +210V V_{SW} (differential) = +245V to -210V			-		
On Resistance	I_{SW} (on) = ±70mA, ±80mA	R_{ON}	-	10	15	Ω
On Voltage	I_{SW} (on) = ±1mA	V_{ON}	-	-	3	V
On-State Leakage Current	Inputs set for ringing -Measure ringing generator current to ground.	$I_{RINGING}$	-	2	-	mA
Steady-State Current [1]	Inputs set for ringing mode.	I_{SW}	-	-	150	mA
Surge Current [1]	Ringing switches on, all other switches off. Apply ±1kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	-	2	A
Release Current	SW4 transition from on to off.	$I_{RINGING}$	-	300	1000	µA
Logic input to switch output isolation	+25°C, $\overline{OFF}_x$ = 0, V_{SW} ($R_{RINGING}$, R_{LINE}) = ±320V	I_{SW}	-	-	1	µA
	+85°C, $\overline{OFF}_x$ = 0, V_{SW} ($R_{RINGING}$, R_{LINE}) = ±330V			-		
	-40°C, $\overline{OFF}_x$ = 0, V_{SW} ($R_{RINGING}$, R_{LINE}) = ±310V			-		
Transient Immunity [2]	-	dV/dt	1500	2100	-	V/µs

[1] *This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

[2] *Applied voltage is 100V_{P-P} square wave at 100Hz.*

1.7.4 Test Switches, SW5 and SW6

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW1} (differential) = T_{LINE} to T_{BAT} V_{SW2} (differential) = R_{LINE} to R_{BAT} All-Off state.					
	+25°C, V_{SW} (differential) = -320V to gnd V_{SW} (differential) = +260V to -60V	I_{SW}	-	-	1	µA
	+85° C, V_{SW} (differential) = -330V to gnd V_{SW} (differential) = +270V to -60V			-		
	-40° C, V_{SW} (differential) = -310V to gnd V_{SW} (differential) = +250V to -60V			-		
On Resistance	I_{SW}(on) = ±10mA, ±40mA, R_{BAT} and T_{BAT} = -2V					
	+25°C	R_{ON}	-	38	-	Ω
	+85°C			46	70	
	-40°C			28	-	
DC current limit	V_{SW} (on) = ±10V, +25°C	I_{SW}	-	175	-	mA
	V_{SW} (on) = ±10V, +85°C		80	110		
	V_{SW} (on) = ±10V, -40°C		-	210	250	
Dynamic current limit (t = <0.5 µs)	Break switches on, all other switches off. Apply ±1kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	2.5	-	A
Logic Input to Switch Output Isolation	+25°C, $\overline{OFF}_x$ = 0, V_{SW} (T_{LINE}, R_{LINE}) = ±320V	I_{SW}	-	-	1	µA
	+85°C, $\overline{OFF}_x$ = 0, V_{SW} (T_{LINE}, R_{LINE}) = ±330V		-	-		
	-40°C, $\overline{OFF}_x$ = 0, V_{SW} (T_{LINE}, R_{LINE}) = ±310V		-	-		
Transient Immunity [1]	-	dV/dt	1500	2100	-	V/µs

[1] *Applied voltage is 100V_{P-P} square wave at 100Hz.*

1.8 Digital I/O Electrical Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input Characteristics						
Input Voltage, Logic Low (P1-P3, $\overline{OFF}_x$, CFG)	Input voltage falling	V_{IL}	0.8	-	-	V
Input Voltage, Logic Low ($LATCH_x$)			0.6	-	-	
Input voltage, Logic High (P1-P3, $\overline{OFF}_x$)	Input voltage rising	V_{IH}	-	-	2.0	
Input Voltage, Logic High (CFG)			-	-	3.0	
Input Voltage, Logic High ($LATCH_x$)			-	-	1.1	
Input Leakage Current, Logic High ($\overline{OFF}_x$)	V_{DD} = 5.25V, V_{BAT} = -72V, V_{IH} = 5V	I_{IH}	15	32	60	µA
Input Leakage Current, Logic High (P1-P3, $LATCH_x$, CFG)	V_{DD} = 5.25V, V_{BAT} = -72V, V_{IH} = 5V	I_{IH}	-	-	20	µA
Input leakage current, Logic Low (P1-P3, $LATCH_x$, $\overline{OFF}_x$, CFG)	V_{DD} = 5.25V, V_{BAT} = -72V, V_{IL} = 0V	I_{IL}	-	-	20	µA
Input leakage current, T_{SDx} Logic High	V_{DD} = 5.25V, V_{BAT} = -72V, V_{IH} = 2.4V	I_{IH}	10	16	30	µA
Input leakage current, T_{SDx} Logic low	V_{DD} = 5.25V, V_{BAT} = -72V, V_{IL} = 0.4V	I_{IL}	10	16	30	µA
Output Characteristics						
Output voltage, T_{SDx} Logic High	V_{DD} = 5.25V, V_{BAT} = -72V, I_{TSD} = 10µA	V_{TSD_off}	2.4	V_{DD}	-	V
Output voltage, T_{SDx} Logic Low	V_{DD} = 5.25V, V_{BAT} = -72V, I_{TSD} = 1mA	V_{TSD_on}	-	0	0.4	V

1.9 Voltage and Power Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Voltage Requirements						
V_{DD}	-	V_{DD}	4.75	5.0	5.25	V
V_{BAT} [1]	-	V_{BAT}	-19	-48	-72	V
[1] V_{BAT} is used only for internal protection circuitry. If V_{BAT} rises above-10 V, the device will enter the all-off state and will remain in the all-off state until the battery drops below approximately -15V.						
Power Specifications						
Power consumption	V_{DD} = 5V, V_{BAT} = -48V, V_{IH} = 2.4V, V_{IL} = 0.4V, Measure I_{DD} and I_{BAT}					mW
	Idle/Talk State	P	-	-	15 [3]	
	All-Off State [2]		-	-	7.5 [3]	
	Ringing or Test Access State		-	-	20 [3]	
V_{DD} Current	V_{DD} = 5V, V_{BAT} = -48V, V_{IH} = 2.4V, V_{IL} = 0.4V					mA
	Idle/Talk State	I_{DD}	-	1.6 [3]	3.0	
	All-Off State		-	0.75 [3]	1.5	
	Ringing or Test Access State		-	1.8/1.5 [3]	4.0	
V_{BAT} Current	V_{DD} = 5V, V_{BAT} = -48V, V_{IH} = 2.4V, V_{IL} = 0.4V, All States	I_{BAT}	-	4	10	µA
[2] Controlled via $\overline{OFF}_x$ pins.						
[3] Combined power or current of both channels, both channels in the same state. Typical values from simulation.						

1.10 Protection Circuitry Electrical Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Protection Diode Bridge						
Forward Voltage drop, continuous current (50/60 Hz)	Apply ± DC current limit of break switches	V_F	-	2.1	3.0	V
Forward Voltage drop, surge current	Apply ± dynamic current limit of break switches	V_F	-	5	-	
Temperature Shutdown Specifications [1]						
Shutdown activation temperature	Not production tested - limits are guaranteed by design and Quality Control sampling audits.	T_{TSD_on}	110	125	150	°C
Shutdown circuit hysteresis		T_{TSD_off}	10	-	25	°C
Loss of Battery Detector Threshold						
Loss of Battery			-19	-10	-5	V
Resumption of Battery			=19	-15	-5	
[1] Temperature shutdown flag (T_{SDx}) will be high during normal operation and low during temperature shutdown state.						

1.11 Truth Tables

1.11.1 Operating States: CFG=0

State	P3	P2	P1	$\overline{OFF}_x$ [1]	Break Switches	Ringing Switches	Test Switches
Idle/Talk	0	0	0	1	ON	OFF	OFF
Test	0	0	1	1	OFF	OFF	ON
Ringing	0	1	0	1	OFF	ON	OFF
Test/Monitor	0	1	1	1	ON	OFF	ON
Idle/Talk	1	0	0	1	ON	OFF	OFF
Test/Monitor	1	0	1	1	ON	OFF	ON
Ringing	1	1	0	1	OFF	ON	OFF
Test Ringing	1	1	1	1	OFF	ON	ON
All-Off	x	x	x	0[2]	OFF	OFF	OFF

[1] P1, P2, and P3 data input values are directed to a given channel when the respective $LATCH_x$ logic signal is set to "0." $\overline{OFF}_x$ is a per-channel control.

[2] A "0" on $\overline{OFF}_x$ resets the CPC75282, the device will remain in the All-Off state until $\overline{OFF}_x$ is returned to "1" and the next $LATCH_x$ signal is applied.

[3] CFG is fixed at D_{GND}; if CFG switches states when V_{DD} is applied, the change will be recognized by a given channel after a LATCH low transition is applied to that channel.

1.11.2 Operating States: CFG=1

State	P3	P2	P1	$\overline{OFF}_x$ [1]	Break Switches	Ringing Switches	Test Switches
Idle/Talk	0	0	0	1	ON	OFF	OFF
Test	0	0	1	1	OFF	OFF	ON
Ringing	0	1	0	1	OFF	ON	OFF
All-Off	0	1	1	1	OFF	OFF	OFF
Idle/Talk	1	0	0	1	ON	OFF	OFF
Test/Monitor	1	0	1	1	ON	OFF	ON
Ringing	1	1	0	1	OFF	ON	OFF
Test Ringing	1	1	1	1	OFF	ON	ON
All-Off	x	x	x	0[2]	OFF	OFF	OFF

[1] P1, P2, and P3 data input values are directed to a given channel when the respective $LATCH_x$ logic signal is set to "0." $\overline{OFF}_x$ is a per-channel control.

[2] A "0" on $\overline{OFF}_x$ resets the CPC75282, the device will remain in the All-Off state until $\overline{OFF}_x$ is returned to "1" and the next $LATCH_x$ signal is applied.

[3] CFG is fixed at v_{DD}; if CFG switches states when V_{DD} is applied, the change will be recognized by a given channel after a LATCH low transition is applied to that channel.

2. Functional Description

2.1 Introduction

The CPC75282 Dual LCAS device has six operating states:

- **Idle/Talk:** Break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 open.
- **Ringing:** Break switches SW1 and SW2 open, ringing switches SW3 and SW4 closed, and test switches SW5 and SW6 open.
- **Test:** Break switches SW1 and SW2 open, ringing switches SW3 and SW4 open, and loop test switches SW5 and SW6 closed.
- **Test/Monitor:** Break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 closed.
- **Test Ringing:** Break switches SW1 and SW2 open, ringing switches SW3 and SW4 closed, and test switches SW5 and SW6 closed.
- **All-off:** Break switches SW1 and SW2 open, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 open.

See **"Truth Tables" on page 11** for more information.

The CPC75282 offers break-before-make and make-before-break switching from the ringing state to the idle/talk state with simple logic input control. Solid-state switch construction means no impulse noise is generated when switching during ring cadence or ring trip, eliminating the need for external zero-cross switching circuitry. State control is via simple logic input so no additional driver circuitry is required. The linear break switches, SW1 and SW2, have exceptionally low R_{ON} and excellent matching characteristics. The ringing switch, SW4, has a minimum open contact breakdown voltage of 465V at +25°C sufficiently high with proper protection to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ringing generator).

Integrated into the CPC75282 is an over-voltage clamping circuit, active current limiting, and a thermal shutdown mechanism to provide protection for the SLIC during a fault condition. Positive and negative lightning surge currents are reduced by the current limiting circuitry and hazardous potentials are diverted away from the SLIC via the protection diode bridge. Power-cross potentials are also reduced by the current limiting and thermal shutdown circuits.

To protect the CPC75282 from an over-voltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at the tip and ring terminals to a level below the maximum breakdown voltage of the switches. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is highly recommended. With proper selection of the secondary protector, a line card using the CPC75282 will meet all relevant ITU, LSSGR, TIA/EIA and IEC protection requirements.

The CPC75282 operates from a single +5V supply. This gives the device extremely low idle and active power consumption with virtually any range of battery voltage. The battery voltage used by the CPC75282 has a two-fold function. For protection purpose it is used as a fault condition current source during a negative lightning event. Second, it is used as a reference so that in the event of battery voltage loss, the CPC75282 will enter the All-Off state.

2.2 Under Voltage Switch Lock-Out Circuitry

Smart logic in the CPC75282 now provides for switch state control during both power up and power loss transitions. An internal detector is used to evaluate the V_{DD} supply to determine when to de-assert the under-voltage switch lock-out circuitry with a rising V_{DD} and when to assert the under-voltage switch lock-out circuitry with a falling V_{DD}. Any time unsatisfactory low V_{DD} conditions exist, the lock-out circuit overrides user switch control by blocking the information at the external input pins, and conditioning internal switch commands to the All-Off state. Upon restoration of V_{DD}, the switches will remain in the All-Off state until the $LATCH_x$ input is pulled low.

The rising V_{DD} lock-out release threshold is internally set to ensure all internal logic is properly biased and functional before accepting external switch commands from the input to control the switch states. For a falling V_{DD} event, the lock-out threshold is set to assure proper logic and switch behavior up to the moment the switches are forced off and external inputs are suppressed.

2.3 Switch Logic

2.3.1 Start-up

The CPC75282 uses smart logic to monitor the V_{DD} supply. Any time the V_{DD} is below an internally set threshold, the smart logic places the control logic to the all-off state until the $LATCH_X$ input is pulled low. Prior to the assertion of a logic low at the $LATCH_X$ pin, the switch control inputs must be properly conditioned.

2.3.2 Switch Timing

When switching from the ringing state to the idle/talk state, the CPC75282 provides the ability to control the release timing of the ringing switches, SW3 and SW4, relative to the state of the switches, SW1 and SW2, using simple logic inputs. The two available techniques are referred to as make-before-break and break-before-make operation. When the break switch contacts of SW1 and SW2 are closed (made) before the ringing switch contacts of SW3 and SW4 are opened (broken), this is referred to as make-before-break operation. Break-before-make operation occurs when the ringing contacts of SW3 and SW4 are opened (broken) before the switch contacts of SW1 and SW2 are closed (made).

With the CPC75282, make-before-break and break-before-make operations can easily be accomplished by applying the proper sequence of logic-level inputs to the device.

The logic sequences for either mode of operation are given in **"Make-Before-Break Operation Logic Table (Ringing to Talk Transition)" on page 13** and **"Break-Before-Make Ringing to Talk Transition Logic Sequence CPC7592xA/B" on page 14**. Logic states and explanations are shown in **"Truth Tables" on page 11**.

2.3.3 Make-Before-Break Operation

To use make-before-break operation, change the logic inputs from the ringing state directly to the idle/talk state. Application of the idle/talk state opens the ringing return switch, SW3, as the break switches, SW1 and SW2, close. The ringing switch, SW4, remains closed until the next zero-crossing of the ringing current. While in the make-before-break state, ringing potentials in excess of the CPC75282 protection circuitry thresholds will be diverted away from the SLIC.

2.3.4: Make-Before-Break Operation Logic Table (Ringing to Talk Transition)

State	(CFG=0, P3=0) P2	P1	$LATCH_X$	$\overline{OFF}_X$	Timing	Break Switches 1_X & 2_X	Ringing Return Switch 3_X	Ringing Switch 4_X	Test Switches 5_X & 6_X
Ringing	1	0	0	1	-	Off	On	On	Off
Make-before-break	0	0			SW4 waiting for next zero-current crossing to turn off. Maximum time is one-half of the ringing cycle. In this transition state current limited by the DC break switch current limit value will be sourced from the ring node of the SLIC.	On	Off	On	Off
Idle/Talk	0	0			Zero-cross current has occurred	On	Off	Off	Off

Break-before-make operation occurs when the ringing switches open before the break switches, SW1 and SW2, close.

2.3.5: Break-Before-Make Ringing to Talk Transition Logic Sequence CPC7592xA/B

State	CFG=0, P3=0 P2	P1	$LATCH_x$	$\overline{OFF}_x$	Timing	Break Switches 1_x & 2_x	Ringing Return Switch 3_x	Ringing Switch 4_x	Test Switches 5_x & 6_x
Ringing	1	0	0	1	-	Off	On	On	Off
All-Off	1	1		0	Hold this state for at least one-half of the ringing cycle. SW4 waiting for zero current to turn off.	Off	Off	On	Off
All-Off	1	1		0	Zero current has occurred. SW4 has opened	Off	Off	Off	Off
Talk	0	0		1	Break switches close.	On	Off	Off	Off

2.3.6 Break -Before- Make Operation

Break-before-make operation can be achieved using $\overline{OFF}_x$ to disable all of the switches when pulled to a logic low. Although logically disabled, an active (closed) ringing switch, SW4, will remain closed until the next zero crossing current event.

1. Pull $\overline{OFF}_x$ to a logic low to end the ringing state. This opens the ringing return switch, SW3, and prevents any other switches from closing.
2. Keep $\overline{OFF}_x$ low for at least one-half the duration of the ringing cycle period to allow sufficient time for a zero crossing current event to occur and for the circuit to enter the break-before-make state.
3. During the $\overline{OFF}_x$ low period, set the P1, P2, and P3 inputs to the idle/talk state.
4. Release $\overline{OFF}_x$, allowing the internal pull-up to activate the break switches.

2.4 Data Latch

The CPC75282 has integrated transparent data latches. The latch enable operation is controlled by logic input levels at the $LATCH_x$ pin. Data input to the latch is via the input pins P1, P2, and P3 while the outputs of the data latch are internal nodes used for state control. When the latch enable control pin is at a logic 0 the data latch is transparent and the input control signals flow directly through the data latch to the state control circuitry. A change in input will be reflected by a change in the switch states.

Whenever the latch enable control pin is at logic 1, the data latch is active and data is locked. Subsequent changes to the input controls P1, P2, and P3 will not result in a change to the control logic or affect the existing switch states.

The switches will remain in the state they were in when the $LATCH_x$ changes from logic 0 to logic 1, and will not respond to changes in input as long as the $LATCH_x$ is at logic 1. However, neither the T_{SDx} nor the $\overline{OFF}_x$ are affected by the latch function. Since internal thermal shutdown control and external $\overline{OFF}_x$ control is not affected by the state of the latch enable input, T_{SDx} and $\overline{OFF}_x$ will override state control.

2.5 T_{SD} Pin Description

The T_{SDx} pins are bidirectional I/O structures with internal pull-up resistors sourced from V_{DD}. As outputs, these pins indicate the status of the thermal shutdown circuitry for the associated channels. Typically, during normal operation, these pins will be pulled up to V_{DD} , but, under fault conditions that create excess thermal loading, the channels will enter thermal shutdown and a logic low will be output.

As inputs, the T_{SDx} pins are utilized to place the channel into the All-Off state by simply pulling the input low. For applications using low-voltage logic devices (lower than V_{DD}), Clare recommends the use of an open-collector or an open-drain type output to control T_{SDx}. This avoids sinking the T_{SDx} pull up bias current to ground during normal operation when the All-Off state is not required. If T_{SDx} is set to a logic 1 or

tied to V_{CC}, the channel just ignores this input, and still enters the thermal shutdown state at high temperature.

2.6 Ringing Switch Zero-Cross Current Turn Off

After the application of a logic input to turn SW4 off, the ringing switch is designed to delay the change in state until the next zero-crossing. Once on, the switch requires a zero-current cross to turn off, and therefore should not be used to switch a pure DC signal. The switch will remain in the on state no matter the logic input until the next zero crossing. These switching characteristics will reduce and possibly eliminate overall system impulse noise normally associated with ringing switches. See Clare's application note, AN-144, Impulse Noise Benefits of Line Card Access Switches, for more information. The attributes of ringing switch, SW4, may make it possible to eliminate the need for a zero-cross switching scheme. A minimum impedance of 300Ω in series with the ringing generator is recommended.

2.7 Power Supplies

Both a +5V supply and battery voltage are connected to the CPC75282. Switch state control is powered exclusively by the +5V supply. As a result, the CPC75282 exhibits extremely low power consumption during active and idle states. Although battery power is not used for switch control, it is required to supply current during negative overvoltage fault conditions at tip and ring.

2.8 Battery Voltage Monitor

The CPC75282 also uses the V_{BAT} voltage to monitor battery voltage. If system battery voltage is lost, both channels of the CPC75282 immediately enter the All-Off state. It remains in this state until the battery voltage is restored. The device also enters the All-Off state if the battery voltage rises more positive than about –10V with respect to ground and remains in the All-Off state until the battery voltage drops below approximately –15V with respect to ground. This battery monitor feature draws a small current from the battery (less than 1μA typical) and will add slightly to the device's overall power dissipation.

2.9 Protection

2.9.1 Diode Bridge

Both channels of the CPC75282 use a combination of current limited break switches, a diode bridge, and a thermal shutdown mechanism to protect the SLIC device or other associated circuitry from damage during line transient events, such as lightning. During a positive transient condition, the fault current is conducted through the diode bridge to ground via F_{GND}. Voltage is clamped to a diode drop above ground. Negative lightning is directed to battery via steering diodes in the diode bridge. For power induction or power-cross fault conditions, the positive cycle of the transient is clamped to a diode drop above ground and the fault current directed to ground. The negative cycle of the transient is steered to battery. Fault currents are limited by the current-limit circuit.

2.9.2 Current Limiting function

If a lightning strike transient occurs when the device is in the Idle/Talk state, the current is passed along the line to the integrated protection circuitry, and restricted by the dynamic current limit response of the active switches. During the Idle/Talk state, when a 1000V 10x1000μ□s lightning pulse (GR-1089-CORE lightning) is applied to the line though a properly clamped external protector, the current seen at T_{LINE} and R_{LINE} will be a pulse with a typical magnitude of 2.5A and a duration less than 0.5μs.

If a power-cross fault occurs with the device in the Idle/Talk state, the current is passed though break switches, SW1 and SW2, on to the integrated protection circuit, but is limited by the DC current limit response of the two break switches. The DC current limit is dependent on the switch differential voltage, as shown in **"Figure 2: Switches 1-3" on page 17**. Note that the current limit circuitry has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to a power cross fault condition, the measured current at T_{LINE} and R_{LINE} will decrease as the device temperature increases. If the device temperature rises sufficiently, the temperature shutdown mechanism will activate and the device will enter the All-Off state.

2.10 Thermal Shutdown

The thermal shutdown mechanism activates when the device die temperature reaches a minimum of 110°C, placing the device in the All-Off state regardless of logic input. During thermal shutdown events the T_{SDx} pin will output a logic low with a nominal 0V level. A logic high is output from the T_{SDx} pin during normal operation with a typical output level equal to V_{DD}.

If presented with a short duration transient, such as a lightning event, the thermal shutdown feature will typically not activate. But in an extended power-cross event, the device temperature will rise and the thermal shutdown mechanism will activate forcing the switches to the All-Off state. At this point the current measured into T_{LINE} or R_{LINE} will drop to zero. Once the device enters thermal shutdown, it will remain in the All-Off state until the temperature of the device drops below the de-activation level of the thermal shutdown circuit. This permits the device to autonomously return to normal operation. If the transient has not passed, current will again flow up to the value allowed by the dynamic DC current limiting of the switches and heating will resume, reactivating the thermal shutdown mechanism. This cycle of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector will activate, shunting the fault current to ground.

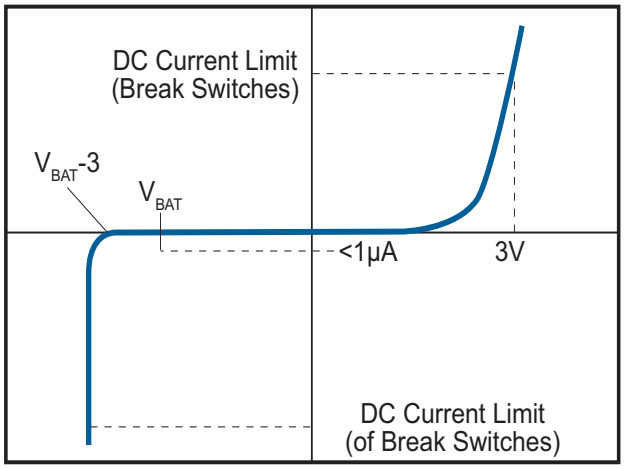
2.11 External Protection Elements

The CPC75282 requires only over-voltage secondary protection on the loop side of the device. The integrated protection feature described above negates the need for additional external protection on the SLIC side. The secondary protector must limit voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC75282. A foldback or crowbar type protector is recommended to minimize stresses on the CPC75282.

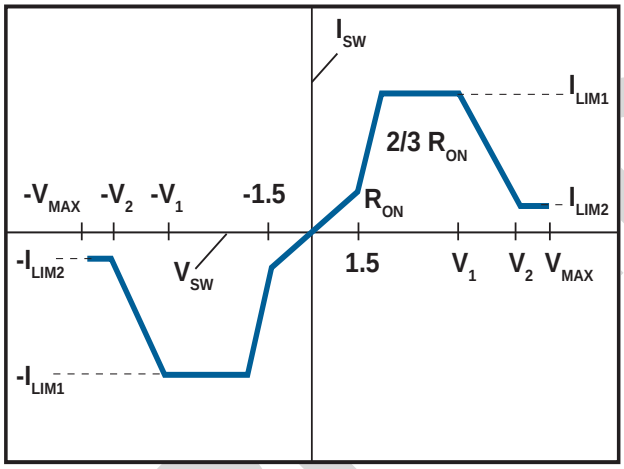
Consult Clare's application note, AN-100, "Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces," for equations related to the specifications of external secondary protectors, fused resistors, and PTCs.

3. Typical Performance Characteristics

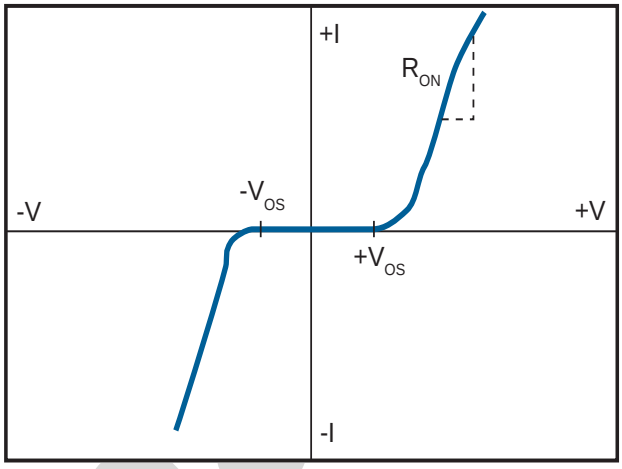
3.1 Figure 1: Protection Circuit



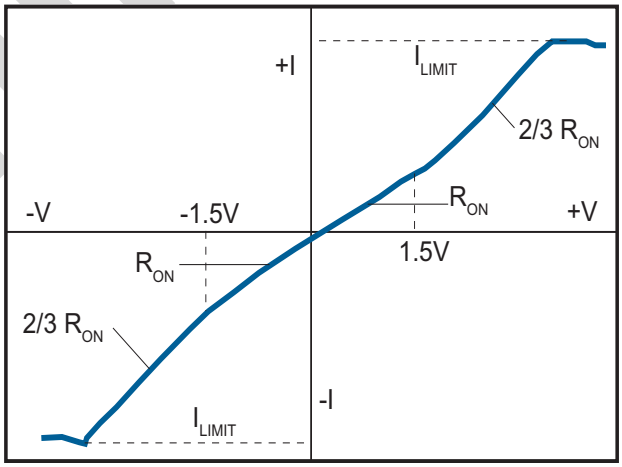
3.2 Figure 2: Switches 1-3



3.3 Figure 3: Switch 4



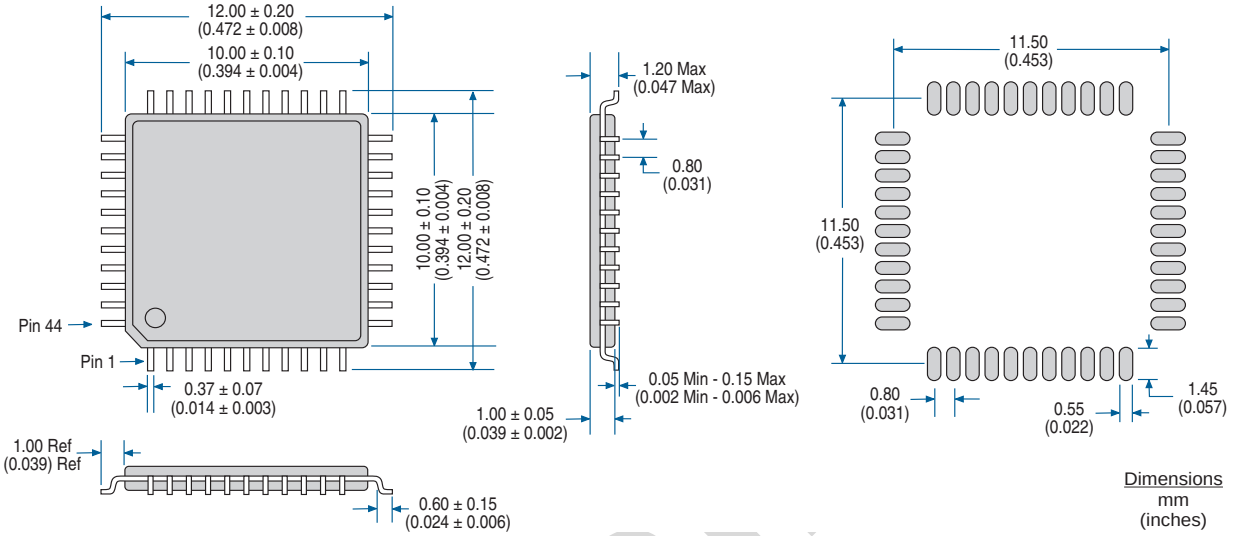
3.4 Figure 4: Switches 5-6



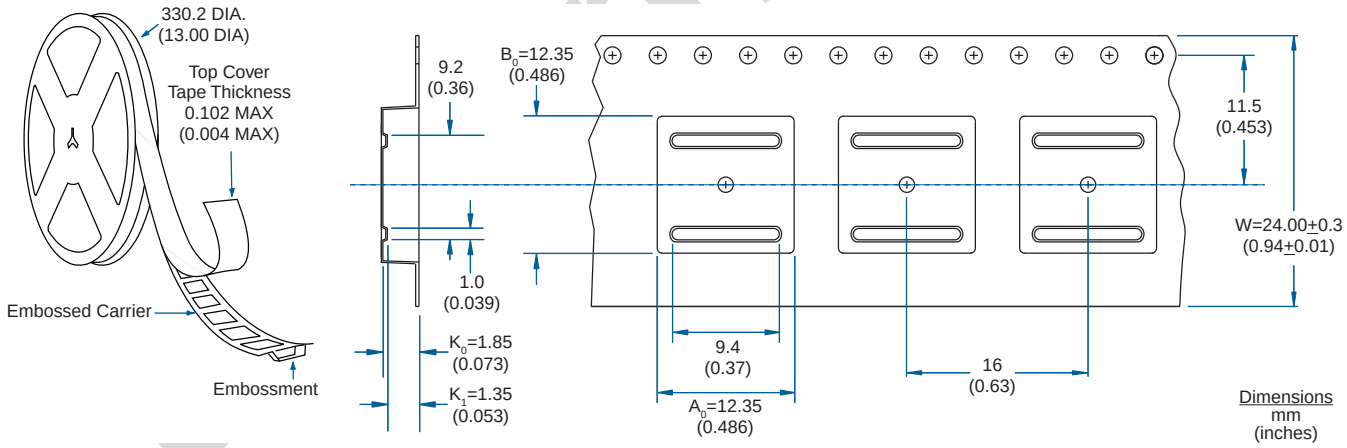
4. Manufacturing Information

4.1 Mechanical Dimensions

4.1.1 Package Dimensions



4.1.2 Tape & Reel Specification



4.2 Soldering

For proper assembly, this component must be processed in accordance with the current revision of IPC/JEDEC standard J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

4.3 Washing

Clare does not recommend ultrasonic cleaning of this part.

For additional information please visit www.clare.com

Specifications: DS-CPC75282 - R00D

8/4/09