VN5R003H-E

3 mΩ reverse battery protection switch

Datasheet – production data

Features

Max supply voltage	V_{CC}	-16 to 41 V
Operating voltage range	V_{CC}	-16 to 28 V
On-state resistance	R_{ON}	3 mΩ

- General
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
- Protections
  - Automatic switch off in case of negative input voltage
  - Electrostatic discharge protection

Application

- Reverse battery protection of an electronic control unit

HPak

Description

The VN5R003H-E is a device made using STMicroelectronics® VIPower® technology. It is intended for providing reverse battery protection to an electronic module.

This device has two power pins (Drain and Source) and a control pin $\overline{IN}$. If the $\overline{IN}$ voltage versus Drain is negative the device is turned on.

A negative voltage of Drain pin versus $\overline{IN}$ automatically turns off the device. When $\overline{IN}$ is left open, device is in OFF-state and behaves like a power diode between Source and Drain pins.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
HPAK	VN5R003H-E	VN5R003HTR-E

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

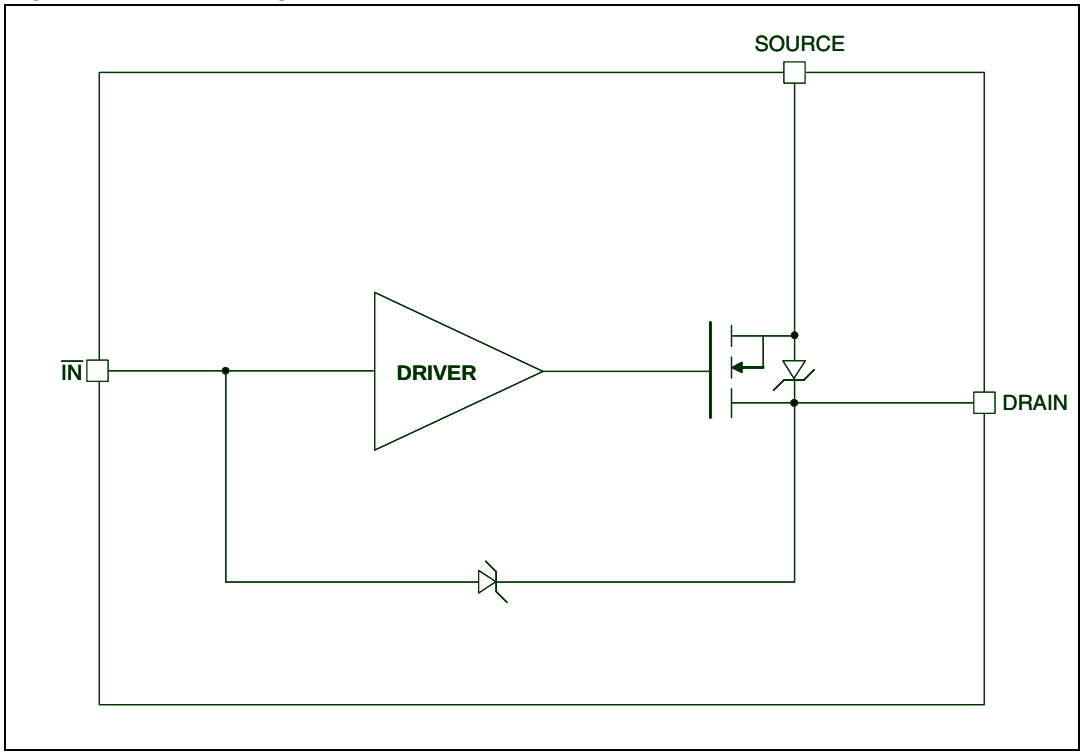
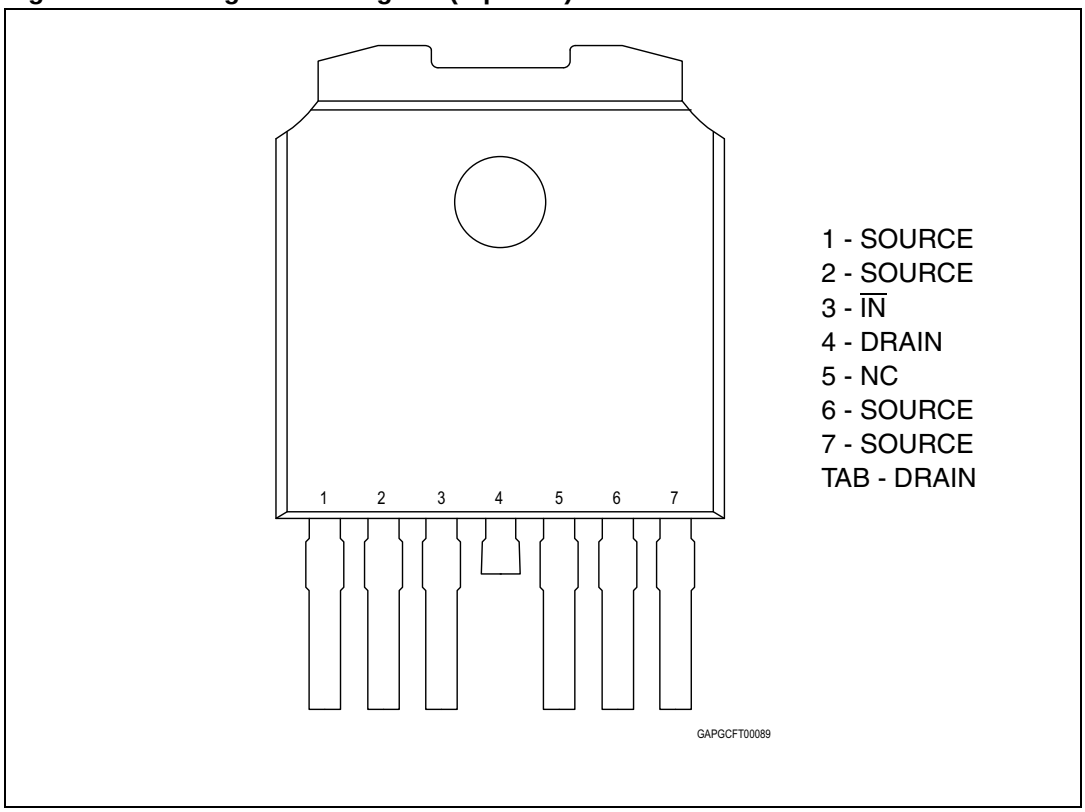


Table 2. Pin function

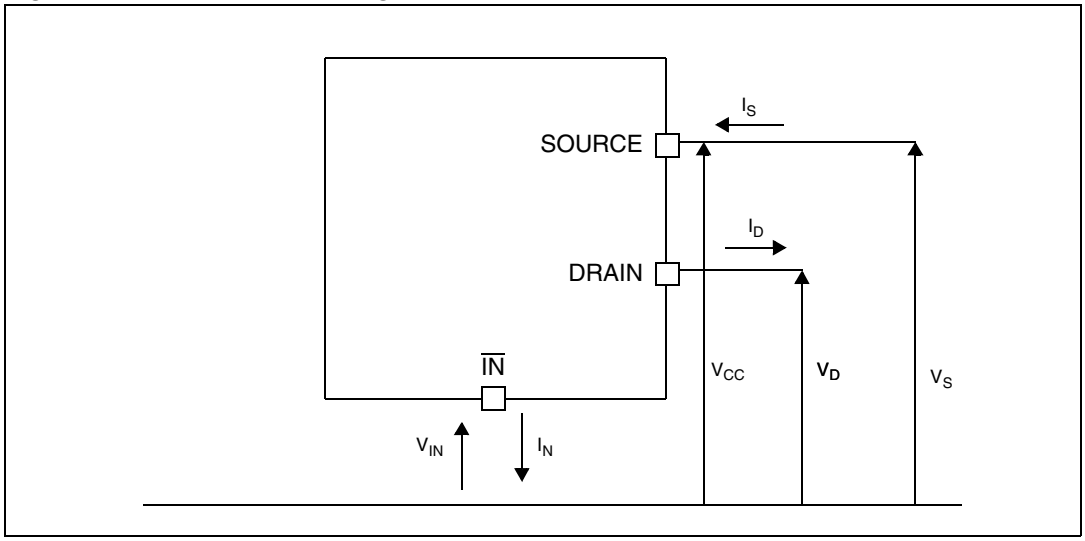
Name	Function
Drain	Power MOS drain
Source	Power MOS source
$\overline{IN}$	Control pin

Figure 2. Configuration diagram (top view)



2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Source power terminal DC voltage (reverse battery mode)	-16 to 41	V
I_S, I_D	Source or Drain current	60	A
$-I_S$, $-I_D$	Reverse currents	60	A
E_{MAX}	Inductive clamp energy L = 2 mH, V_D = 0 V, $\overline{IN}$ open, I_S < 0, T_{jstart} = 25°C	0.9	J
V_{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF) - All terminals	5000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	1000	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max.	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (mounted on FR4 using 6 cm^2 copper pad)	42	°C/W

2.3 Electrical characteristics

Table 5. Power section for reverse battery mode(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Operating supply voltage	—	-16	13	28	V
V_{CLPDS}	Drain-Source clamp voltage	V_D = 0 V, $\overline{IN}$ open, I_S = -5 A	17		23	V
V_{CLPDIN}	Drain input clamp voltage	V_{IN} = 0 V, I_D = 20 mA	41		52	V
V_F	Source drain voltage	$\overline{IN}$ = open, I_S = 10 A; T_j = 25°C		0.85		V
R_{ON}	On state resistance between SOURCE and Drain terminals	I_S = 10 A; T_j = 25°C; 8 V < V_{CC} < 28 V		3		mΩ
		I_S = 10 A; T_j = 150°C; 8 V < V_{CC} < 28 V			5.5	
$I_{\overline{IN}}$	Input current	V_S = 13 V , $V_{\overline{IN}}$ = 0 V		2	3	mA
$I_{\overline{IN}(REV)}$	Reverse input current	V_S = -16 V, $V_{\overline{IN}}$ = 0 V	-2		0	mA
I_{OUT_rev}	Output reverse current	V_S = -16 V, V_D = 0 V, $\overline{IN}$ open	-1.5		-0.5	mA

1. Operating conditions: 40°C < T_j < 150°C

Table 6. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1(2)	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse	—		100 ms, 0.01 Ω
5b(3)	+65 V	+87 V	1 pulse	—		400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. The device does not turn Off once the ISO pulse is applied.
3. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 7. Electrical transient requirements (part 2)

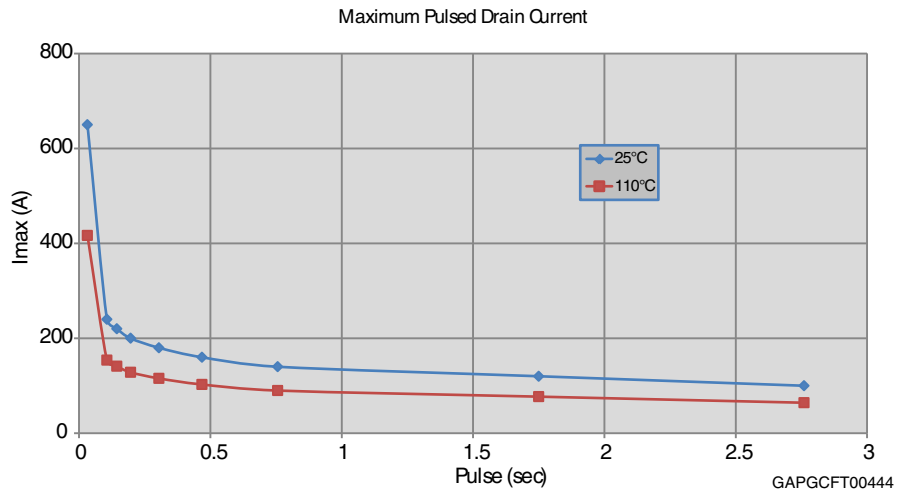
ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)	C	C

1. Transient pulses have been applied with the INPUT pin grounded with R1>5Ω.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 8. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 4. Maximum pulsed drain current (V_{BATT} = 13 V)



Note:
PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 mm,
Copper areas: minimum pad lay-out and 2 cm^2

3 Application information

Figure 5 shows the solution for systems supplied directly from the battery. If the system goes into *Stand-by* mode, the transistor T1 is switched off by the microcontroller with zero quiescent current. System is still supplied through the PowerMOS body diode.

Figure 5. Battery supplied systems

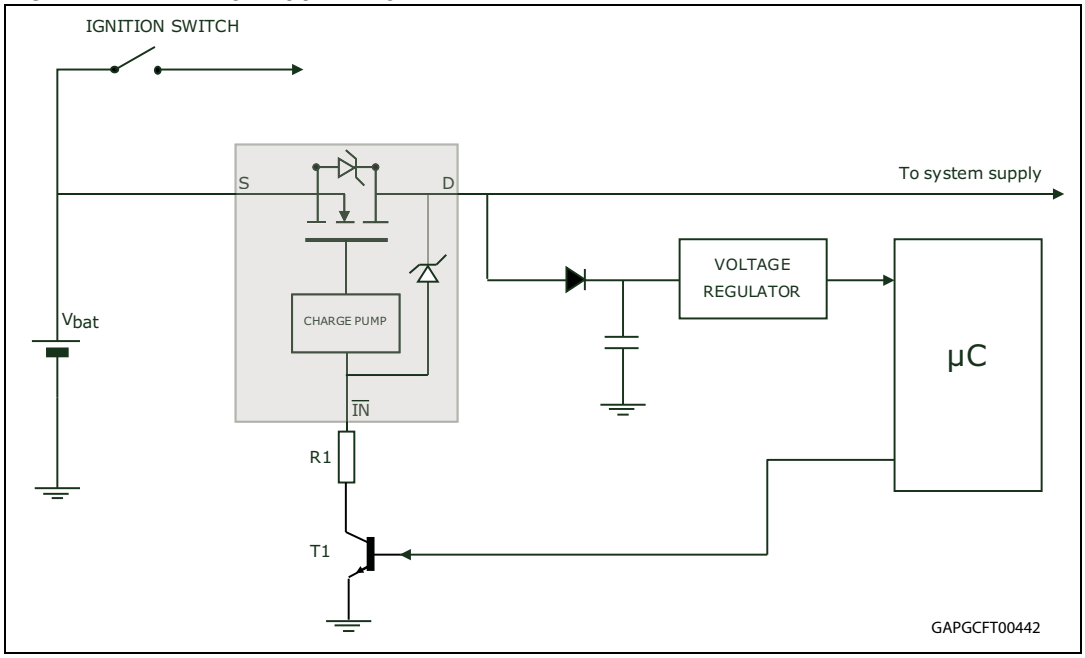
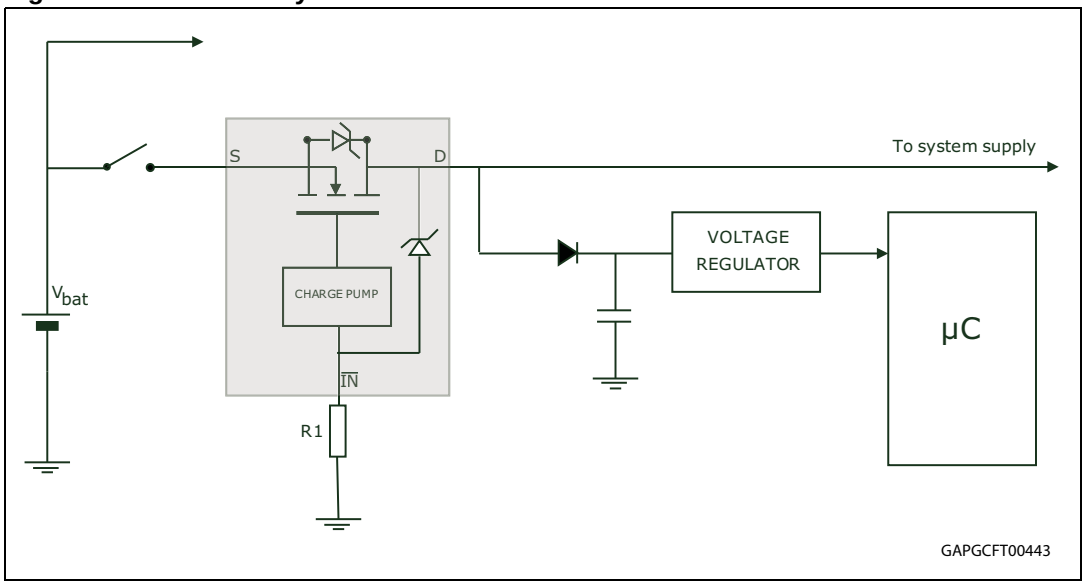


Figure 6 refers to a solution for systems supplied after the ignition switch. Low quiescent currents are not strictly required, so resistor R1 can be directly connected to ground.

Figure 6. Switched systems



4 Package and PC board thermal data

4.1 HPAK thermal data

Figure 7. PC board

Note:
Layout condition of Rth and Zth measurements (Board finish thickness 1.6 mm +/- 10%, board double layer, board dimension 78 mm x 86 mm, board material FR4, Cu thickness = 70 µm (front and back side), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 25 µm, footprint dimension 6.4 mm x 7 mm).

Figure 8. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

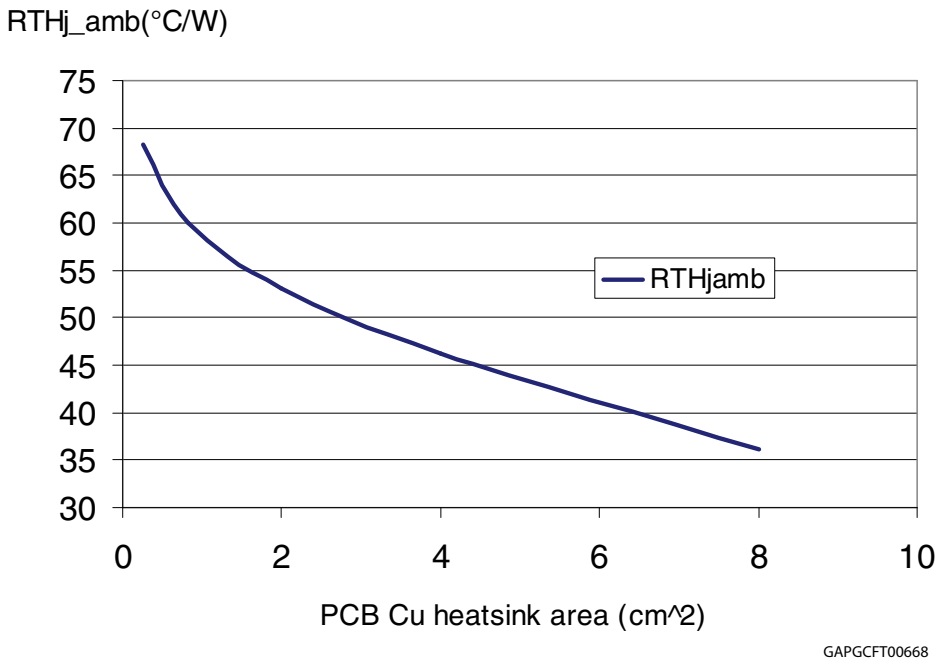


Figure 9. HPAK thermal impedance junction ambient single pulse

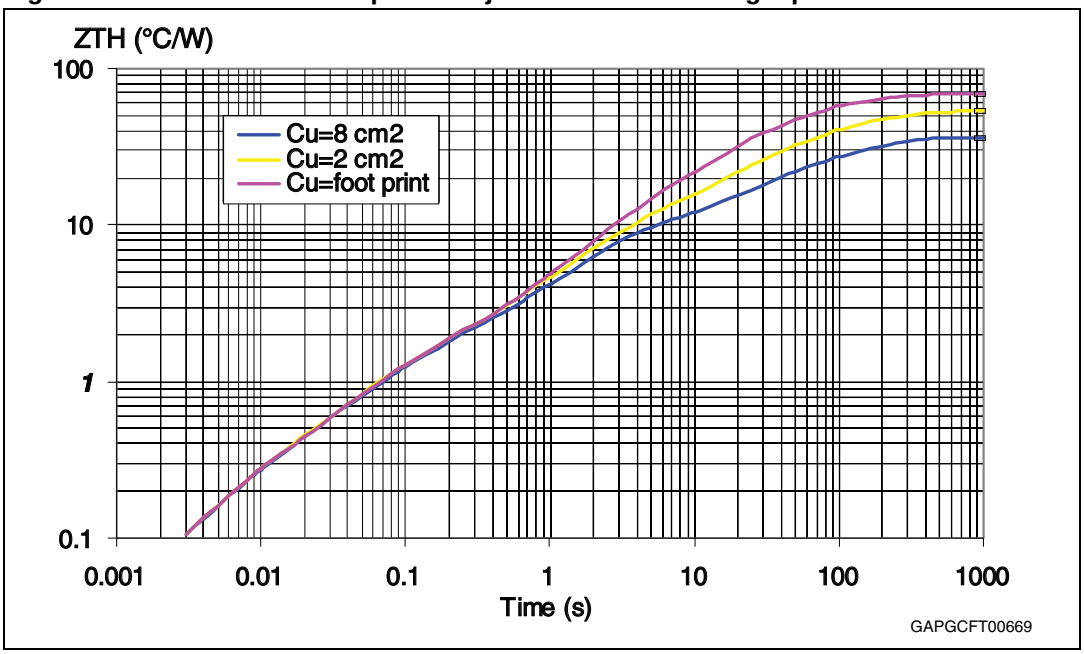
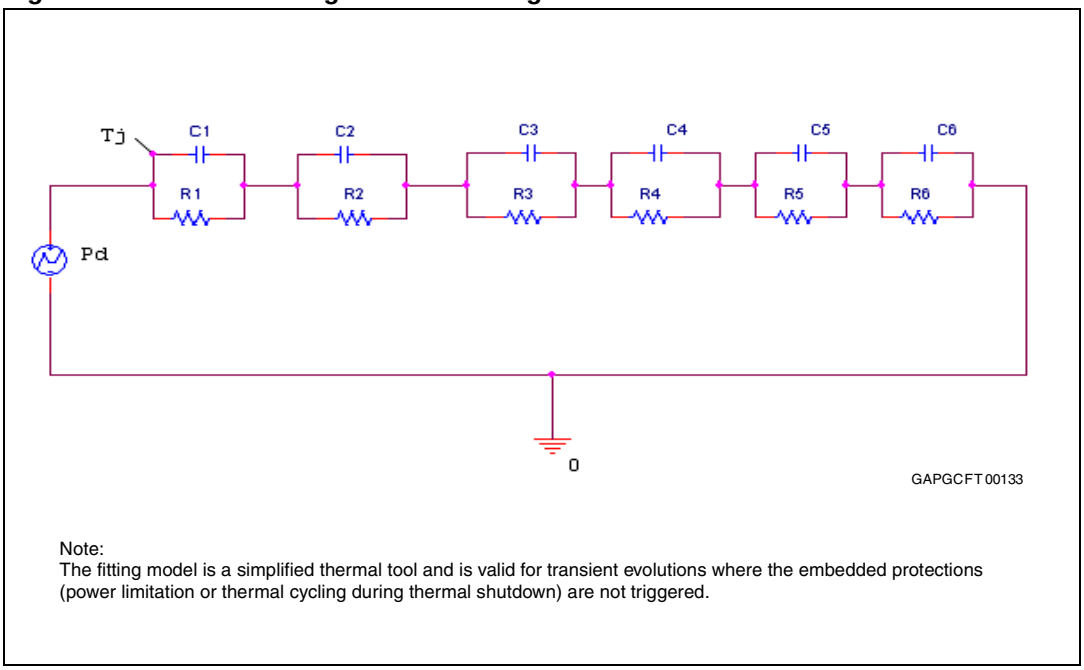


Figure 10. Thermal fitting model of a single-channel HSD in HPAK



Note:
The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Table 9. Thermal parameter

Area/island (cm^2)	Footprint	4	8
R1 (°C/W)	0.01		
R2 (°C/W)	0.15		
R3 (°C/W)	1		
R4 (°C/W)	8		
R5 (°C/W)	28	21	12
R6 (°C/W)	31	24	16
C1 (W.s/°C)	0.005		
C2 (W.s/°C)	0.05		
C3 (W.s/°C)	0.08		
C4 (W.s/°C)	0.4		
C5 (W.s/°C)	0.8	1.4	3
C6 (W.s/°C)	3	6	9

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 HPAK mechanical data

Figure 11. HPAK package dimension

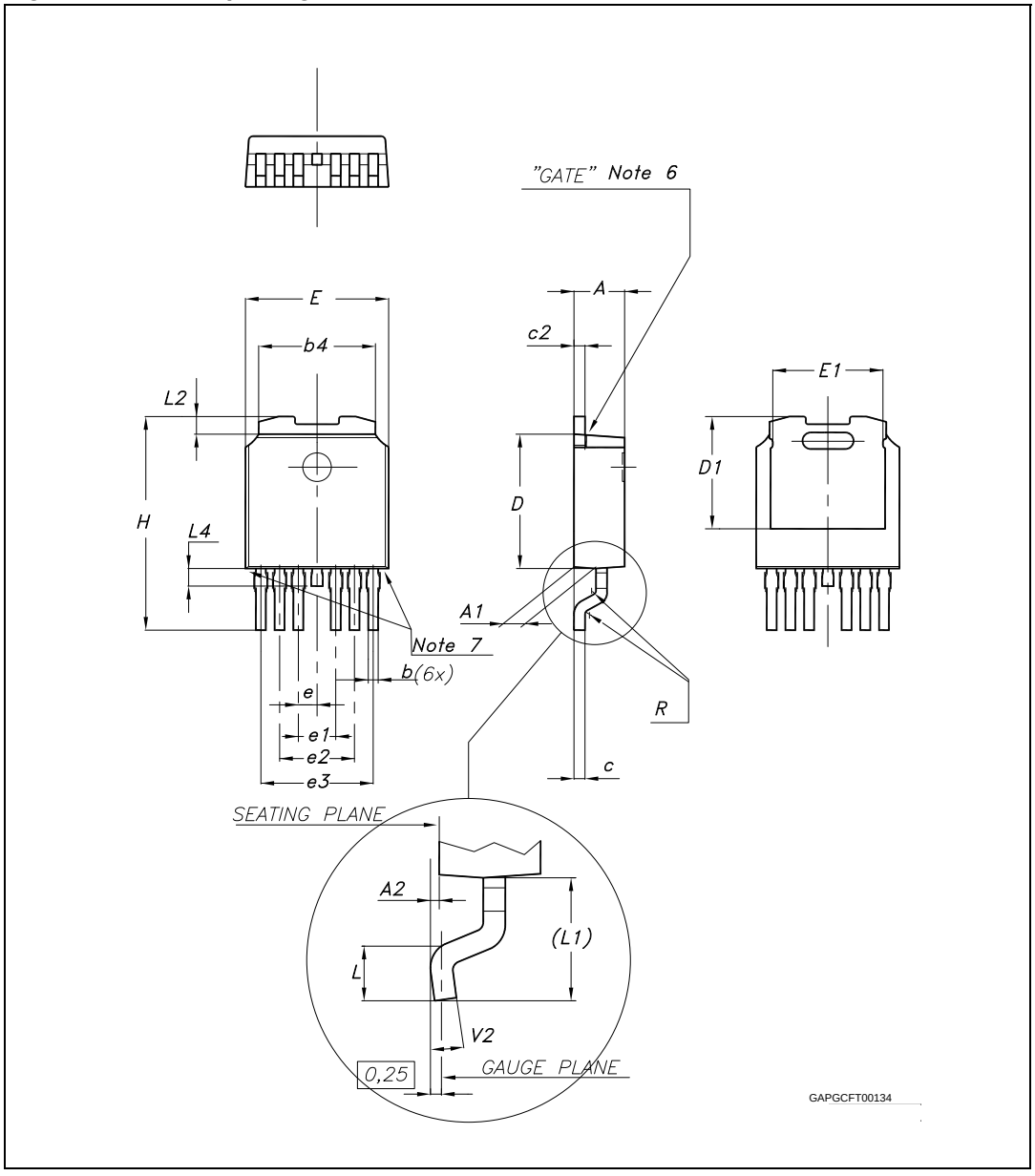
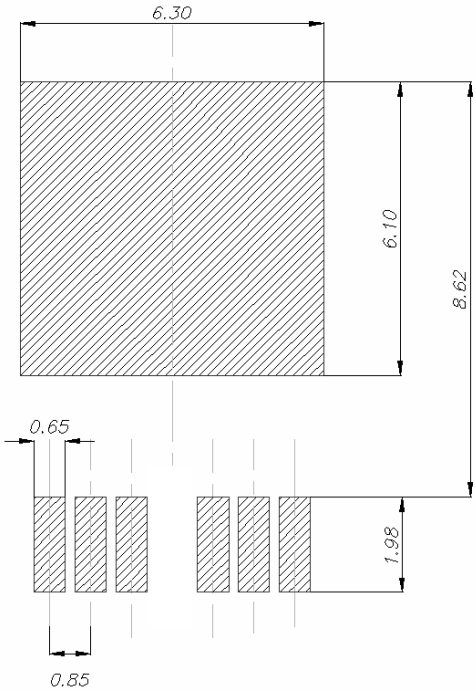


Table 10. HPAK mechanical data

Ref. dim	Data book mm		
	Typ	Min.	Max.
A	—	2.20	2.40
A1	—	0.90	1.10
A2	—	0.03	0.23
b	—	0.45	0.60
b4	—	5.20	5.40
c	—	0.45	0.60
c2	—	0.48	0.60
D	—	6.00	6.20
D1	5.10	—	—
E	—	6.40	6.60
E1	5.20	—	—
e	0.85	—	—
e1	—	1.60	1.80
e2	—	3.30	3.50
e3	—	5.00	5.20
H	—	9.35	10.10
L	—	1	—
(L1)	2.80	—	—
L2	0.80	—	—
L4	—	0.60	1.00
R	0.20	—	—
V2	—	0°	8°

5.3 HPAK suggested land pattern

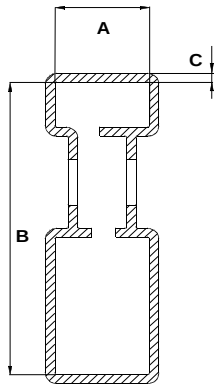
Figure 12. HPAK suggested pad layout[a]



All dimensions are in mm.

5.4 Packing information

Figure 13. HPAK tube shipment (no suffix)

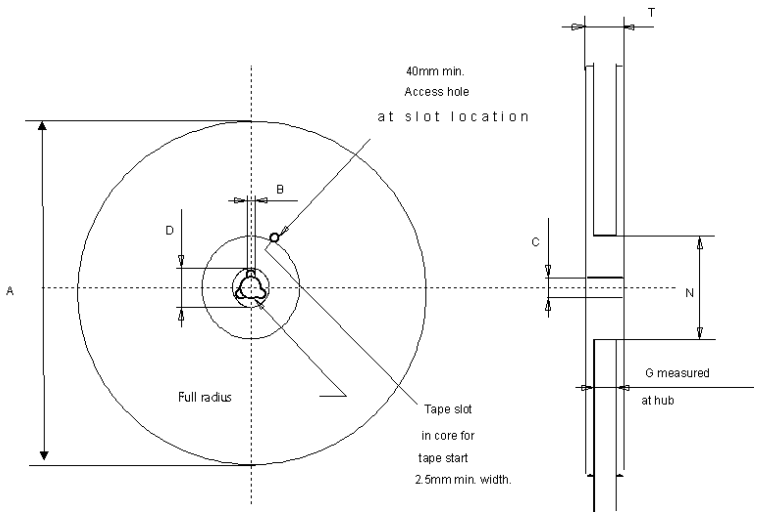


Base q.ty	75
Bulk q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

a. The land pattern proposed is not intended to over-rule User's PCB design, manufacturing and soldering process rules

Figure 14. HPAK tape and reel (suffix “TR”)



REEL DIMENSIONS

All dimensions are in mm.

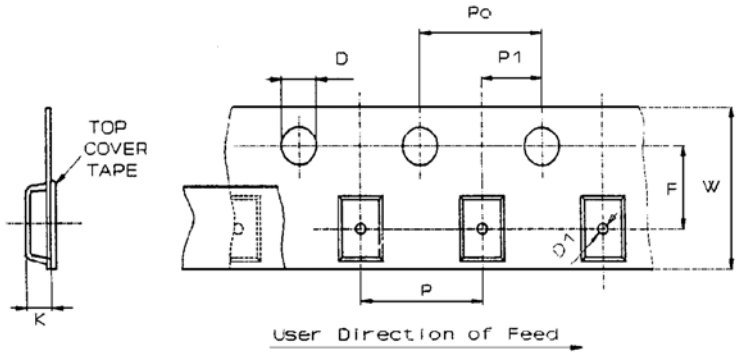
Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

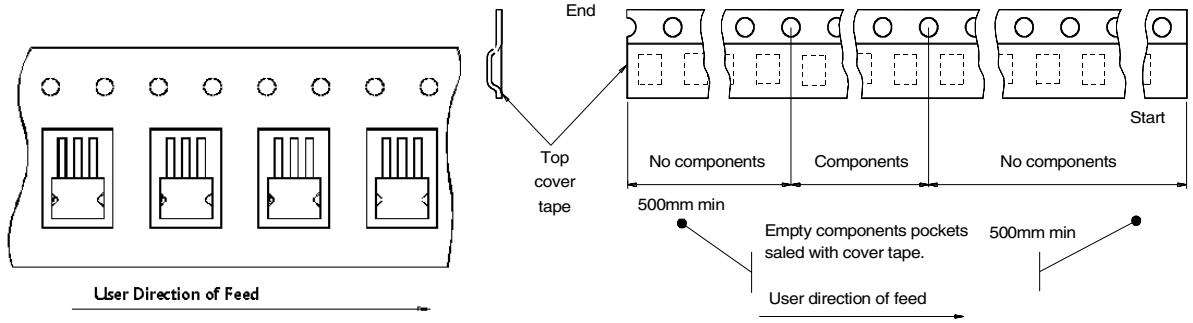
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	16
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	8
Hole diameter	**D (± 0.1/-0)**	1.5
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.05)**	7.5
Compartment depth	**K (max)**	2.75
Hole spacing	**P1 (± 0.1)**	2

All dimensions are in mm.





6 Revision history

Table 11. Document revision history

Date	Revision	Changes
23-Jun-2010	1	Initial release.
06-Jul-2010	2	Updated *Table 4: Thermal data*.
06-Oct-2010	3	Added *Figure 4: Maximum pulsed drain current (V_{BATT} = 13 V)*
18-Nov-2010	4	Changed document status from target specification to datasheet. *Table 3: Absolute maximum ratings*: – Removed V_D row *Table 5: Power section for reverse battery mode* – $I_{\overline{IN}}$: added maximum value *Table 6: Electrical transient requirements (part 1)* – Added *Note 2* Updated *Figure 5: Battery supplied systems* and *Figure 6: Switched systems*
17-Apr-2012	5	Updated *Figure 4: Maximum pulsed drain current (V_{BATT} = 13 V)*

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