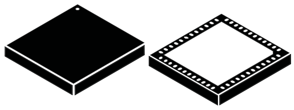
STA381BW

Sound Terminal®
2.1-channel high-efficiency digital audio system

Datasheet — production data

Features

- Wide-range supply voltage
  - 4.5 V to 26 V (operating range)
  - 30 V (absolute maximum rating)
- I^{2}C control with selectable device address
- Embedded full IC protection
  - Manufacturing short-circuit protection (out vs. gnd, out vs. vcc, out vs. out)
  - Thermal protection
  - Overcurrent protection
  - Undervoltage protection
- 1 Vrms stereo analog input
- I^{2}S interface, sampling rate 32 kHz ~ 192 kHz, with internal sampling frequency converter for fixed processing frequency
- Three output power stage configurations
  - 2.0 mode, L/R full bridges
  - 2.1 mode, L/R two half-bridges, subwoofer full bridge
  - 2.1 mode, L/R full bridges, PWM output for external subwoofer amplifier
- Driving load capabilities
  - 2 x 20 W into 8 Ω ternary modulation
  - 2 x 9 W into 4 Ω + 1 x 20 W into 8 Ω
- FFX™ 100 dB dynamic range
- Fixed output PWM frequency at any input sampling frequency
- Embedded RMS meter for measuring real-time loudness
- Two analog outputs
  - Selectable headphone / line out driver with adjustable gain via external resistors
  - New F3X™ analog output
- New fully programmable noise-gating function



VQFN48 (7 x 7 mm)

- Headphone
  - Embedded negative charge pump
  - Full capless output configuration
  - Driving load capabilities: 40 mW into 32 Ω
- Line out
  - 2 Vrms line output capability
- Up to 12 user-programmable biquads with noise-shaping technology
- Direct access to coefficients through I^{2}C shadowing mechanism
- Fixed (88.2 kHz / 96 kHz) internal processing sampling rate
- Two independent DRCs configurable as a dual-band anticlipper or independent limiters/compressors (B^{2}DRC)
- Digital gain/att +48 dB to -80 dB with 0.125 dB/step resolution
- Independent (fade-in, fade-out) soft volume update with programmable rate 48 ~ 1.5 dB/ms
- Bass/treble tones control
- Audio presets: 15 crossover filters, 5 anticlipping modes, nighttime listening mode
- STSpeakerSafe™ protection circuitry
  - Pre- and post-processing DC blocking filters
  - Checksum engine for filter coefficients
  - PWM fault self-diagnosis
- STCompressor™ dual-band DRC

Table 1. Device summary

Order code	Package	Packing
STA381BW	VQFN48	Tray
STA381BWTR	VQFN48	Tape and Reel

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1 Description

The STA381BW is an integrated solution embedding digital audio processing, digital amplification, FFX™ power output stage, headphone and 2 Vrms line outputs. It is part of the Sound Terminal® family and provides full digital audio streaming from the source to the speaker, offering cost effectiveness, low power dissipation and sound enrichment.

The STA381BW input section consists of a flexible digital input serial audio interface, feeding the digital processing unit, and an analog 1 Vrms input for a seamless connection with pure analog sources. The serial audio data input interface supports many formats, including the popular IIS format.

The STA381BW is based on an FFX™ (Fully Flexible Amplification) processor, proprietary technology from STMicroelectronics. FFX™ is the evolution of the ST ternary technology: the advanced processor is available for ternary, binary, binary differential and phase shift PWM modulation. The STA381BW embeds the ternary, binary and binary differential implementations, a subset of the full capability of the FFX™ processor.

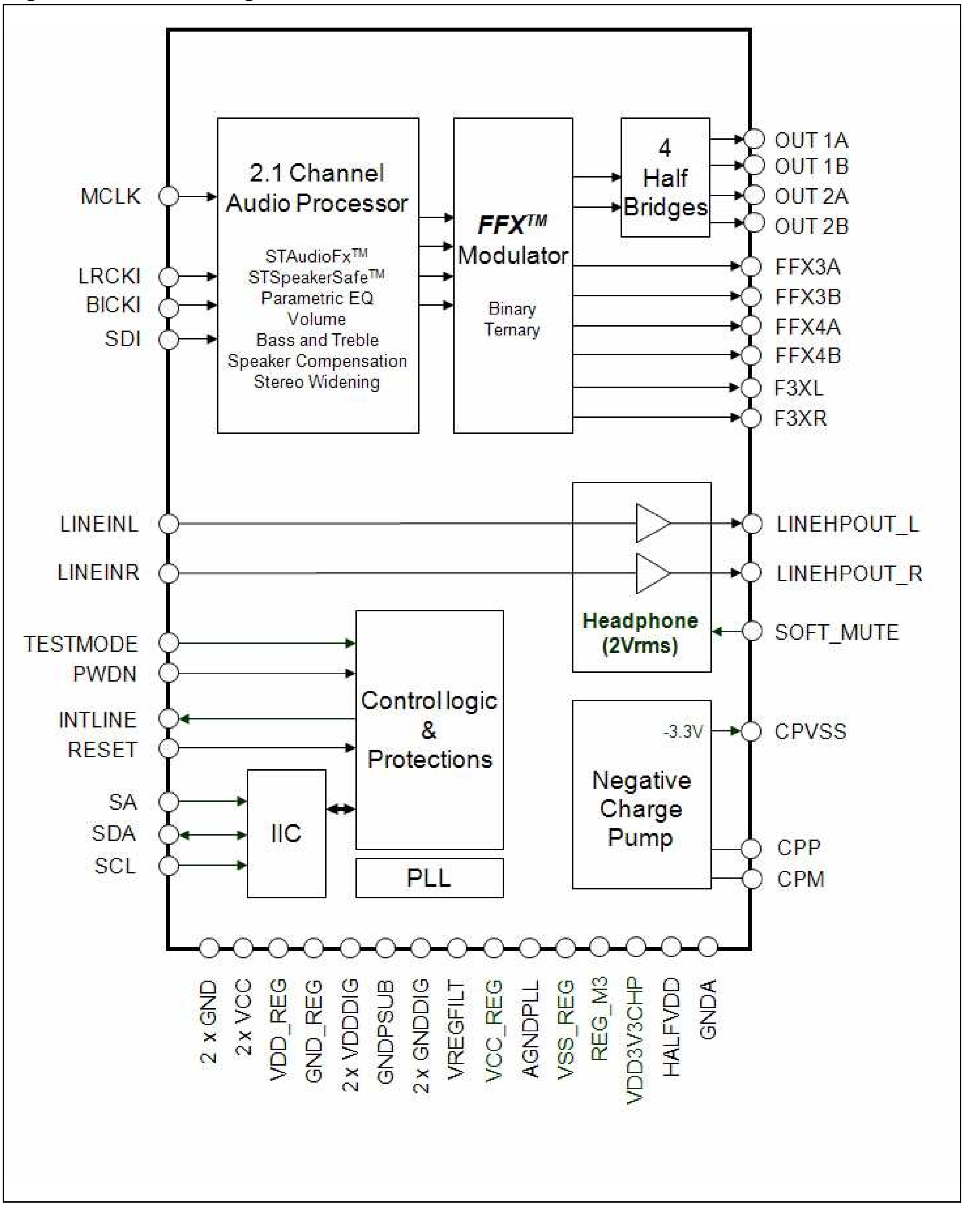
The STA381BW power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes. A 2.1-channel setup can be implemented with two half-bridges (L/R) together with a single full-bridge (subwoofer). Alternatively, the 2.0-channel setup can be done with two full-bridges. When using this configuration, an external amplifier for the SW channel can also be driven through the PWM output. The STA381BW is able to deliver 2 x 20 W (ternary) into an 8 Ω load at 18 V or 2 x 9 W (binary) into a 4 Ω load, plus 1 x 20 W (ternary) into an 8 Ω load at 18 V.

The STA381BW also provides a capless headphone out (with embedded negative charge pump), able to deliver up to 40 mW into a 32 Ω load or, alternatively, can be configured as a 2 Vrms line output.

The STA381BW digital processing unit includes up to 12 programmable biquads (EQs), allowing perfect sound equalization and offering advanced noise-shaping techniques. Moreover, the coefficient range ensures a great variety of filter shapes (low/high-pass, low/high shelf, peak, notch, band-pass). The equalization engine is fully compatible with the ST speaker compensation technology embedded into the APWorkbench suite. A state-of-the-art multi-band DRC, STCompressor™ equalizes the system to provide active speaker protection with full audio quality preservation against sudden sound peaks. Moreover, STSpeakerSafe™ technology offers reliable speaker protection under any condition. The master clock can be from stable BICKI (64xfs, 50% duty cycle) or external XTI.

1.1 Block diagram

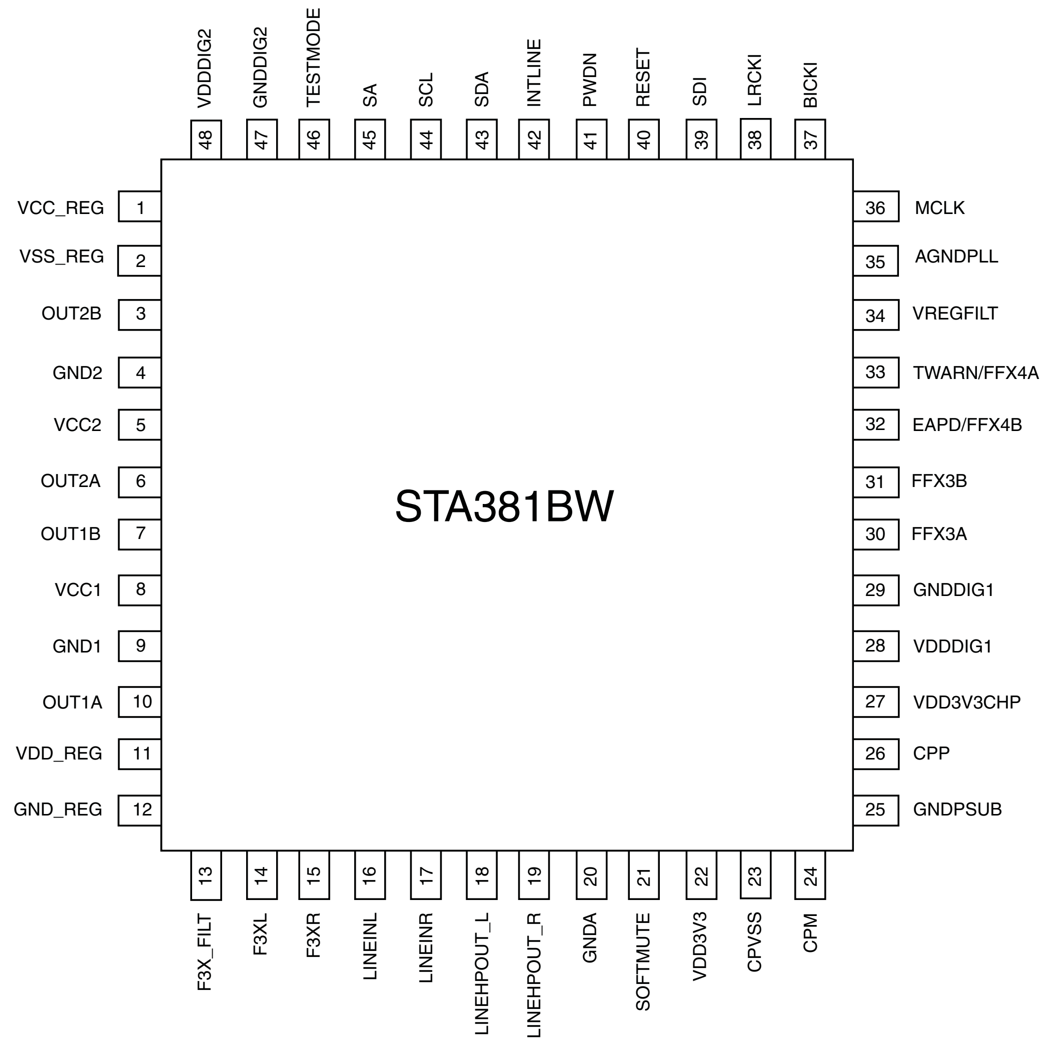
Figure 1. Block diagram



2 Pin connections

2.1 Connection diagram

Figure 2. Pin connections VQFN48 (top view)



2.2 Pin description

Table 2. Pin list

VQFN 48-pin	Name	Type	Description
1	VCC_REG	POWER	VCC reg
2	VSS_REG	POWER	Vss reg, VCC_REG-3.3 V
3	OUT2B	OUTPUT	Half-bridge 2B output
4	GND2	POWER	Half-bridge 2A and 2B ground
5	VCC2	POWER	Half-bridge 2A and 2B supply
6	OUT2A	OUTPUT	Half-bridge 2A output
7	OUT1B	OUTPUT	Half-bridge 1B output
8	VCC1	POWER	Half-bridge 1A and 1B supply
9	GND1	POWER	Half-bridge 1A and 1B ground
10	OUT1A	OUTPUT	Half-bridge 1A output
11	VDD_REG	POWER	VDD reg 3.3 V
12	GND_REG	POWER	DC reg ground
13	F3X_FILT	POWER	F3X reference voltage
14	F3XL	OUTPUT	F3X analog out left channel
15	F3XR	OUTPUT	F3X analog out right channel
16	LINEINL	INPUT	Line in left channel
17	LINEINR	INPUT	Line in right channel
18	LINEHPOUT_L	OUTPUT	Headphone/line driver left channel
19	LINEHPOUT_R	OUTPUT	Headphone/line driver right channel
20	GNDA	POWER	Headphone/line driver power ground
21	SOFTMUTE	INPUT	Soft mute
22	VDD3V3	POWER	+3 V LDO power supply
23	CPVSS	POWER	-3.3 V charge pump pin
24	CPM	FILTER	CHP Cfly negative
25	GNDPSUB	POWER	Charge pump ground
26	CPP	FILTER	CHP Cfly positive
27	VDD3V3CHP	POWER	Charge pump power supply
28	VDDDIG1	POWER	I/O ring power supply
29	GNDDIG1	POWER	Digital core ground
30	FFX3A	OUTPUT	Digital PWM line out
31	FFX3B	OUTPUT	Digital PWM line out

Table 2. Pin list (continued)

VQFN 48-pin	Name	Type	Description
32	EAPD/FFX4B	OUTPUT	Digital PWM line out
33	TWARN/FFX4A	OUTPUT	Digital PWM line out
34	VREGFILT	POWER	Digital VDD from core
35	AGNDPLL	POWER	PLL analog ground
36	MCLK	INPUT	PLL input clock
37	BICKI	INPUT	IIS serial clock
38	LRCKI	INPUT	IIS left/right clock
39	SDI	INPUT	IIS serial data input
40	RESET	INPUT	Reset
41	PWDN	INPUT	Device power-down 0 = power-down 1 = normal operation
42	INTLINE	OUTPUT	Fault interrupt
43	SDA	I/O	IIC serial data
44	SCL	INPUT	IIC serial clock
45	SA	INPUT	IIC select address (pull-down)
46	TEST_MODE	INPUT	This pin must be connected to ground (pull-down)
47	GNDDIG2	POWER	Digital I/O ground
48	VDDDIG2	POWER	Digital core LDO supply

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
Vcc	Power supply voltage (VCCxA, VCCxB)	-0.3		30	V
VDD_DIG	Digital supply voltage	-0.3		4	V
VDD3V3 VDD3V3CHP	Charge pump and analog path LDO supply	-0.3		4	V
Top	Operating junction temperature	0		150	°C
Tstg	Storage temperature	-40		150	°C
R_{Line}	Load impedance - line driver mode	1			kΩ
R_{Hp}	Load impedance - headphone driver mode	16			Ω
R_{Btl}	Load impedance - power output-BTL mode	5			Ω

Warning: Stresses beyond those listed in *Table 3* above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supplies with nominal values rated within the recommended operating conditions may rise beyond the maximum operating conditions for a short time when no or very low current is sunk (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
Rth j-case	Thermal resistance junction-case (thermal pad)			1.5	°C/W
Tth-sdj	Thermal shutdown junction temperature		150		°C
Tth-w	Thermal warning temperature		130		°C
Tth-sdh	Thermal shutdown hysteresis		20		°C

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
Vcc	Power supply voltage (VCCxA, VCCxB)	4.5		26	V
VDD_DIG	Digital supply voltage	2.7	3.3	3.6	V
VDD3V3 VDD3V3CHP	Charge pump and analog path LDO supply	2.7	3.3	3.6	V
Tamb	Ambient temperature	0		70	°C
R_{Line}	Load impedance - line driver mode	5	10		kΩ
R_{Hp}	Load impedance - headphone driver mode	16	32		Ω
R_{Btl}	Load impedance - power output-BTL mode	5	8		Ω

3.4 Electrical specifications for the digital section

The specifications given in this section are valid for the operating conditions: VDD_DIG = 3.3 V, T_{amb} = 25 °C.

Table 6. Electrical specifications - digital section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low level input current without pull-up/down device	Vi = 0 V			0.5	µA
I_{ih}	High level input current without pull-up/down device	Vi = VDD_DIG = 3.3 V			0.1	µA
V_{il}	Low level input voltage				0.8	V
V_{ih}	High level input voltage		2.0			V
V_{ol}	Low level output voltage	Iol = 2 mA			0.15	V
V_{oh}	High level output voltage	Ioh = 2 mA	VDD_DIG -0.15			V
R_{pu}	Pull-up/down resistance			50		kΩ

3.5 Electrical specifications for the power section

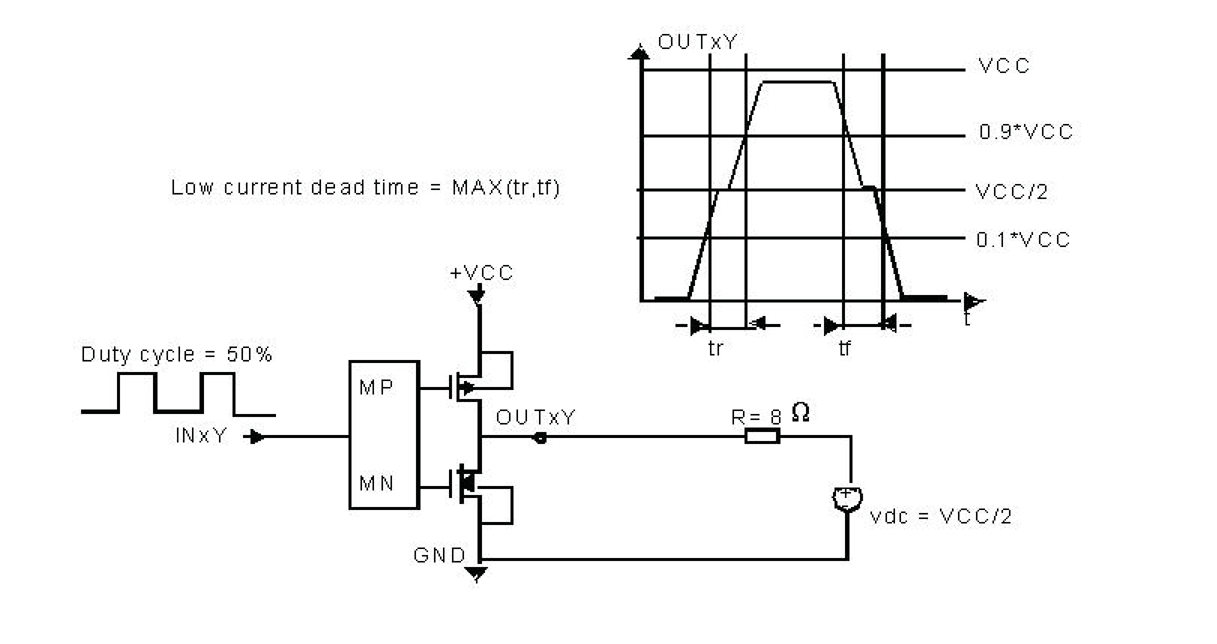
The specifications given in this section are valid for the operating conditions: V_{CC} = 24 V, f = 1 kHz, f_{sw} = 384 kHz, T_{amb} = 25° C and R_L = 8 Ω, unless otherwise specified.

Table 7. Electrical specifications - power section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Output power BTL	Digital limited(1)		20		W
	Output power SE	Digital limited(1)		5		
	Output power SE R_L = 4 Ω	Digital limited(1)		9		
R_{dsON}	Power Pchannel/Nchannel MOSFET	I_d = 1.5 A		120		mΩ
gP	Power Pchannel R_{dsON} matching	I_d = 1.5 A	95			%
gN	Power Nchannel R_{dsON} matching	I_d = 1.5 A	95			%
Idss	Power Pchannel/Nchannel leakage				10	µA
I_{LDT}	Low current dead time (static)	Resistive load(2)		8	15	ns
t_r	Rise time	Resistive load(2)		10	18	ns
t_f	Fall time	Resistive load(2)		10	18	ns
I_{vcc}	Supply current from Vcc in power-down	PWRDN = 0		0.1	1	µA
	Supply current from Vcc in operation	PCM Input signal = -60 dBfs, Switching frequency = 384 kHz, No LC filters		52	60	mA
Ilim	Overcurrent limit		4	5	6.5	A
UVL	Undervoltage protection			3.5	4.3	V
V_{OV}	Overvoltage protection			28.25		V
t_{min}	Output minimum pulse width	No load	20	30	60	ns
DR	Dynamic range			100		dB
SNR	Signal-to-noise ratio, ternary mode	A-weighted		100		dB
	Signal-to-noise ratio, binary mode	A-weighted		90		dB
THD+N	Total harmonic distortion + noise	FFX stereo mode, Po = 1 W, f = 1 kHz		0.2		%
X_{TALK}	Crosstalk	FFX stereo mode, <5 kHz, one channel driven at 1 W and other channel measured		80		dB
η	Peak efficiency, FFX mode	Po = 2 x 20 W into 8 Ω		90		%

1. The related THD can be defined through appropriate DRC settings (see section: *4.3: STCompressorTM*)
2. Refer to *Figure 3: Test circuit*.

Figure 3. Test circuit



3.6 Electrical specifications for the analog section

The specifications given in this section are valid for the operating conditions: V_{CC} = 24 V f = 1 kHz, T_{amb} = 25 °C, VDD3V3 = 3.3 V, R_{Line}= 5 kΩ, R_{Hp} = 32 Ω, unless otherwise specified.

Table 8. Electrical specifications for the analog section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vout	Output voltage for line out	G_v = 2.5, THD < 1%, Rload = 5 kΩ	1.9		2.1	Vrms
Pout	Output voltage for HP out	THD+N = 10%, G_v = 2.5, Rload = 32 Ω		40		mW
DR	Dynamic range for line out	Vout = 2 V_{RMS}, F_{in} = 200 Hz, V_{in} = 0.8 mV (-60 dBFs)		100		dB
X-Talk	Channel separation for line out	V_{out} = 2 Vrms, G_v = 2.5		75		dB
PSRR	Power supply rejection ratio	HP mode, P_0 = 15 mW		70		dB
		Line out mode, V_{Out} = 2 Vrms		70		
R_{in}	Line input resistance				30(1)	kΩ
THD+N	Total harmonic distortion + noise	HP mode, V_{out} = 200 mV_{RMS}, G_v = 2.5		0.03		%
		Line out mode, V_{Out} = 0.2 Vrms, G_v = 2.5		0.03		%

1. Refer to *8.2: Headphone and 2 Vrms line out*, *Figure 47: Headphone and line out block diagram*, R_{in} = R1

4 Device overview

The mentioned hyperlink in this section relates to the default New Map *Section 6: Register description: New Map*.

4.1 Processing data path

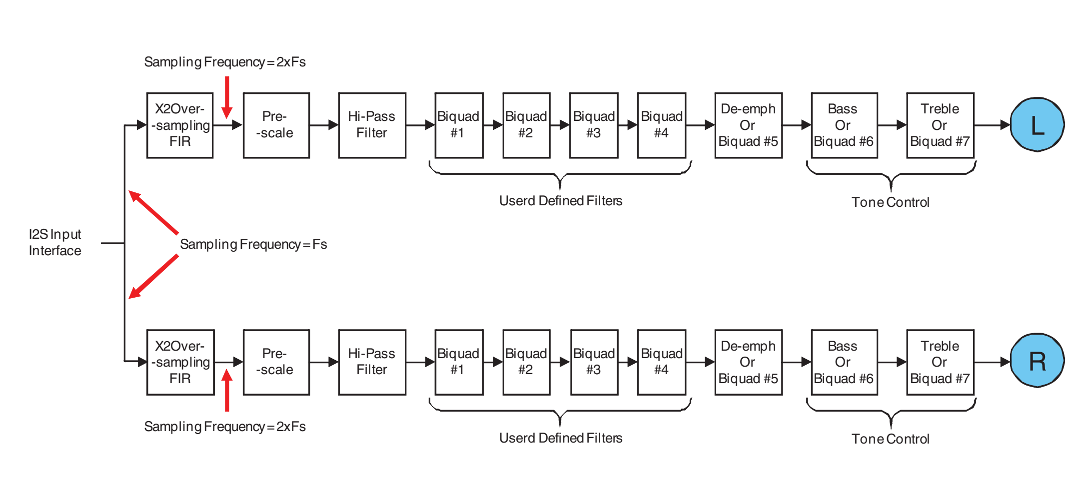
The whole STA381BW processing chain is composed of two consecutive sections. In the first one dual-channel processing is implemented (*Figure 4*) and then each channel is fed into the post-mixing block allowing to generate either a third channel (typically used in 2.1 output configurations together with crossover filters) or to have the channels processed by the dual-band DRC block (2.0 output configuration with crossover filters used to define the cutoff frequency of the two bands).

The first section begins with a 2x oversampling FIR filter allowing 2*Fs audio processing. Then a selectable high-pass filter removes the DC level (enabled if HFB = 0). The channel 1 and 2 processing chain can include up to 8 filters, depending on the selected configuration (bits BQL, BQ5, BQ6, BQ7 and XO[3:0]). By default, 4 independent filters per channel are enabled, plus the pre-configured Bass and Treble controls (BQL=0, BQ5=0, BQ6=0, BQ7=0).

The STA381BW offers the possibility to share the filter coefficients between the two processing channels. When this option is set (BQL=1), filters from the 1st to the 4th have the same coeffcients set. Under these conditions, filters from the 5th to 7th can be used as custom filters as well (provided the relevant BQx bits are set). Once again filter coefficients are shared between the two processing channels.

Moreover the common 8th filter, from the subsequent processing section, can be available on both channels (provided the pre-defined crossover frequencies are not used, XO[3:0]=0, and the dual-band DRC is not used).

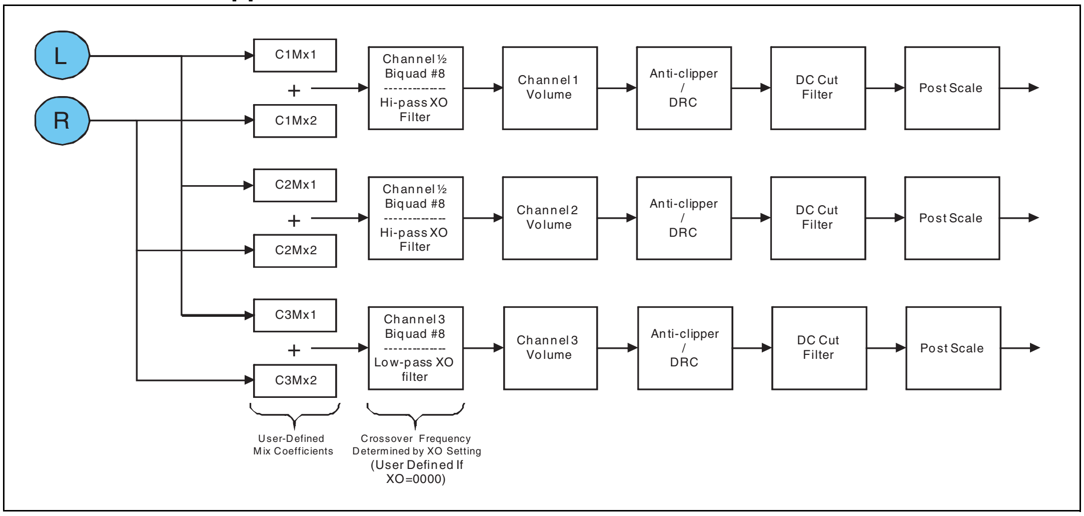
Figure 4. Processing path, first part



The second processing stage embeds a mixing block, a biquadratic/crossover filter, a DRC stage, the volume control, a DC cut filter and a post scaler. Depending on the device settings, the following configuration and features are available:

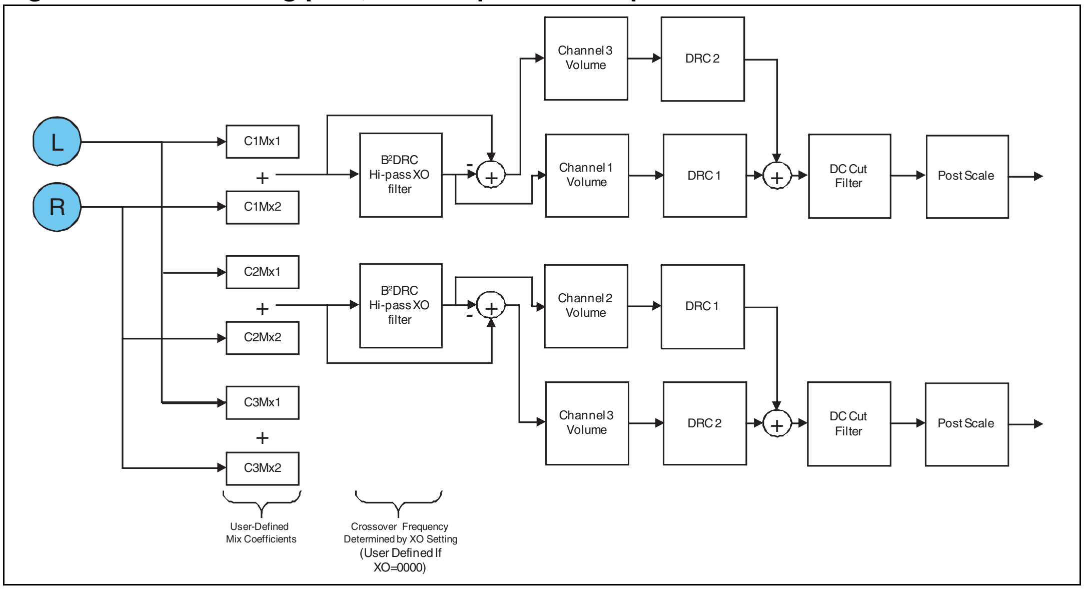
- 2.1 output with individually configurable anticlipper/DRCs (*Figure 5*): two individually configurable DRC/anticlippers are available while the eighth biquadratic filter, jointly with the mixer block, can be used to perform LFE. This configuration and features ensure the backward compatibility with previous Sound Terminal® products.

Figure 5. Processing path, second part: 2.1 output with individually configurable anticlipper/DRCs



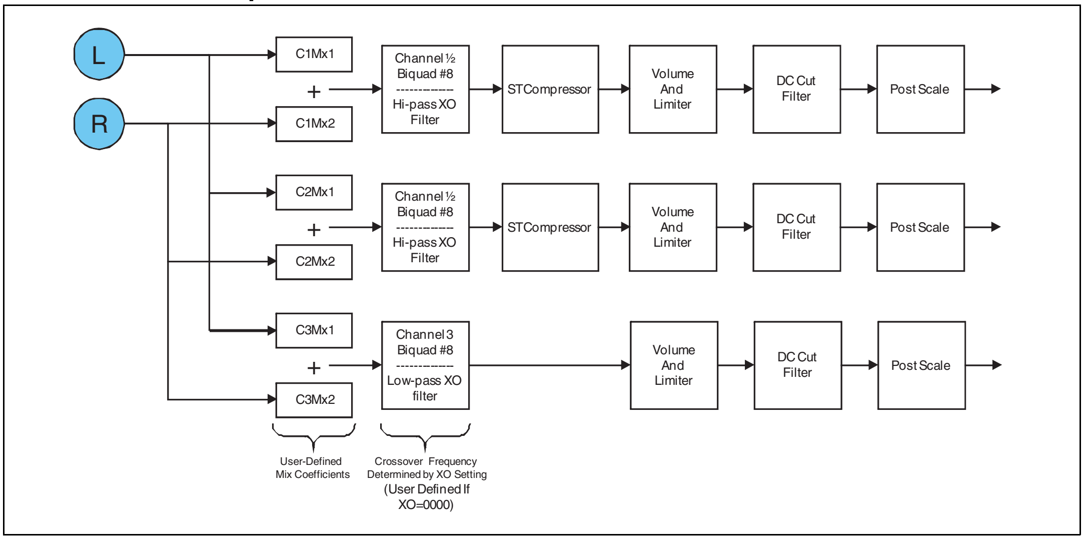
- 2.0 output with B^2DRC (*Figure 6*): the mixer and the eighth biquadratic filter are used to divide the channel into two sub-bands, then each sub-band is independently processed by a DRC block. The two bands are then re-composed and fed to the following processing blocks. The crossover frequency is user-selectable. This configuration and features ensure the backward compatibility with the previous Sound Terminal® products. For further information please refer to *Chapter 6.11.1: Dual-band DRC*.

Figure 6. Processing path, second part: 2.0 output with B^2DRC



- 2.1 output with STCompressor™ (*Figure 7*): the STA381BW embeds the latest, state-of-the-art multi-band dynamic, range compressor, called STCompressor™. When using this configuration, up to 10 biquad filters are available for dedicated processing. Please refer to *Section 4.3: STCompressorTM* for further information about this feature.

Figure 7. Processing path, second part: 2.1 output configuration with STCompressor™



4.2 Input oversampling

Figure 4 shows the input oversampling block in front of the main processing. When 32 kHz Fs is used, the default x2 oversampling ratio can be increased to a x3.

Activating this feature, it is possible to have a 384 kHz PWM switching frequency (instead of the default 256 kHz) when 32 kHz Fs is used.

When bit 0 of register PLLCFG1 is set to one, the feature is activated so that the PLL ratio is modified to generate 49.152 MHz internal clock and the audio data path (after the input oversampling block) is running at 96 kHz.

It is not recommended to use the x3 oversampling feature when Fs > 32 kHz because of the PLL maximum frequency constraint.

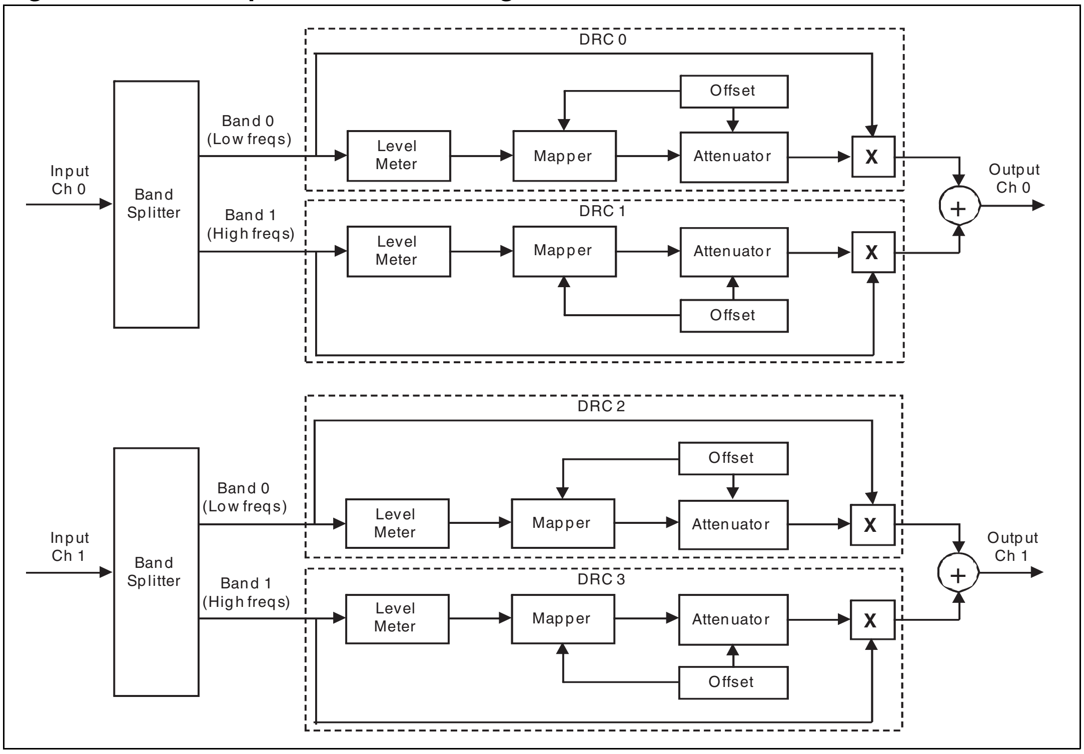
4.3 STCompressor^{TM}

The STCompressor^{TM} (STC from now on) is a stereo, dual-band Dynamic Range Control (DRC) and its main purpose is to provide optimum output power level control for speaker protection, preserving as much as possible the original audio quality of the signal.

Two main I^2C registers control the STC behavior: STCCFG0 and STCCFG1. On top of the data flow control bits, these registers also allow enabling the checksum engine to protect the STC filters from erroneous coefficients downloads, thus improving the final application circuitry and safety of the speakers.

4.3.1 STC block diagram

Figure 8. STCompressor™ block diagram



The STC takes as input 2 channels and every channel is processed independently (i.e. an independent DRC for each band of each channel) following the steps listed below (*Figure 8*):

1. Splits the input signal into 2 bands (band splitter)
2. Measures the level of the signal (level meter)
3. Computes the attenuation (mapper)
4. Applies the attenuation and offset (attenuator)

The band splitter settings are common to both the processing channels while the settings of the remaining blocks can be independently set for each band of each processing channel.

Caution: All the settings explained hereafter apply only to the behavior of the STCompressor™. For the settings concerning other device operating configurations (see *Chapter 4.1: Processing data path*) please refer to the appropriate paragraphs and registers.

4.3.2 Band splitter

The band splitter block is used to divide the signal into 2 sub-bands (typically low- and high-frequency bands). This is done through two 2^{nd} order biquads (IIR filters) for each band, thus allowing to have up to a 4^{th} order filter per band. This feature guarantees a totally flat band recombination (see *Figure 9*). Using different filtering orders, indeed, causes a non-negligible gain around the filter's cutoff frequency, endangering the overall audio fidelity and, eventually, also the safety of the speaker. The sub-band recombination can be enabled or disabled.

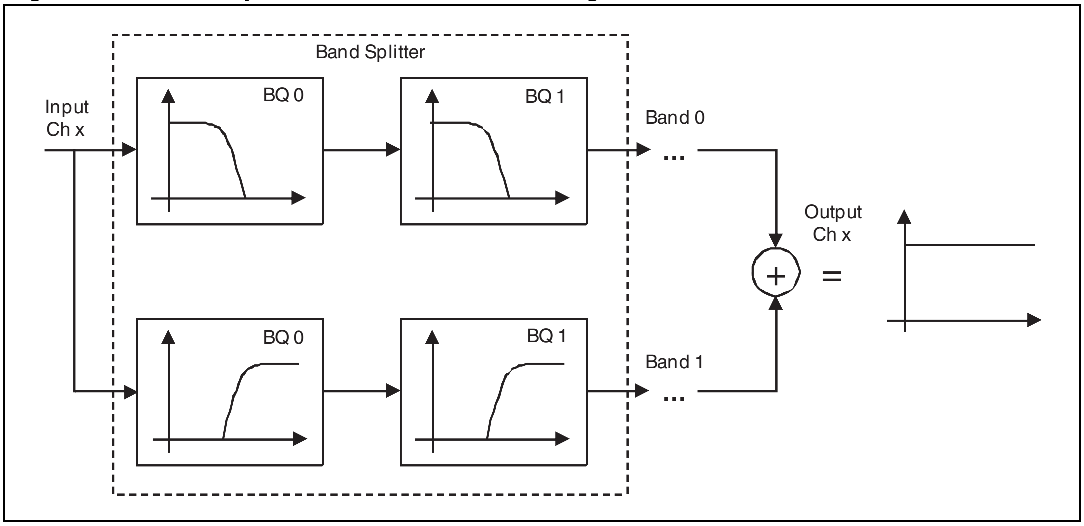
The band splitter filter coefficients have a user-selectable range [-1, 1), [-2, 2) and [-4, 4). The RAM coefficient 0x7 is responsible for these settings according to *Table 9*. The range default value is [-4, 4).

Table 9. Coefficients extended-range configuration 0x74h

CEXT_Bx[1]	CEXT_Bx[0]	Range
0	0	[-1;1)
0	1	[-2;2)
1	0	[-4;4)
1	1	Reserved

Please refer to *Section 6.24: User-defined coefficient control registers (addr 0x27 - 0x37)* and to *Table 13* for further details.

Figure 9. Band splitter with 4^{th} order filtering



4.3.3 Level meter

The level meter block measures the input signal level (in dB). Two kinds of measures are performed: peak and RMS. The mapper configuration and the input signal automatically determine which measurement to take into account.

4.3.4 Mapper

The mapper block computes the appropriate attenuation value (expressed in dB) to be applied to the signal, basing its calculations on the level meter output value, on the compressor threshold and on the limiter threshold.The attenuation value is then passed to the attenuator block.

The STC reacts differently depending on these three parameters (*Figure 10*):

- level meter output value < compressor threshold < limiter threshold: under these circumstances the signal level is small enough to not require any type of limiting/compressing action. The signal remains unchanged.
- compressor threshold < level meter output value < limiter threshold: under these circumstances the signal level is compressed to a ratio determined by the compressor rate.
- compressor threshold < limiter threshold < level meter output value: under these circumstances the signal level exceeds the limiter threshold which represents the maximum output power allowed. The signal is limited to avoid unpredictable effects and damages.

The compressor threshold, the limiter threshold and the compressor rate are all user-selectable parameters. The compressor threshold range of value is [-48, 0] dB with a 0.25 dB step. The limiter threshold range of values is [-24, +12] dB with a 0.25 dB step. The compressor ratio range of value is [0, 15], the meaning of these values is specified in *Table 10*. For further details please refer to *Table 12*. Either setting the compressor rate to 1:1 or setting the compressor threshold greater than the limiter threshold makes the STC behave as a pure limiter (*Figure 11*).

Figure 10. STCompressor™ behavior

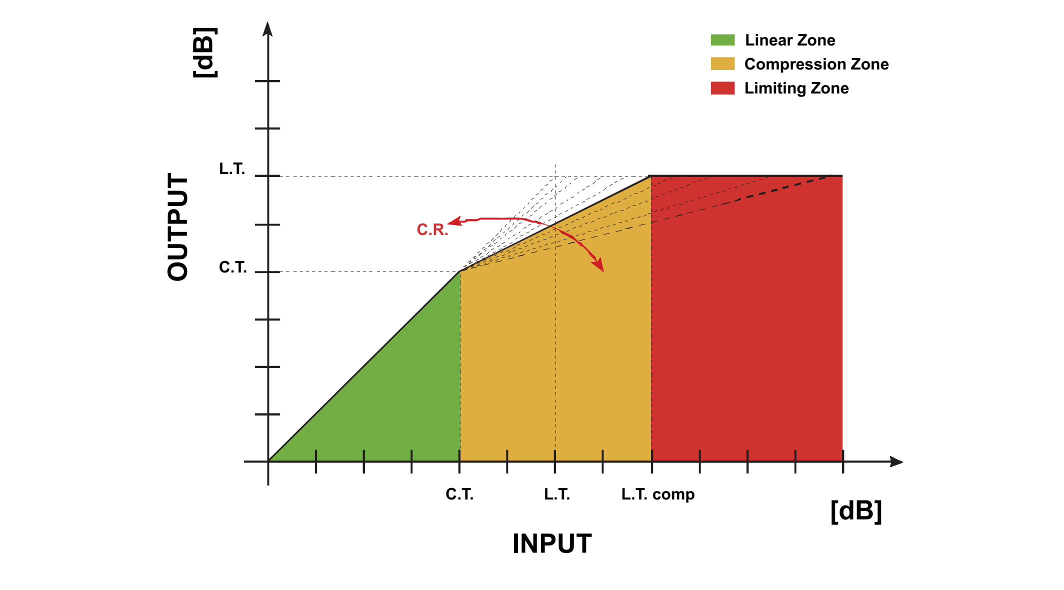


Figure 11. STCompressor^{TM} behavior as a limiter

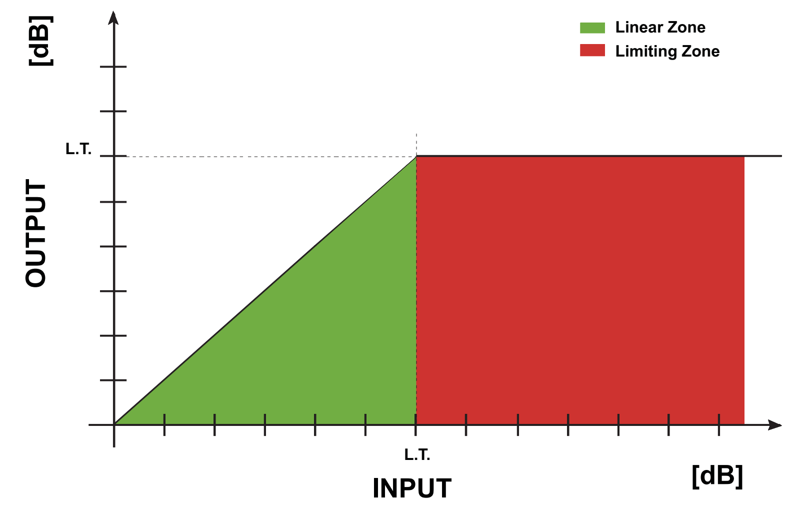


Table 10. Compressor ratio

Compressor ratio	Ratio value
0	1:1
1	1:1.25
2	1:1.5
3	1:1.75
4	1:2
5	1:2.5
6	1:3
7	1:3.5
8	1:4
9	1:4.5
10	1:5
11	1:5.5
12	1.6
13	1:7
14	1:8
15	1:16

4.3.5 Attenuator

The attenuation is characterized by two different phases: attack and release.

Given an input signal above the limiter threshold, during the attack phase the STC decreases the gain in order to reach the output level determined by the mapper. In this process the key parameter is the attack rate (dB/ms) which determines how fast the STC reacts according to the following equation:

$$\text{AttackTime} = \frac{\text{OutputSignalLevel} - \text{MapperLevel}}{\text{AttackRate}}$$

where:

- *Output Signal Level* is the attenuated signal coming from the attenuator block itself and used as feedback
- *Mapper Level* is the target signal level to be reached

The attack rate is user-selectable and its range is [0, +16] dB/ms with a 0.25 dB/ms step.

Given an input signal moving below the limiter threshold, during the release phase the STC increases the gain in order to return the original input signal dynamic. In this process the key parameter is the release rate (dB/ms) which determines how fast the STC releases the attenuation on the input signal according to the following equation:

$$\text{ReleaseTime} = \frac{\text{OutputSignalLevel} - \text{MapperLevel}}{\text{ReleaseRate}}$$

The release rate is user-selectable and its range is [0.0078, 1) dB/ms with a 0.0039 dB/ms step.

4.3.6 Dynamic attack

Due to its dynamic, the input signal may exceed the limiter threshold by a variable amount of decibels. In such different situations it might be useful to be able to tune the attack rate to make the STC react slower or faster depending on the context. The attack rate value, set by the user, can be dynamically varied through the dynamic attack rate (DAR). It is a parameter (expressed in ms/dB) acting as a weighted coefficient, multiplying the difference between the attenuator output signal and the mapper target level. The dynamic attack rate affects the user-programmed attack rate according to the following equations:

$$\text{DynamicAttackTime} = (\text{OutputSignalLevel} - \text{MapperLevel}) \times \text{DAR}$$

$$\text{AttackTime} = \frac{\text{OutputSignalLevel} - \text{MapperLevel}}{\text{AttackRate}} + \text{DynamicAttackTime}$$

$$\Rightarrow \text{AttackRate} = \frac{\text{OutputSignalLevel} - \text{MapperLevel}}{\text{AttackTime} - \text{DynamicAttackTime}}$$

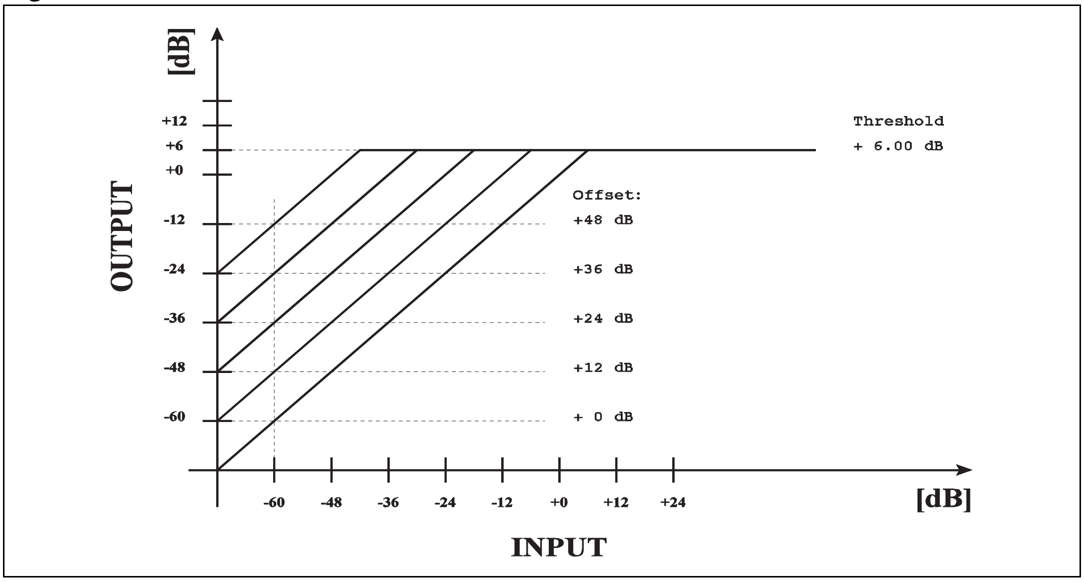
The DAR is user-definable and its range of values is [0, +1) ms/dB, (*Table 12*) with a 0.0039 ms/dB step. The DAR is the same for all 4 sub-bands.

4.3.7 Offset

The offset is a user-selectable gain or volume control. When using the STC it is advised to use the offset to tune the output volume instead of the regular volume controls. The offset is located before the attenuator block, ensuring that the output power limit (limiter threshold) is never exceeded (*Figure 12*). On the other side, the traditional volume control is located after the STC attenuator, thus a wrong setting of this control could nullify the STC effect.

Each sub-band has its own and independent offset. Its range is [0, +48] dB with a 0.25 dB step (*Table 12*).

Figure 12. Offset effect

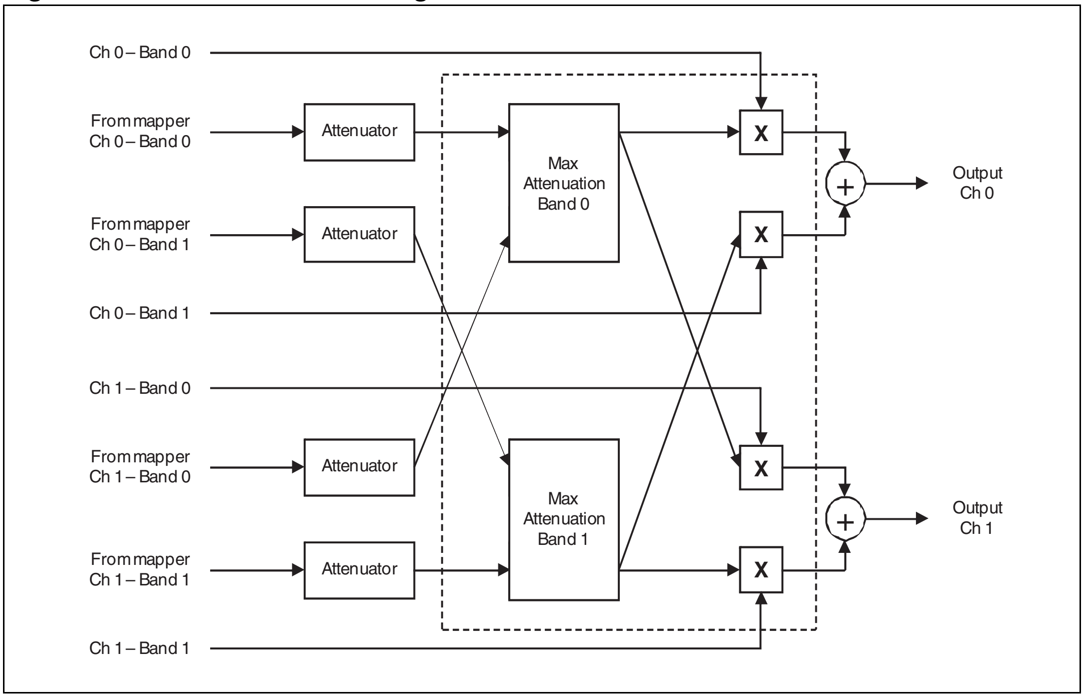


4.3.8 Stereo link

The stereo link feature allows applying the same attenuation to the corresponding band of each channel (i.e. band 0 left channel and band 0 right or band 1 left channel and band 1 right channel). This should help to prevent image shifting that could occur when individually compressing each channel and causing a volume mismatch between left and right.

When the stereo link is active, the proper attenuation for each band is independently computed, then the highest one for each band is applied (*Figure 13*).

Figure 13. Stereo link block diagram



4.3.9 Programming of coefficients

The coefficients are expressed in different value ranges and in decimal notation (refer to the previous paragraphs). In order to be programmed they must be converted into a [-1, +1) range and in hexadecimal notation (*Table 11*). This can be achieved with the following procedure:

- if CoeffDecValue>0

$$\text{CoeffI2CValue} = \text{rnd}((\text{CoeffDecValue}/2^6) \times 2^{23})$$

- if CoeffDecValue<0

$$\text{CoeffI2CValue} = 2^{24} - \text{rnd}((\text{CoeffDecValue}/2^6) \times 2^{23})$$

where CoeffI2CValue is the final decimal value to be converted into hexadecimal notation while CoeffDecValue is the coefficient value (in decimal notation) to start from.

Table 11. Conversion example

Original value (dec)	I^2C value (hex)
+48.00	0x600000
+24.00	0x300000
+16.00	0x200000
+12.00	0x180000
+06.00	0x0C0000
+02.00	0x040000
+01.00	0x020000
-01.00	0xFE0000
-02.00	0xFC0000
-06.00	0xF40000
-12.00	0xE80000
-24.00	0xD00000
-48.00	0xA00000

4.3.10 Memory map

All the control parameters listed in the previous paragraphs are stored in the internal device memory. Please refer to *Table 12* and *Table 13* for a complete list of their addresses.

For the programming procedure please refer to *Section 6.24: User-defined coefficient control registers (addr 0x27 - 0x37)*. Be aware that the read-all operation is not available for the STC coefficients memory.

Table 12. STC coefficients memory map

Function			Address	Parameter	Range	Precision	Unit	Default
CH0	Band 0	DRC 0	0x54	RR: release rate	[0.0078,1)	0.0039	dB/ms	0x200000
			0x55	AR: attack rate	[0,16]	0.25	dB/ms	0x200000
			0x56	LT: limiter threshold	[-24, +12]	0.25	dB	0x000000
			0x57	CR: compressor ratio	[0,15]	1	index	0x000000
			0x58	CT: compressor threshold	[-48, 0]	0.25	dB	0x000000
	Band 1	DRC 1	0x59	RR: release rate	[0.0078,1)	0.0039	dB/ms	0x200000
			05A	AR: attack rate	[0,16]	0.25	dB/ms	0x200000
			0x5B	LT: limiter threshold	[-24, +12]	0.25	dB	0x000000
			0x5C	CR: compressor ratio	[0,15]	1	index	0x000000
			0x5D	CT: compressor threshold	[-48, 0]	0.25	dB	0x000000
CH1	Band 0	DRC 2	0x5E	RR: release rate	[0.0078,1)	0.0039	dB/ms	0x200000
			0x5F	AR: attack rate	[0,16]	0.25	dB/ms	0x200000
			0x60	LT: limiter threshold	[-24, +12]	0.25	dB	0x000000
			0x61	CR: compressor ratio	[0,15]	1	index	0x000000
			0x62	CT: compressor threshold	[-48, 0]	0.25	dB	0x000000
	Band 1	DRC 3	0x63	RR: release rate	[0.0078,1)	0.0039	dB/ms	0x200000
			0x64	AR: attack rate	[0,16]	0.25	dB/ms	0x200000
			0x65	LT: limiter threshold	[-24, +12]	0.25	dB	0x000000
			0x66	CR: compressor ratio	[0,15]	1	index	0x000000
			0x67	CT: compressor threshold	[-48, 0]	0.25	dB	0x000000
OFFSET			0X68	OFS0: offset DRC 0	[0, +48]	0.25	dB	0x000000
			0X69	OFS1: offset DRC 1	[0, +48]	0.25	dB	0x000000
			0X6A	OFS2: offset DRC 2	[0, +48]	0.25	dB	0x000000
			0X6B	OFS3: offset DRC 3	[0, +48]	0.25	dB	0x000000
Dynamic attack rate			0x71	DAR: dynamic attack rate	[0, 1)	0.0039	ms/dB	0x000000
CRC expected			0x72					
CRC computed			0x73					
Biquads CTRL			0x74	Band splitter filter coefficients range				0x0000AA

Table 13. STC band splitter filters memory map

Function		Address	Coefficient	Range	Default
Band 0	BQ0	0x40	B1/2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x41	B2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x42	-A1/2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x43	-A2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x44	B0/2	[-1, 1), [-2, 2), **[-4, 4)**	0x100000
	BQ1	0x45	B1/2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x46	B2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x47	-A1/2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x48	-A2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x49	B0/2	[-1, 1), [-2, 2), **[-4, 4)**	0x100000
Band 1	BQ0	0x4A	B1/2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x4B	B2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x4C	-A1/2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x4D	-A2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x4E	B0/2	[-1, 1), [-2, 2), **[-4, 4)**	0x100000
	BQ1	0x4F	B1/2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x50	B2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x51	-A1/2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x52	-A2	[-1, 1), [-2, 2), **[-4, 4)**	0x000000
		0x53	B0/2	[-1, 1), [-2, 2), **[-4, 4)**	0x100000

5 I^2C bus specification

The STA381BW supports the I^2C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master). This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA381BW is always a slave device in all of its communications. It supports up to 400 kb/sec rate (fast-mode bit rate). The STA381BW I^2C is a slave-only interface. The I^2C interface works properly only in the case that the master clock generated by the PLL has a frequency 10 times higher compared to the frequency of the applied SCL signal.

5.1 Communication protocol

5.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. An SDA transition while the clock is high is used to identify a START or STOP condition.

5.1.2 Start condition

START is identified by a high-to-low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

5.1.3 Stop condition

STOP is identified by a low-to-high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the STA381BW and the bus master.

5.1.4 Data input

During the data input the STA381BW samples the SDA signal on the rising edge of clock SCL. For correct device operation, the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

5.2 Device addressing

To start communication between the master and the STA381BW, the master must initiate with a start condition. Following this, the master sends to the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The seven most significant bits are the device address identifiers, corresponding to the I^2C bus definition. In the STA381BW the I^2C interface has two device addresses depending on the SA port configuration, 0x38 when SA = 0, and 0x3A when SA = 1.

The eighth bit (LSB) identifies read or write operation RW, this bit is set to 1 for read mode and to 0 for write mode. After a START condition the STA381BW identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

5.3 Write operation

Following the START condition, the master sends a device select code with the RW bit set to 0. The STA381BW acknowledges this and then waits for the byte of the internal address. After receiving the internal byte address the STA381BW again responds with an acknowledgement.

5.3.1 Byte write

In the byte write mode the master sends one data byte which is acknowledged by the STA381BW. The master then terminates the transfer by generating a STOP condition.

5.3.2 Multi-byte write

The multi-byte write mode can start from any internal address. The master generating a STOP condition terminates the transfer.

5.4 Read operation

5.4.1 Current address byte read

Following the START condition, the master sends a device select code with the RW bit set to 1. The STA381BW acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

5.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA381BW. The master acknowledges each data byte read and then generates a STOP condition, terminating the transfer.

5.4.3 Random address byte read

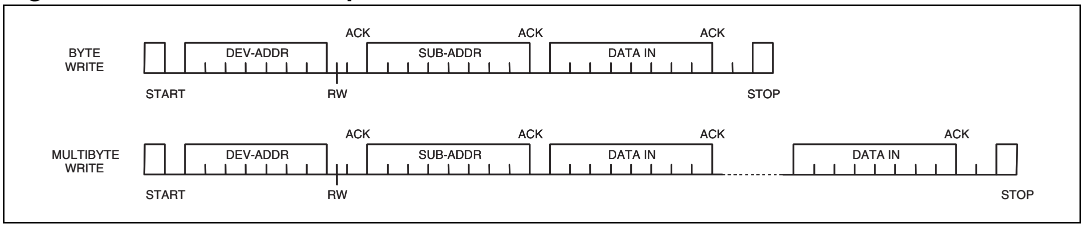
Following the START condition, the master sends a device select code with the RW bit set to 0. The STA381BW acknowledges this and then the master writes the internal address byte. After receiving the internal byte address, the STA381BW again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA381BW acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

5.4.4 Random address multi-byte read

The multi-byte read mode can start from any internal address. Sequential data bytes are read from sequential addresses within the STA381BW. The master acknowledges each data byte read and then generates a STOP condition, terminating the transfer.

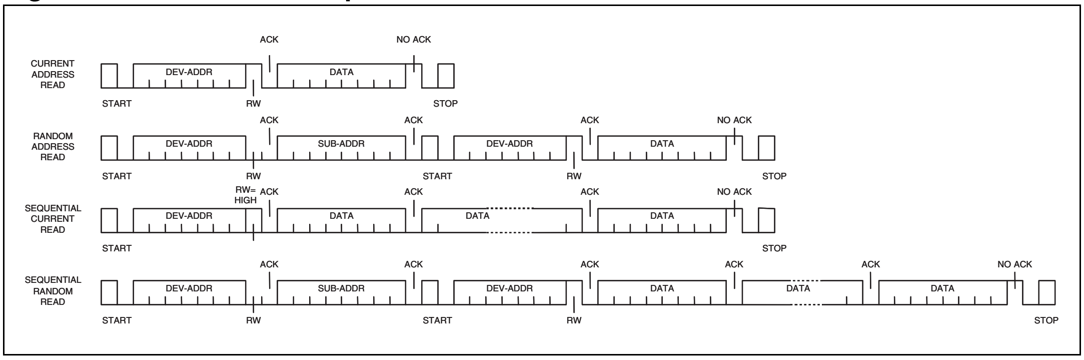
5.4.5 Write mode sequence

Figure 14. Write mode sequence



5.4.6 Read mode sequence

Figure 15. Read mode sequence



6 Register description: New Map

Mapping of two registers is available on the STA381BW, the selection is done by setting register 0x7E bit D7. By default, 0x7E is set to 1 and refers to a map that is not compatible with previous Sound Terminal devices. This register's mapping is also called “New Map”.

To keep compatibility with previous Sound Terminal devices, 0x7E bit D7 must be set to 0 after device turn-on and after any reset (via SW or via external pin). Please refer to *Section 7: Register description: Sound Terminal compatibility* for all the information about device compatibility.

Missing addresses are to be considered as reserved.

Table 14. Default register map table: NEW MAP

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	CLK	CLK_CFG[3:0]							I2S
0x01	STATUS	FAULT	DRCCRC	EQCRC	BADPWM			I2SERR	PLLUL
0x02	RESET								SRESET
0x03	SVOL							SVOL[1:0]	
0x04	MVOL	MVOL[7:0]							
0x05	FINEVOL							FINE[1:0]	
0x06	CH1VOL	CH1VOL[7:0]							
0x07	CH2VOL	CH2VOL[7:0]							
0x08	POST	POST[7:0]							
0x09	OPER							OPER[1:0]	
0x0A	FUNCT		CRC	APEQ	PEQ		AMDRC	MDRCE	DRC
0x10	HPCFG								MUTE
0x11	CONFA	FDRB			IR1	IR0	MCS2	MCS1	MCS0
0x12	CONFB	C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
0x13	CONFC			CSZ3	CSZ2	CSZ1	CSZ0		
0x14	CONFD	SME	ZDE		BQL	PSL	DSPB		
0x15	CONFE		ZCE		PWMS	AME	NSBW		
0x16	CONFF	EAPD	PWDN		LDTE	BCLE	IDE		
0x17	MUTELOC	LOC1	LOC0			C3M	C2M	C1M	MMUTE
0x1B	CH3VOL	CH3VOL[7:0]							
0x1D	AUTO	XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0x1F	C1CFG					C1BO	C1VBP	C1EQBP	C1TCB
0x20	C2CFG					C2BO	C2VBP	C2EQBP	C2TCB
0x21	C3CFG	C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VBP		
0x22	TONE	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0x23	L1AR	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x24	L1ATRT	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0

Table 14. Default register map table: NEW MAP (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x25	L2AR	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x26	L2ATRT	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0x27	CFADDR			CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x28	B1CF1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x29	B1CF2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x2A	B1CF3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x2B	B2CF1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x2C	B2CF2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x2D	B2CF3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x2E	A1CF1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
0x2F	A1CF2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x30	A1CF3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0x31	A2CF1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x32	A2CF2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x33	A2CF3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x34	B0CF1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x35	B0CF2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x36	B0CF3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x37	CFUD					RA	R1	WA	W1
0x3C	FDRC1	FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0x3D	FDRC2	FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0x3F	MTH2			MTH[21:16]					
0x40	MTH1	MTH[15:8]							
0x43	EATH1	EATHEN1	EATH1[6:0]						
0x44	ERTH1	ERTHEN1	ERTH1[6:0]						
0x45	EATH2	EATHEN2	EATH2[6:0]						
0x46	ERTH2	ERTHEN2	ERTH2[6:0]						
0x47	CONFX			PS48DB	XAR1	XAR2	BQ5	BQ6	BQ7
0x52	PLLFRAC1	PLL_FRAC[15:8]							
0x53	PLLFRAC2	PLL_FRAC[7:0]							
0x54	PLLDIV	PLL_DITH[1:0]		PLL_NDIV[5:0]					
0x55	PLLCFG0	PLL_DPD	PLL_FCT	PLL_STB	PLL_ STBBYP	PLL_IDIV[3:0]			
0x56	PLLCFG1			PLL_DIRP	PLL_PWD	PLL_BYP	OSC_PD		BOOST32K
0x57	PLLSTATE					BYPSTATE	PDSTATE	OSCOK	LOWCK
0x58	SHOK						GNDSH	VCCSH	OUTSH
0x5A	CXT41	CEXT_B4[1:0]		CEXT_B3[1:0]		CEXT_B2[1:0]		CEXT_B1[1:0]	

Table 14. Default register map table: NEW MAP (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x5B	CXT75			CEXT_B7[1:0]		CEXT_B6[1:0]		CEXT_B5[1:0]	
0x5C	MISC1	RPDNEN		BRIDGOFF			CPWMEN		
0x5D	MISC2	LPDP	LPD	LPDE	PNDLSL[2:0]				SHEN
0x5E	BPTH	BPTH[5:0]							
0x60	BPTIM	BPTIM[7:0]							
0x61	ZCCFG0	WTHH	WTHL	FINETH	HSEL[1:0]		ZMTH[2:0]		
0x62	ZCCFG1	RMS_CH0[7:0]							
0x63	ZCCFG2	RMS_CH0[15:8]							
0x64	ZCCFG3	RMS_CH1[7:0]							
0x65	ZCCFG4	RMS_CH1[15:8]							
0x66	HPCFG	HPLN				CPFEN	CPOK	ABFAULT	DCROK
0x69	F3XCFG1	F3XLNK							
0x6A	F3XCFG2	F3X_FAULT			F3X_SM_SLOPE[2:0]			F3X_MUTE	F3X_ENA
0x6B	STCCFG0						NP_ CRCRES		
0x6C	STCCFG1							STC_LNK	
0x6F	MTH0	MTH[7:0]							
0x70	CHPSINC			CHPI	INITCNT[3:0]				CHPRD
0x71	BQCHKE0	BQ_CKE[7:0]							
0x72	BQCHKE1	BQ_CKE[15:8]							
0x73	BQCHKE2	BQ_CKE[23:16]							
0x74	XCCHKE0	XC_CKE[7:0]							
0x75	XCCHKE1	XC_CKE[15:8]							
0x76	XCCHKE2	XC_CKE[23:16]							
0x77	BQCHKR0	BQ_CKR[7:0]							
0x78	BQCHKR1	BQ_CKR[15:8]							
0x79	BQCHKR2	BQ_CKR[23:16]							
0x7A	XCCHKR0	XC_CKR[7:0]							
0x7B	XCCHKR1	XC_CKR[15:8]							
0x7C	XCCHKR2	XC_CKR[23:16]							
0x7D	CHKCTRL	XCAUTO				BCAUTO			
0x7E	MISC4	SMAP						WRA	CH12

6.1 CLK register (addr 0x00)

D7	D6	D5	D4	D3	D2	D1	D0
CLK_CFG[3:0]				Reserved	Reserved	Reserved	I2S
0	0	0	0	0	0	0	0

Table 15. CLK register

Bit	R/W	RST	Name	Description
7	R/W	0	CLK_CFG[3:0]	0000: 44.1/48 kHz BITCLK = 64 Fs 0001: 32 kHz BITCLK = 64 Fs 0010: 96 kHz BITCLK = 64 Fs 0011: 48/44.1/32 kHz MCK = 256 Fs others: clock configuration depends on IR/MCS bits
6	R/W	0		
5	R/W	0		
4	R/W	0		
0	R/W	0	I2S	‘0’ = SAI configured in I^2S mode ‘1’ = SAI configuration depends on CONFB register status

6.2 STATUS register (addr 0x01)

D7	D6	D5	D4	D3	D2	D1	D0
FAULT	DRCCRC	EQCRC	BADPWM	Reserved	Reserved	I2SERR	PLLUL
NA	NA	NA	NA	NA	NA	NA	NA

Table 16. STATUS register

Bit	R/W	RST	Name	Description
7	R		FAULT(1)	‘0’ = the power bridge is in fault condition ‘1’ = the power bridge is in normal condition
6	R		DRCCRC	‘0’ = normal operation ‘1’ = CRC error on DRC BIQUADS
5	R		EQCRC	‘0’ = normal operation ‘1’ = CRC error on BIQUADS
4	R		BADPWM	‘0’ = normal operation ‘1’ = PWM outputs are invalid
1	R		I2SERR	‘0’ = normal operation ‘1’ = SAI interface error detected (see *Section 6.14: Configuration register B (addr 0x12)*)
0	R		PLLUL	‘0’ = PLL is locked ‘1’ = PLL is not locked

1. Fault status is set to 1 once the power bridge goes to tri-state mode.

6.3 RESET register (addr 0x02)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SRESET
0	0	0	0	0	0	0	0

Table 17. RESET register

Bit	R/W	RST	Name	Description
0	R/W	0	SRESET	'0': normal operation '1': reset the device

After SRESET is written, the last IC acknowledge is skipped and the EAPD bit (reg 0x16 bit D7) is set to 1 instead of the 0 default value obtained after hardware reset.

6.4 Soft volume register (addr 0x03)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SVOL[1:0]	
0	0	0	0	0	0	0	1

Table 18. Soft volume register

Bit	R/W	RST	Name	Description
1	R/W		SVOL[1:0]	00: 30 ms 01: 100 ms (default) 10: 100 ms 11: Soft-mute disabled
0	R/W			

Values are specified for fs = 48 kHz, 96 kHz or 192 kHz.

6.5 MVOL register (addr 0x04)

D7	D6	D5	D4	D3	D2	D1	D0
MVOL[7:0]							
0	0	0	0	0	0	0	0

Table 19. Master volume register

Bit	R/W	RST	Name	Description
7	R/W	0	MVOL[7:0]	0x00: Hard mute (immediate switchoff) 0x01: Mute 0x02: Mute (PWM on) 0x03: Mute (PWM on) others: volume = [(MVOL-255)/2] dB(1)
6	R/W	0		
5	R/W	0		
4	R/W	0		
3	R/W	0		
2	R/W	0		
1	R/W	0		
0	R/W	0		

1. If the volume is below -60 dB, the level will be approximated to 1 dB step.

6.6 FINEVOL register (addr 0x05)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FINE[1:0]	
0	0	0	0	0	0	0	0

Table 20. Fine volume register

Bit	R/W	RST	Name	Description
1	R/W		FINE[1:0]	00 = 0 dB 01 = -0.125 dB 10 = -0.25 dB 11 = -0.375 dB
0	R/W			

6.7 CH1VOL register (addr 0x06)

D7	D6	D5	D4	D3	D2	D1	D0
CH1VOL[7:0]							
1	0	0	1	1	1	1	1

Table 21. Channel 1 volume register

Bit	R/W	RST	Name	Description
7	R/W	1	CH1VOL[7:0]	0x00: mute others: volume = [(CH1VOL-159)/2] dB(1)
6	R/W	0		
5	R/W	0		
4	R/W	1		
3	R/W	1		
2	R/W	1		
1	R/W	1		
0	R/W	1		

1. If the volume is below -60 dB, the level will be approximated to 1 dB step.

6.8 CH2VOL register (addr 0x07)

D7	D6	D5	D4	D3	D2	D1	D0
CH2VOL[7:0]							
1	0	0	1	1	1	1	1

Table 22. Channel 2 volume register

Bit	R/W	RST	Name	Description
7	R/W	1	CH2VOL[7:0]	0x00: mute others: volume = [(CH2VOL-159)/2] dB(1)
6	R/W	0		
5	R/W	0		
4	R/W	1		
3	R/W	1		
2	R/W	1		
1	R/W	1		
0	R/W	1		

1. If the volume is below -60 dB, the level will be approximated to 1 dB step.

6.9 POST scaler register (addr 0x08)

D7	D6	D5	D4	D3	D2	D1	D0
POST[7:0]							
1	0	0	0	0	0	0	0

Post scaler is set to POST/128 for both CH1 and CH2.

6.10 OPER register (addr 0x09)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OPER[1:0]	
0	0	0	0	0	0	0	0

Table 23. OPER register

Bit	R/W	RST	Name	Description
1	R/W	0	OPER[1:0]	output configuration modes
0	R/W	0		

Table 24. OPER configuration selection

OPER[1:0]	Output configuration	PBTL enable
00	2-channel (full-bridge) power, 2-channel data-out: 1A/1B → 1A/1B 2A/2B → 2A/2B LineOut1 → 3A/3B LineOut2 → 4A/4B Line out configuration determined by LOC register	No
11	2-channel (full-bridge) power, 1-channel FFX: 1A/1B → 1A/1B 2A/2B → 2A/2B 3A/3B → 3A/3B EAPDEXT and TWARNEXT Active	Yes
10	2(half-bridge).1(full-bridge) on-board power: 1A → 1A Binary 0° 2A → 1B Binary 90° 3A/3B → 2A/2B Binary 45° 1A/B → 3A/B Binary 0° 2A/B → 4A/B Binary 90°	No
01	1 channel mono-parallel: 3A → 1A/1B w/ C3BO 45° 3B → 2A/2B w/ C3BO 45° 1A/1B → 3A/3B 2A/2B → 4A/4B CH3 downmixed on all the PWM channels.	No

Figure 16. OPER = 00 (default value)

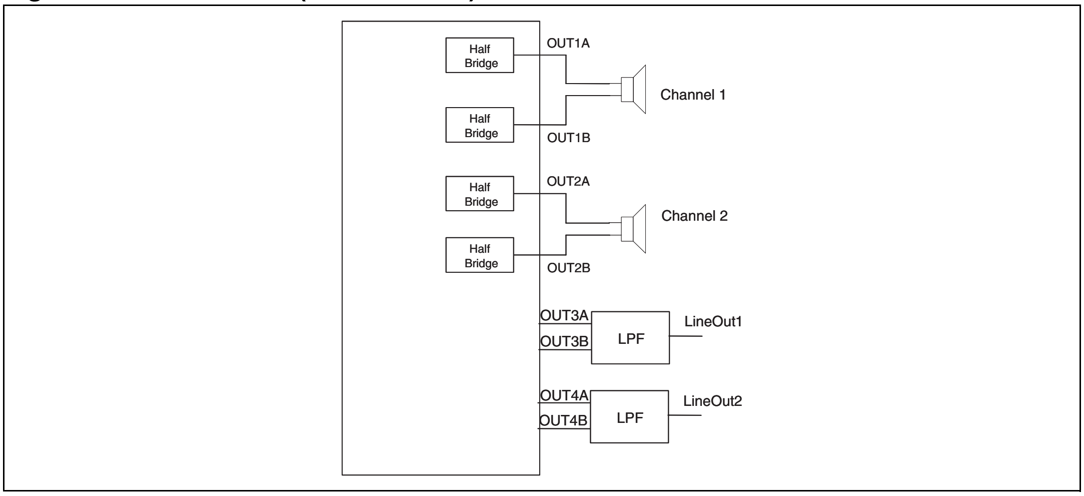


Figure 17. OPER = 11

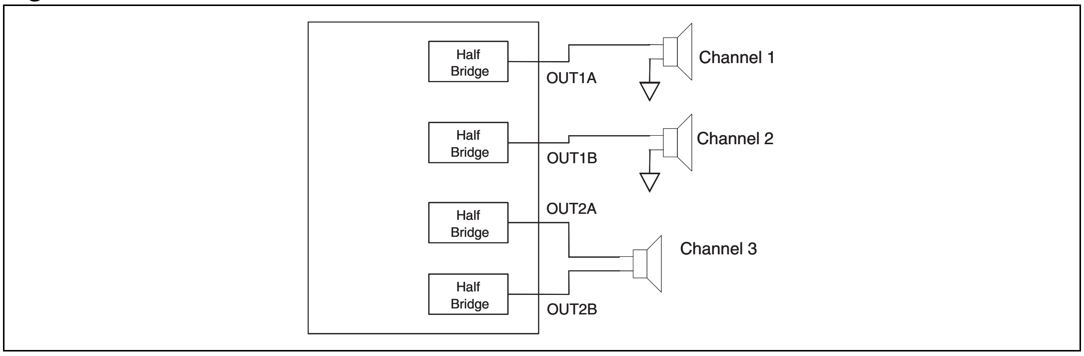


Figure 18. OPER = 10

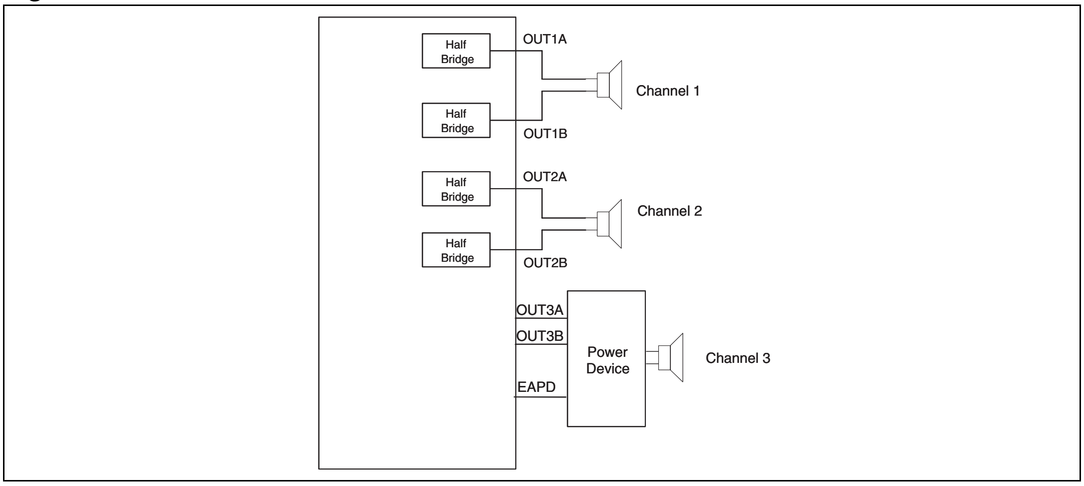
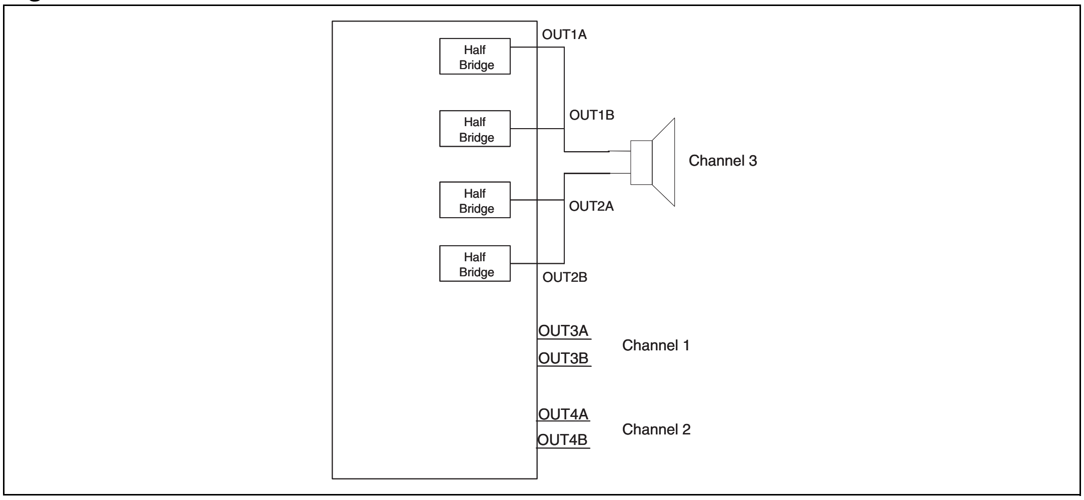
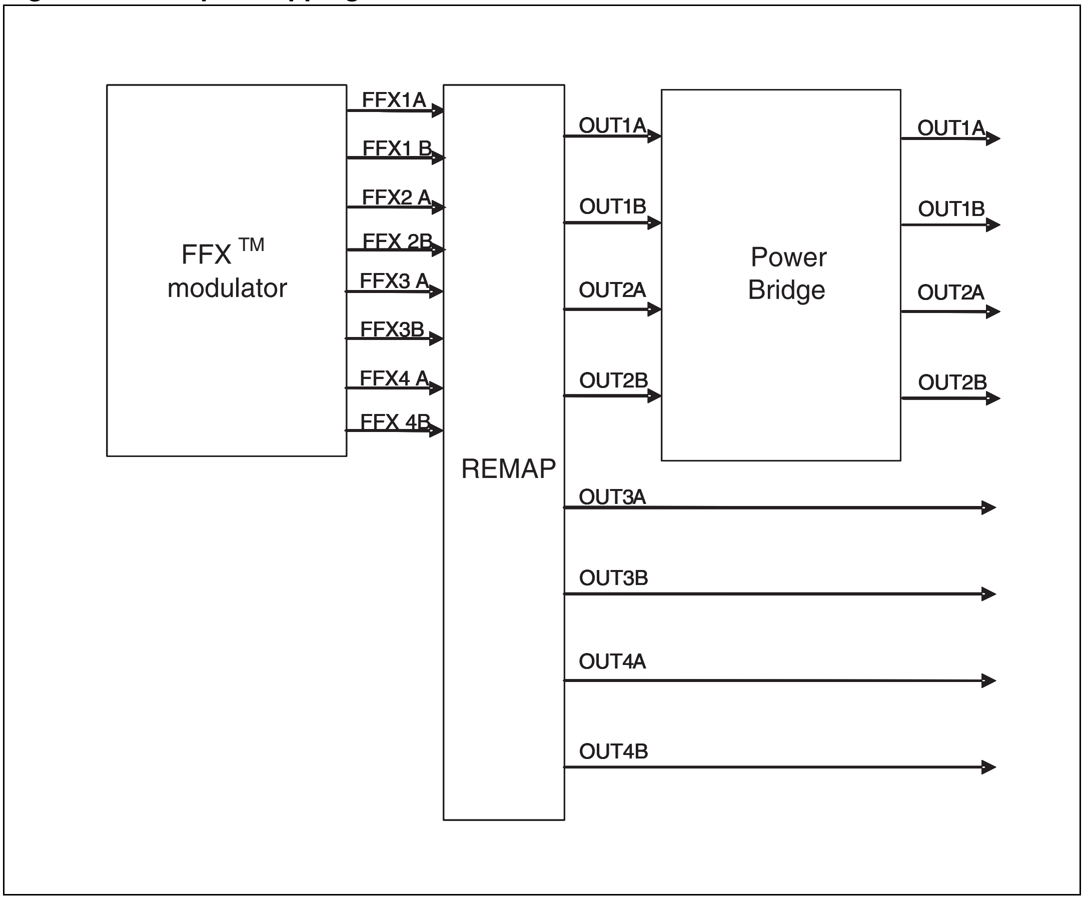


Figure 19. OPER = 01



The STA381BW can be configured to support different output configurations. For each PWM output channel, a PWM slot is defined. A PWM slot is always 1 / (8 * fs) seconds length. The PWM slot defines the maximum extension for the PWM rising and falling edge, that is, the rising edge as well as the falling edge cannot range outside the PWM slot boundaries.

Figure 20. Output mapping scheme



For each configuration the PWM signals from the digital driver are mapped in different ways to the power stage.

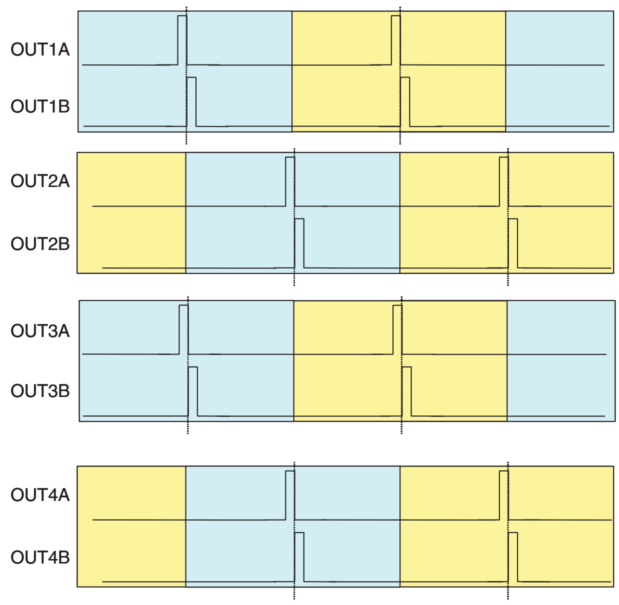
2.0 channels, two full-bridges (OPER = 00)

- FFX1A -> OUT1A
- FFX1B -> OUT1B
- FFX2A -> OUT2A
- FFX2B -> OUT2B
- FFX3A -> OUT3A
- FFX3B -> OUT3B
- FFX4A -> OUT4A
- FFX4B -> OUT4B
- FFX1A/1B configured as ternary
- FFX2A/2B configured as ternary
- FFX3A/3B configured as line out ternary
- FFX4A/4B configured as line out ternary

On channel 3 line out (LOC bits = 00, reg 0x17 bit D7,D6) the same data as channel 1 processing is sent. On channel 4 line out (LOC bits = 00) the same data as channel 2 processing is sent. In this configuration, neither volume control nor EQ has any effect on channels 3 and 4.

In this configuration the PWM slot phase is the following as shown in *Figure 21*.

Figure 21. 2.0 channels (OPER = 00) PWM slots



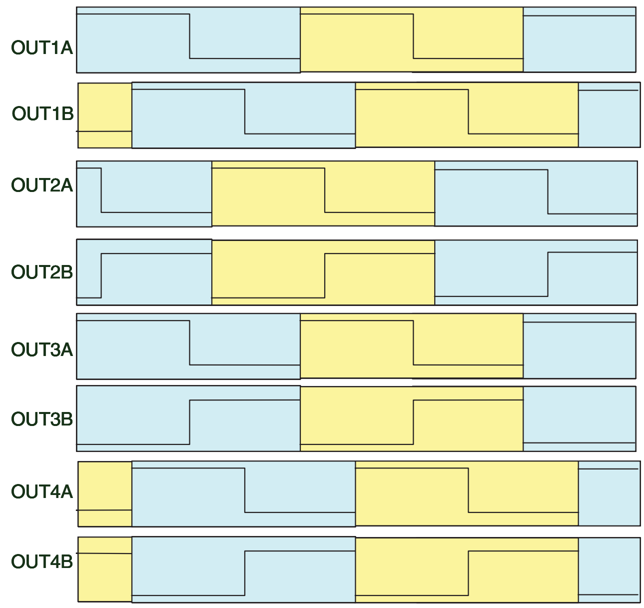
2.1 channels, two half-bridges + one full-bridge (OPER = 11)

- FFX1A -> OUT1A
- FFX2A -> OUT1B
- FFX3A -> OUT2A
- FFX3B -> OUT2B
- FFX1A -> OUT3A
- FFX1B -> OUT3B
- FFX2A -> OUT4A
- FFX2B -> OUT4B
- FFX1A/1B configured as binary
- FFX2A/2B configured as binary
- FFX3A/3B configured as binary
- FFX4A/4B is not used

In this configuration, channel 3 has full control (volume, EQ, etc…). On OUT3/OUT4 channels, channel 1 and channel 2 PWM are replicated.

In this configuration the PWM slot phase is the following as shown in *Figure 22*.

Figure 22. 2.1 channels (OPER = 11) PWM slots



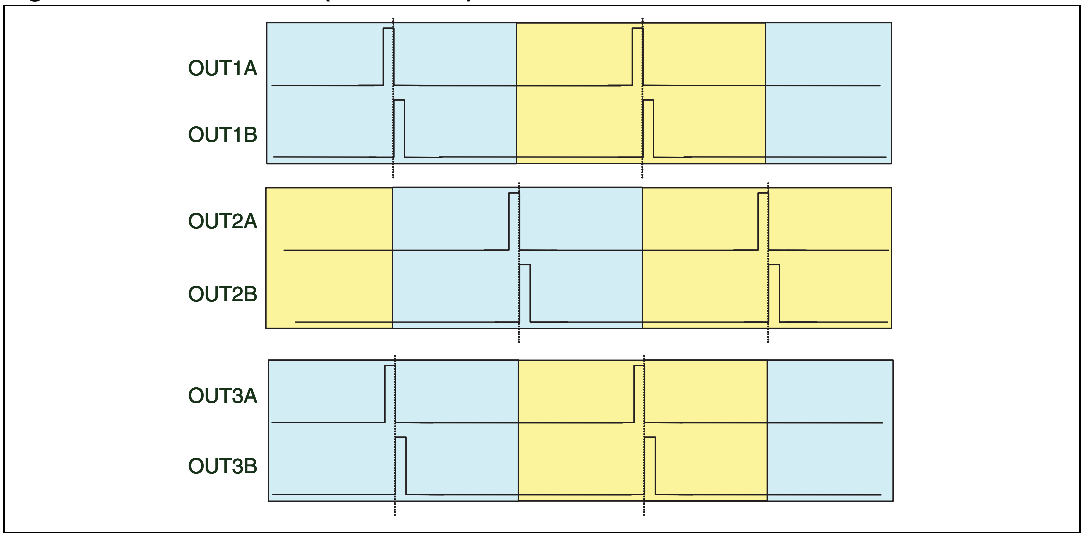
2.1 channels, two full-bridges + one external full-bridge (OPER = 10)

- FFX1A -> OUT1A
- FFX1B -> OUT1B
- FFX2A -> OUT2A
- FFX2B -> OUT2B
- FFX3A -> OUT3A
- FFX3B -> OUT3B
- EAPD -> OUT4A
- TWARN -> OUT4B
- FFX1A/1B configured as ternary
- FFX2A/2B configured as ternary
- FFX3A/3B configured as ternary
- FFX4A/4B is not used

In this configuration, channel 3 has full control (volume, EQ, etc…). On OUT4 channel the external bridge control signals are muxed.

In this configuration the PWM slot phase is the following as shown in *Figure 23*.

Figure 23. 2.1 channels (OPER = 10) PWM slots



6.11 FUNCT register (addr 0x0A)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	CRC	APEQ	PEQ	Reserved	AMDRC	MDRCE	DRC
0	0	1	0	0	0	0	0

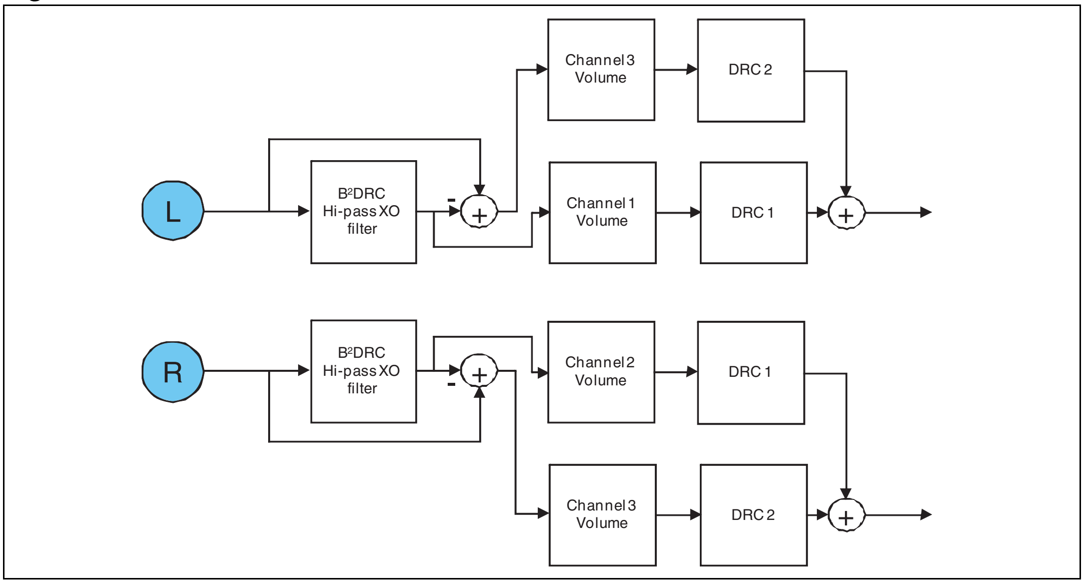
Table 25. FUNCT register

Bit	R/W	RST	Name	Description
6	R/W	0	CRC	‘0’: disable CRC computation and comparison ‘1’: enable CRC computation and comparison
5	R/W	1	APEQ	‘0’: extended BQ disabled, 8th biquadratic filter disabled ‘1’: extended BQ enabled, 8th biquadratic filter enabled
4	R/W	0	PEQ	‘0’: Normal operation ‘1’: PEQ disabled, disables all biquadratic filters
2	R/W	0	AMDRC	‘0’: STCompressor bypassed ‘1’: STCompressor enabled
1	R/W	0	MDRCE	‘0’: MDRCE bypassed ‘1’: MDRCE enabled
0	R/W	0	DRC	‘0’: DRC disabled ‘1’: DRC enabled

6.11.1 Dual-band DRC

The STA381BW device provides a dual-band DRC (B^2DRC) on the left and right channels data path, as depicted in *Figure 24*. Dual-band DRC is activated by setting MDRCE = 1.

Figure 24. B^2DRC scheme



The low-frequency information (LFE) is extracted from the left and right channels, removing the high frequencies using a programmable biquad filter, and then computing the difference with the original signal. Limiter 1 (DRC1) is then used to control the amplitude of the left/right high-frequency components, while limiter 2 (DRC2) is used to control the low-frequency components (see *Section 6.23: Dynamic control registers (addr 0x23 - 0x26 / addr 0x43 - 0x46)*).

The cutoff frequency of the high-pass filters can be user-defined, XO[3:0] = 0, or selected from the pre-defined values.

DRC1 and DRC2 are then used to independently limit L/R high frequencies and LFE channel amplitude (see *Section 6.23: Dynamic control registers (addr 0x23 - 0x26 / addr 0x43 - 0x46)*) as well as their volume control. To be noted that, in this configuration, the dedicated channel 3 volume control can actually act as a bass boost enhancer as well (0.5 dB/step resolution).

The processed LFE channel is then recombined with the L and R channels in order to reconstruct the 2.0 output signal.

Sub-band decomposition

The sub-band decomposition for B^2DRC can be configured specifying the cutoff frequency. The cutoff frequency can be programmed in two ways, using the XO bits in register 0x0C, or using the “user programmable” mode (coefficients stored in RAM addresses 0x28 to 0x31).

For the user-programmable mode, use the formulas below to compute the high-pass filters:

b0 = (1 + alpha) / 2	a0 = 1
b1 = -(1 + alpha) / 2	a1 = -alpha
b2 = 0	a2 = 0

where alpha = (1-sin(ω_0))/cos(ω_0), and ω_0 is the cutoff frequency.

A first-order filter is recommended to guarantee that for every ω_0 the corresponding low-pass filter obtained as difference (as shown in *Figure 24*) will have a symmetric (relative to the HP filter) frequency response, and the corresponding recombination after the DRC has low ripple. Second-order filters can be used as well, but in this case the filter shape must be carefully chosen to provide good low-pass response and minimum ripple recombination. For second-order filters, it is not possible to give a closed formula to get the best coefficients, but empirical adjustment should be done.

DRC settings

The DRC blocks used by B^2DRC are the same as those described in *Section 6.23: Dynamic control registers (addr 0x23 - 0x26 / addr 0x43 - 0x46)*. B^2DRC configure automatically the DRC blocks in anticlipping mode. Attack and release thresholds can be selected using registers 0x32, 0x33, 0x34, 0x35, while attack and release rates are configured by registers 0x12 and 0x14.

Band downmixing

The low-frequency band is down-mixed to the left and right channels at the B^2DRC output. Channel volume can be used to weight the bands recombination to fine-tune the overall frequency response.

6.12 HPCFG register (addr 0x10)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MUTE
0	0	0	0	0	0	0	1

Table 26. HPCFG register

Bit	R/W	RST	Name	Description
0	R/W	1	MUTE	‘0’: HP/Line out is ON ‘1’: HP/LIne out is muted

6.13 Configuration register A (addr 0x11)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	Reserved	Reserved	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	1	1	1

6.13.1 Master clock select

Table 27. Master clock select

Bit	R/W	RST	Name	Description
0	R/W	1	MCS0	Selects the ratio between the input I^2S sampling frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	1	MCS2	

The STA381BW supports sampling rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. Therefore the internal clock is:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin or BICKI pin (depending on the MCS settings) must be a multiple of the input sampling frequency (f_s).

The relationship between the input clock (either XTI or BICKI) and the input sampling rate is determined by both the MCSx and the IR (input rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally. In *Table 28* MCS 111 and 110 indicate that BICKI has to be used as the clock source, while XTI is used in all the other cases.

Table 28. Input sampling rates

Input sampling rate *fs* (kHz)	IR	MCS[2:0]							
		111	110	101	100	011	010	001	000
32, 44.1, 48	00	64*fs(*)	NA	576 * fs	128 * fs	256 * fs	384 * fs	512 * fs	768 * fs
88.2, 96	01	64*fs(*)	32*fs(*)	NA	64 * fs	128 * fs	192 * fs	256 * fs	384 * fs
176.4, 192	1X	64*fs(*)	32*fs(*)	NA	32 * fs	64 * fs	96 * fs	128 * fs	192 * fs

Note: (*): Clock is BICKI

6.13.2 Interpolation ratio selection

Table 29. Internal interpolation ratio

Bit	R/W	RST	Name	Description
4:3	R/W	00	IR [1:0]	Selects internal interpolation ratio based on input I^2S sampling frequency

The STA381BW has variable interpolation (oversampling) settings such that internal processing and FFX output rates remain consistent. The first processing block interpolates by either 3 times (*Table 83: PLL register 0x56 bits* D0), 2 times or 1 time (pass-through) or provides a 2-times downsample. The oversampling ratio of this interpolation is determined by the IR bits.

Table 30. IR bit settings as a function of the input sampling rate

Input sampling rate fs (kHz)	IR	1st stage interpolation ratio
32	00	2-times oversampling
44.1	00	2-times oversampling
48	00	2-times oversampling
88.2	01	Pass-through
96	01	Pass-through
176.4	10	2-times downsampling
192	10	2-times downsampling

6.13.3 Fault-detect recovery bypass

Table 31. Fault-detect recovery bypass

Bit	R/W	RST	Name	Description
7	R/W	0	FDRB	0: fault-detect recovery enabled 1: fault-detect recovery disabled

The on-chip STA381BW power output block provides feedback to the digital controller using inputs to the power control block. The FAULT input is used to indicate a fault condition (either overcurrent or thermal). When FAULT is asserted (set to 0), the power control block attempts a recovery from the fault by asserting the tri-state output (setting it to 0 which directs the power output block to begin recovery), holds it at 0 for period of time in the range of 0.1 ms to 1 second as defined by the fault-detect recovery constant register (FDRC registers 0x3C-0x3D), then toggles it back to 1. This sequence is repeated as long as the fault indication exists. This feature is enabled by default but can be bypassed by setting the FDRB control bit to 1.

6.14 Configuration register B (addr 0x12)

D7	D6	D5	D4	D3	D2	D1	D0
C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
1	0	0	0	0	0	0	0

6.14.1 Serial data interface

The STA381BW audio serial input was designed to interface with standard digital audio components and to accept a number of serial data formats. The STA381BW always acts as the slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data 1 and 2 SDI12.

The SAI bits (D3 to D0) and the SAIFB bit (D4) are used to specify the serial data format. The default serial data format is I^2S, MSB-first. Available formats are shown in the tables that follow.

6.14.2 Serial data first bit

Table 32. Serial data first bit

SAIFB	Format
0	MSB-first
1	LSB-first

Table 33. Support serial audio input formats for MSB-first (SAIFB = 0)

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	0000	0	I^2S 15-bit data
	0001	0	Left/right-justified 16-bit data
48 * fs	0000	0	I^2S 16- to 23-bit data
	0001	0	Left-justified 16- to 24-bit data
	0010	0	Right-justified 24-bit data
	0110	0	Right-justified 20-bit data
	1010	0	Right-justified 18-bit data
	1110	0	Right-justified 16-bit data
64 * fs	0000	0	I^2S 16- to 24-bit data
	0001	0	Left-justified 16- to 24-bit data
	0010	0	Right-justified 24-bit data
	0110	0	Right-justified 20-bit data
	1010	0	Right-justified 18-bit data
	1110	0	Right-justified 16-bit data

Table 34. Supported serial audio input formats for LSB-first (SAIFB = 1)

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	1100	1	I^2S 15-bit data
	1110	1	Left/right-justified 16-bit data
48 * fs	0100	1	I^2S 23-bit data
	0100	1	I^2S 20-bit data
	1000	1	I^2S 18-bit data
	1100	1	LSB first I^2S 16-bit data
	0001	1	Left-justified 24-bit data
	0101	1	Left-justified 20-bit data
	1001	1	Left-justified 18-bit data
	1101	1	Left-justified 16-bit data
	0010	1	Right-justified 24-bit data
	0110	1	Right-justified 20-bit data
	1010	1	Right-justified 18-bit data
	1110	1	Right-justified 16-bit data
64 * fs	0000	1	I^2S 24-bit data
	0100	1	I^2S 20-bit data
	1000	1	I^2S 18-bit data
	1100	1	LSB first I^2S 16-bit data
	0001	1	Left-justified 24-bit data
	0101	1	Left-justified 20-bit data
	1001	1	Left-justified 18-bit data
	1101	1	Left-justified 16-bit data
	0010	1	Right-justified 24-bit data
	0110	1	Right-justified 20-bit data
	1010	1	Right-justified 18-bit data
	1110	1	Right-justified 16-bit data

To make the STA381BW work properly, the serial audio interface LRCKI clock must be synchronous to the PLL output clock. It means that:

- the frequency of PLL clock / frequency of LRCKI = N ±4 cycles, where N depends on the settings in *Table 30*
- the PLL must be locked.

If these two conditions are not met, and the IDE bit (reg 0x05 bit 2) is set to 1, the STA381BW will immediately mute the I^2S PCM data out (provided to the processing block) and it will freeze any active processing task.

To avoid any audio side effects (like pop noise), it is strongly recommended to soft mute any audio streams flowing into the STA381BW data path before the desynchronization event happens. At the same time any processing related to the I^2C configuration should be issued only after the serial audio interface and the internal PLL are synchronous again.

Note: Any mute or volume change causes some delay in the completion of the I^2C operation due to the soft volume feature. The soft volume phase change must be finished before any clock desynchronization.

6.14.3 Delay serial clock enable

Table 35. Delay serial clock enable

Bit	R/W	RST	Name	Description
5	R/W	0	DSCKE	0: No serial clock delay 1: Serial clock delay by 1 core clock cycle to tolerate anomalies in some I^2S master devices

6.14.4 Channel input mapping

Table 36. Channel input mapping

Bit	R/W	RST	Name	Description
6	R/W	0	C1IM	0: Processing channel 1 receives left I^2S input 1: Processing channel 1 receives right I^2S input
7	R/W	1	C2IM	0: Processing channel 2 receives left I^2S input 1: Processing channel 2 receives right I^2S input

Each channel received via I^2S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

6.15 Configuration register C (addr 0x13)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	CSZ3	CSZ2	CSZ1	CSZ0	Reserved	Reserved
1	0	0	1	0	1	1	1

6.15.1 FFX compensating pulse size register

Table 37. FFX compensating pulse size bits

Bit	R/W	RST	Name	Description
2	R/W	1	CSZ0	When OM[1,0] = 11, this register determines the size of the FFX compensating pulse from 0 clock ticks to 15 clock periods.
3	R/W	1	CSZ1	
4	R/W	1	CSZ2	
5	R/W	0	CSZ3	

Table 38. Compensating pulse size

CSZ[3:0]	Compensating pulse size
0000	0 ns (0 ticks) compensating pulse size
0001	20 ns (1 tick) clock period compensating pulse size
…	…
1111	300 ns (15 ticks) clock period compensating pulse size

6.16 Configuration register D (addr 0x14)

D7	D6	D5	D4	D3	D2	D1	D0
SME	ZDE	Reserved	BQL	PSL	DSPB	Reserved	Reserved
0	0	0	1	1	0	0	0

6.16.1 DSP bypass

Table 39. DSP bypass

Bit	R/W	RST	Name	Description
2	R/W	0	DSPB	0: Normal operation 1: Bypass of biquad and bass/treble functions

Setting the DSPB bit bypasses the EQ function of the STA381BW.

6.16.2 Post-scale link

Table 40. Post-scale link

Bit	R/W	RST	Name	Description
3	R/W	1	PSL	0: Each channel uses individual post-scale values 1: Each channel uses channel 1 post-scale values

Post-scale functionality can be used for power-supply error correction. For multi-channel applications running off the same power supply, the post-scale values can be linked to the value of channel 1 for ease of use and in order to update the values faster.

6.16.3 Biquad coefficient link

Table 41. Biquad coefficient link

Bit	R/W	RST	Name	Description
4	R/W	1	BQL	0: Each channel uses coefficient values 1: Each channel uses channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the channel 1 coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

6.16.4 Zero-detect mute enable

Table 42. Zero-detect mute enable

Bit	R/W	RST	Name	Description
6	R/W	0	ZDE	Setting of 1 enables the automatic zero-detect mute Setting of 0 disables the automatic zero-detect mute

Refer to *6.32: Enhanced zero-detect mute and input level measurement (address 0x61-0x65, 0x3F, 0x40, 0x6F)*.

6.16.5 Submix mode enable

Table 43. Submix mode enable

Bit	R/W	RST	Name	Description
7	R/W	0	SME	0: Submix into left/right disabled 1: Submix into left/right enabled

6.17 Configuration register E (addr 0x15)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	ZCE	Reserved	PWMS	AME	NSBW	Reserved	Reserved
1	0	0	0	0	0	1	0

6.17.1 Noise-shaper bandwidth selection

Table 44. Noise-shaper bandwidth selection

Bit	R/W	RST	Name	Description
2	R/W	0	NSBW	1: Third order NS 0: Fourth order NS

6.17.2 AM mode enable

Table 45. AM mode enable

Bit	R/W	RST	Name	Description
3	R/W	0	AME	0: Normal FFX operation 1: AM reduction mode FFX operation

The STA381BW features an FFX processing mode that minimizes the amount of noise generated in the frequency range of AM radio. This mode is intended for use when FFX is operating in a device with an active AM tuner. The SNR of the FFX processing is reduced to approximately 83 dB in this mode, which is still greater than the SNR of AM radio.

6.17.3 PWM speed mode

Table 46. PWM speed mode

Bit	R/W	RST	Name	Description
4	R/W	0	PWMS	0: Normal speed (384 kHz) all channels 1: Odd speed (341.3 kHz) all channels. Not suitable for binary BTL mode.

6.17.4 Zero-crossing enable

Table 47. Zero-crossing enable

Bit	R/W	RST	Name	Description
6	R/W	0	ZCE	‘1’: Volume adjustment only occurs at digital zero-crossing ‘0’: Volume adjustment occur immediately

The ZCE bit enables zero-crossing adjustment. When volume is adjusted on digital zero-crossing, no clicks are audible

6.18 Configuration register F (addr 0x16)

D7	D6	D5	D4	D3	D2	D1	D0
EAPD	PWDN	Reserved	LDTE	BCLE	IDE	Reserved	Reserved
0	1	0	1	1	1		

6.18.1 Invalid input detect mute enable

Table 48. Invalid input detect mute enable

Bit	R/W	RST	Name	Description
2	R/W	1	IDE	Setting of 1 enables the automatic invalid input detect mute

Setting the IDE bit enables this function, which looks at the input I^2S data and automatically mutes if the signals are perceived as invalid.

6.18.2 Binary output mode clock loss detection

Table 49. Binary output mode clock loss detection

Bit	R/W	RST	Name	Description
3	R/W	1	BCLE	Binary output mode clock loss detection enable

This bit detects loss of input MCLK in binary mode and will output 50% duty cycle.

6.18.3 LRCK double trigger protection

Table 50. LRCK double trigger protection

Bit	R/W	RST	Name	Description
4	R/W	1	LDTE	LRCLK double trigger protection enable

This bit actively prevents double triggering of LRCLK.

6.18.4 Power-down

Table 51. IC power-down

Bit	R/W	RST	Name	Description
7	R/W	1	PWDN	0: IC power-down low-power condition 1: IC normal operation

The PWDN register is used to place the IC in a low-power state. When PWDN is written as 0, the output begins a soft-mute. After the mute condition is reached, EAPD is asserted to power down the power stage, then the master clock to all internal hardware except the I^2C block is gated. This places the IC in a very low power consumption state.The register state is preserved once the device recovers from power-down.

6.18.5 External amplifier power-down

Table 52. External amplifier power-down

Bit	R/W	RST	Name	Description
7	R/W	0	EAPD	0: External power stage power-down active 1: Normal operation

The EAPD register directly disables/enables the internal power circuitry.

When EAPD = 0, the internal power section is placed in a low-power state (disabled). This register also controls the EAPD/FFX4B output pin when OCFG = 11.

6.19 Volume control registers (addr 0x17 - 0x1B)

6.19.1 Mute/line output configuration register (addr 0x17)

D7	D6	D5	D4	D3	D2	D1	D0
LOC1	LOC0	Reserved	Reserved	C3M	C2M	C1M	MMUTE
0	0	0	0	0	0	0	0

Table 53. Line output configuration

LOC[1:0]	Line output configuration
00	Line output fixed - no volume, no EQ
01	Line output variable - CH3 volume effects line output, no EQ
10	Line output variable with EQ - CH3 volume effects line output
11	Reserved

Line output is only active when OCFG = 00. In this case LOC determines the line output configuration. The source of the line output is always the channel 1 and 2 inputs.

Table 54. Mute configuration

Bit	R/W	RST	Name	Description
3	R/W	0	C3M	Channel 3 mute 0 - No mute condition. It is possible to set the channel volume 1 - Channel 3 in hardware mute
2	R/W	0	C2M	Channel 2 mute 0 - No mute condition. It is possible to set the channel volume 1 - Channel 2 in hardware mute
1	R/W	0	C1M	Channel 1 mute 0 - No mute condition. It is possible to set the channel volume 1 - Channel 1 in hardware mute
0	R/W	0	MMUTE	Master mute 0 - Normal operation 1 - All channels are in mute condition

6.19.2 Channel 3 / line output volume (addr 0x1B)

D7	D6	D5	D4	D3	D2	D1	D0
CH3VOL							
0	1	1	0	0	0	0	0

The volume structure of the STA381BW consists of individual volume registers for each channel and a master volume register that provides an offset to each channel's volume setting. The individual channel volumes are adjustable in 0.5 dB steps from +48 dB to -80 dB.

As an example, if CH3VOL = 0x00 or +48 dB and MVOL= -12 dB, then the total gain for channel 3 = +36 dB.

The master mute, when set to 1, mutes all channels at once, whereas the individual channel mute (CxM) mutes only that channel. Both the master mute and the channel mutes provide a “soft mute” with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate (approximately 96 kHz).

A “hard (instantaneous) mute” can be obtained by programming a value of 0xFF (255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register, any channel whose total volume is less than -80 dB is muted.

All changes in volume take place at zero-crossings when ZCE = 1 (*Section 6.17: Configuration register E (addr 0x15)*) on a per-channel basis as this creates the smoothest possible volume transitions. When ZCE = 0, volume updates occur immediately.

Table 55. Channel 3 volume as a function of CH3VOL[7:0]

CH3VOL[7:0]	Volume
00000000 (0x00)	+48 dB
00000001 (0x01)	+47.5 dB
00000010 (0x02)	+47 dB
...	...
01011111 (0x5F)	+0.5 dB
01100000 (0x60)	0 dB
01100001 (0x61)	-0.5 dB
...	...
11010111 (0xD7)	-59.5 dB
11011000 (0xD8)	-60 dB
11011001 (0xD9)	-61 dB
11011010 (0xDA)	-62 dB
...	...
11101100 (0xEC)	-80 dB
11101101 (0xED)	Hard channel mute
...	...
11111111 (0xFF)	Hard channel mute

6.20 Audio preset registers (0x1D)

D7	D6	D5	D4	D3	D2	D1	D0
XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0	0	0	0	0	0	0	0

6.20.1 AM interference frequency switching

Table 56. AM interference frequency switching bits

Bit	R/W	RST	Name	Description
0	R/W	0	AMAME	Audio preset AM enable 0: switching frequency determined by PWMS setting 1: switching frequency determined by AMAM settings

Table 57. Audio preset AM switching frequency selection

AMAM[2:0]	48 kHz/96 kHz input fs	44.1 kHz/88.2 kHz input fs
000	0.535 MHz - 0.720 MHz	0.535 MHz - 0.670 MHz
001	0.721 MHz - 0.900 MHz	0.671 MHz - 0.800 MHz
010	0.901 MHz - 1.100 MHz	0.801 MHz - 1.000 MHz
011	1.101 MHz - 1.300 MHz	1.001 MHz - 1.180 MHz
100	1.301 MHz - 1.480 MHz	1.181 MHz - 1.340 MHz
101	1.481 MHz - 1.600 MHz	1.341 MHz - 1.500 MHz
110	1.601 MHz - 1.700 MHz	1.501 MHz - 1.700 MHz

6.20.2 Bass management crossover

Table 58. Bass management crossover

Bit	R/W	RST	Name	Description
4	R/W	0	XO0	Selects the bass management crossover frequency. A 1st-order high-pass filter (channels 1 and 2) or a 2nd-order low-pass filter (channel 3) at the selected frequency is performed.
5	R/W	0	XO1	
6	R/W	0	XO2	
7	R/W	0	XO3	

Table 59. Bass management crossover frequency

XO[3:0]	Crossover frequency
0000	*Table 73.: RAM block for biquads, mixing, scaling and bass management*
0001	80 Hz
0010	100 Hz
0011	120 Hz
0100	140 Hz
0101	160 Hz
0110	180 Hz
0111	200 Hz
1000	220 Hz
1001	240 Hz
1010	260 Hz
1011	280 Hz
1100	300 Hz
1101	320 Hz
1110	340 Hz
1111	360 Hz

6.21 Channel configuration registers (addr 0x1F - 0x21)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	C1BO	C1VPB	C1EQBP	C1TCB
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	C2BO	C2VPB	C2EQBP	C2TCB
0	1	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VPB	Reserved	Reserved
1	0	0	0	0	0	0	0

6.21.1 Tone control bypass

Tone control (bass/treble) can be bypassed on a per-channel basis for channels 1 and 2.

Table 60. Tone control bypass

CxTCB	Mode
0	Perform tone control on channel x - normal operation
1	Bypass tone control on channel x

6.21.2 EQ bypass

EQ control can be bypassed on a per-channel basis for channels 1 and 2. If EQ control is bypassed on a given channel, the prescale and all filters (biquads, bass, treble in any combination) are bypassed for that channel.

Table 61. EQ bypass

CxEQBP	Mode
0	Perform EQ on channel x - normal operation
1	Bypass EQ on channel x

6.21.3 Volume bypass

Each channel contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register, then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel.

Table 62. Volume bypass register

CxVBP	Mode
0	Normal volume operations
1	Volume is bypassed

6.21.4 Binary output enable registers

Each individual channel output can be set to output a binary PWM stream. In this mode output A of a channel is considered the positive output and output B is the negative inverse.

Table 63. Binary output enable registers

CxBO	Mode
0	FFX 3-state output - normal operation
1	Binary output

6.21.5 Limiter select

Limiter selection can be made on a per-channel basis according to the channel limiter select bits. CxLS bits are not considered in case of dual-band DRC (*Section 6.11.1: Dual-band DRC*), EQ DRC (*Section 6.26.1: Extended post-scale range*) usage.

Table 64. Channel limiter mapping as a function of C3LS bits

C3LS[1:0]	Channel limiter mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2

6.21.6 Output mapping

Output mapping can be performed on a per-channel basis according to the CxOM channel output mapping bits. Each input into the output configuration engine can receive data from any of the three processing channel outputs.

Table 65. Channel output mapping as a function of C3OM bits

C3OM[1:0]	Channel x output source from
00	Channel1
01	Channel 2
10	Channel 3

6.22 Tone control register (addr 0x22)

D7	D6	D5	D4	D3	D2	D1	D0
TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0	1	1	1	0	1	1	1

6.22.1 Tone control

Table 66. Tone control boost/cut as a function of BTC and TTC bits

BTC[3:0]/TTC[3:0]	Boost/cut
0000	-12 dB
0001	-12 dB
…	…
0111	-4 dB
0110	-2 dB
0111	0 dB
1000	+2 dB
1001	+4 dB
…	…
1101	+12 dB
1110	+12 dB
1111	+12 dB

6.23 Dynamic control registers (addr 0x23 - 0x26 / addr 0x43 - 0x46)

6.23.1 Limiter 1 attack/release rate (L1AR addr 0x23)

D7	D6	D5	D4	D3	D2	D1	D0
L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0	1	1	0	1	0	1	0

6.23.2 Limiter 1 attack/release threshold (L1ATRT addr 0x24)

D7	D6	D5	D4	D3	D2	D1	D0
L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0	1	1	0	1	0	0	1

6.23.3 Limiter 2 attack/release rate (L2AR addr 0x25)

D7	D6	D5	D4	D3	D2	D1	D0
L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0	1	1	0	1	0	1	0

6.23.4 Limiter 2 attack/release threshold (L2 ATRT addr 0x26)

D7	D6	D5	D4	D3	D2	D1	D0
L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0	1	1	0	1	0	0	1

The STA381BW includes two independent limiter blocks. The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anticlipping mode or to actively reduce the dynamic range for a better listening environment such as a nighttime listening mode which is often needed for DVDs. The two modes are selected via the DRC bit in *Section 6.11: FUNCT register (addr 0x0A)*. Each channel can be mapped to either limiter or not mapped, meaning that the channel will clip when 0 dBfs is exceeded. Each limiter looks at the present value of each channel that is mapped to it, selects the maximum absolute value of all these channels, performs the limiting algorithm on that value, and then, if needed, adjusts the gain of the mapped channels in unison.

The limiter attack thresholds are determined by the LxAT registers if the EATHx[7] (bit D7 of register 0x43 or 0x45) bits are set to 0, else the thresholds are determined by EATHx[6:0]. It is recommended in anticlipping mode to set this to 0 dBfs, which corresponds to the maximum unclipped output power of an FFX amplifier. Since gain can be added digitally within the STA381BW it is possible to exceed 0 dBfs or any other LxAT setting. When this occurs, the limiter, when active, automatically starts reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. Gain reduction occurs on a peak-detect algorithm. Setting the EATHx[7] bits to 1 selects the anticlipping mode.

The limiter release thresholds are determined by the LxRT registers if the ERTHx[7] (bit D7 of register 0x44 or 0x46) bits are set to 0, else the thresholds are determined by

ERTHx[6:0]. Setting the ERTHx[7] bits to 1 automatically selects the anticlipping mode. The release of the limiter, when the gain is again increased, is dependent on an RMS-detect algorithm. The output of the volume/limiter block is passed through an RMS filter. The output of this filter is compared to the release threshold, determined by the release threshold register. When the RMS filter output falls below the release threshold, the gain is again increased at a rate dependent upon the release rate register. The gain can never be increased past its set value and, therefore, the release only occurs if the limiter has already reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range, this is helpful as overlimiting can reduce the dynamic range to virtually zero and cause program material to sound “lifeless”.

In anticlipping mode, the attack and release thresholds are set relative to full-scale. In DRC mode (bit D0 reg 0x0A set to 1), the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

Figure 25. Basic limiter and volume flow diagram

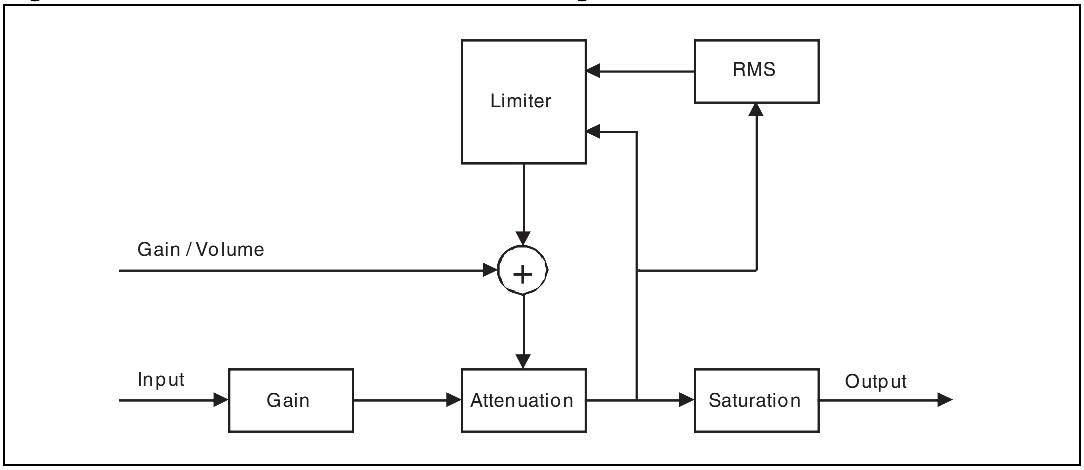


Table 67. Limiter attack rate as a function of LxA bits

LxA[3:0]	Attack rate dB/ms	
0000	3.1584	Fast
0001	2.7072	
0010	2.2560	
0011	1.8048	
0100	1.3536	
0101	0.9024	
0110	0.4512	
0111	0.2256	
1000	0.1504	
1001	0.1123	
1010	0.0902	
1011	0.0752	
1100	0.0645	
1101	0.0564	
1110	0.0501	
1111	0.0451	Slow

Table 68. Limiter release rate as a function of LxR bits

LxR[3:0]	Release rate dB/ms	
0000	0.5116	Fast
0001	0.1370	
0010	0.0744	
0011	0.0499	
0100	0.0360	
0101	0.0299	
0110	0.0264	
0111	0.0208	
1000	0.0198	
1001	0.0172	
1010	0.0147	
1011	0.0137	
1100	0.0134	
1101	0.0117	
1110	0.0110	
1111	0.0104	Slow

Anticlipping mode

Table 69. Limiter attack threshold as a function of LxAT bits (AC mode)

LxAT[3:0]	AC (dB relative to fs)
0000	-12
0001	-10
0010	-8
0011	-6
0100	-4
0101	-2
0110	0
0111	+2
1000	+3
1001	+4
1010	+5
1011	+6
1100	+7
1101	+8
1110	+9
1111	+10

Table 70. Limiter release threshold as a function of LxRT bits (AC mode)

LxRT[3:0]	AC (dB relative to fs)
0000	-∞
0001	-29 dB
0010	-20 dB
0011	-16 dB
0100	-14 dB
0101	-12 dB
0110	-10 dB
0111	-8 dB
1000	-7 dB
1001	-6 dB
1010	-5 dB
1011	-4 dB
1100	-3 dB
1101	-2 dB
1110	-1 dB
1111	-0 dB

Dynamic range compression mode

Table 71. Limiter attack threshold as a function of LxAT bits (DRC mode)

LxAT[3:0]	DRC (dB relative to volume)
0000	-31
0001	-29
0010	-27
0011	-25
0100	-23
0101	-21
0110	-19
0111	-17
1000	-16
1001	-15
1010	-14
1011	-13
1100	-12
1101	-10
1110	-7
1111	-4

Table 72. Limiter release threshold as a function of LxRT bits (DRC mode)

LxRT[3:0]	DRC (dB relative to volume + LxAT)
0000	-∞
0001	-38 dB
0010	-36 dB
0011	-33 dB
0100	-31 dB
0101	-30 dB
0110	-28 dB
0111	-26 dB
1000	-24 dB
1001	-22 dB
1010	-20 dB
1011	-18 dB
1100	-15 dB
1101	-12 dB
1110	-9 dB
1111	-6 dB

6.23.5 Limiter 1 extended attack threshold (addr 0x43)

D7	D6	D5	D4	D3	D2	D1	D0
EATHEN1	EATH1[6]	EATH1[5]	EATH1[4]	EATH1[3]	EATH1[2]	EATH1[1]	EATH1[0]
0	0	1	1	0	0	0	0

The extended attack threshold value is determined as follows:

attack threshold = -12 + EATH1 / 4

To enable this feature, the EATHEN1 bit must be set to 1.

6.23.6 Limiter 1 extended release threshold (addr 0x44)

D7	D6	D5	D4	D3	D2	D1	D0
ERTHEN1	ERTH1[6]	ERTH1[5]	ERTH1[4]	ERTH1[3]	ERTH1[2]	ERTH1[1]	ERTH1[0]
0	0	1	1	0	0	0	0

The extended release threshold value is determined as follows:

release threshold = -12 + ERTH1 / 4

To enable this feature, the ERTHEN1 bit must be set to 1.

6.23.7 Limiter 2 extended attack threshold (addr 0x45)

D7	D6	D5	D4	D3	D2	D1	D0
EATHEN2	EATH2[6]	EATH2[5]	EATH2[4]	EATH2[3]	EATH2[2]	EATH2[1]	EATH2[0]
0	0	1	1	0	0	0	0

The extended attack threshold value is determined as follows:

attack threshold = -12 + EATH2 / 4

To enable this feature, the EATHEN2 bit must be set to 1.

6.23.8 Limiter 2 extended release threshold (addr 0x46)

D7	D6	D5	D4	D3	D2	D1	D0
ERTHEN2	ERTH2[6]	ERTH2[5]	ERTH2[4]	ERTH2[3]	ERTH2[2]	ERTH2[1]	ERTH2[0]
0	0	1	1	0	0	0	0

The extended release threshold value is determined as follows:

release threshold = -12 + ERTH2 / 4

To enable this feature, the ERTHEN2 bit must be set to 1.

Note: Attack/release threshold step is 0.125 dB in the range -12 dB to 0 dB.

6.24 User-defined coefficient control registers (addr 0x27 - 0x37)

6.24.1 Coefficient address register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0	0	0	0	0	0	0	0

6.24.2 Coefficient b1 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

6.24.3 Coefficient b1 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0	0	0	0	0	0	0	0

6.24.4 Coefficient b1 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0	0	0	0	0	0	0	0

6.24.5 Coefficient b2 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0	0	0	0	0	0	0	0

6.24.6 Coefficient b2 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0	0	0	0	0	0	0	0

6.24.7 Coefficient b2 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0	0	0	0	0	0	0	0

6.24.8 Coefficient a1 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

6.24.9 Coefficient a1 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0	0	0	0	0	0	0	0

6.24.10 Coefficient a1 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0	0	0	0	0	0	0	0

6.24.11 Coefficient a2 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0	0	0	0	0	0	0	0

6.24.12 Coefficient a2 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0	0	0	0	0	0	0	0

6.24.13 Coefficient a2 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0	0	0	0	0	0	0	0

6.24.14 Coefficient b0 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0	0	0	0	0	0	0	0

6.24.15 Coefficient b0 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0	0	0	0	0	0	0	0

6.24.16 Coefficient b0 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0	0	0	0	0	0	0	0

6.24.17 Coefficient write/read control register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				RA	R1	WA	W1
0				0	0	0	0

Coefficients for user-defined EQ, mixing, scaling, and bass management are handled internally in the STA381BW via RAM. Access to this RAM is available to the user via an I^2C register interface. A collection of I^2C registers is dedicated to this function. One contains a coefficient base address, five sets of three store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the write/read of the coefficient(s) to/from RAM.

Note: The read and write operation on RAM coefficients works only if the LRCKI pin is switching.

Reading a coefficient from RAM

1. Write 6 bits of the address to I^2C register 0x27.
2. Write 1 to the R1 bit in I^2C address 0x37.
3. Read the top 8 bits of the coefficient in I^2C address 0x28.
4. Read the middle 8 bits of the coefficient in I^2C address 0x29.
5. Read the bottom 8 bits of the coefficient in I^2C address 0x2A.

Reading a set of coefficients from RAM

1. Write 6 bits of the address to I^2C register 0x27.
2. Write 1 to the RA bit in I^2C address 0x37.
3. Read the top 8 bits of the coefficient in I^2C address 0x28.
4. Read the middle 8 bits of the coefficient in I^2C address 0x29.
5. Read the bottom 8 bits of the coefficient in I^2C address 0x2A.
6. Read the top 8 bits of coefficient b2 in I^2C address 0x2B.
7. Read the middle 8 bits of coefficient b2 in I^2C address 0x2C.
8. Read the bottom 8 bits of coefficient b2 in I^2C address 0x2D.
9. Read the top 8 bits of coefficient a1 in I^2C address 0x2E.
10. Read the middle 8 bits of coefficient a1 in I^2C address 0x2F.
11. Read the bottom 8 bits of coefficient a1 in I^2C address 0x30.
12. Read the top 8 bits of coefficient a2 in I^2C address 0x31.
13. Read the middle 8 bits of coefficient a2 in I^2C address 0x32.
14. Read the bottom 8 bits of coefficient a2 in I^2C address 0x33.
15. Read the top 8 bits of coefficient b0 in I^2C address 0x34.
16. Read the middle 8 bits of coefficient b0 in I^2C address 0x35.
17. Read the bottom 8 bits of coefficient b0 in I^2C address 0x36.

Writing a single coefficient to RAM

1. Write 6 bits of the address to I^2C register 0x27.
2. Write the top 8 bits of the coefficient in I^2C address 0x28.
3. Write the middle 8 bits of the coefficient in I^2C address 0x29.
4. Write the bottom 8 bits of the coefficient in I^2C address 0x2A.
5. Write 1 to the W1 bit in I^2C address 0x37.

Writing a set of coefficients to RAM

1. Write 6 bits of the starting address to I^2C register 0x27.
2. Write the top 8 bits of coefficient b1 in I^2C address 0x28.
3. Write the middle 8 bits of coefficient b1 in I^2C address 0x29.
4. Write the bottom 8 bits of coefficient b1 in I^2C address 0x2A.
5. Write the top 8 bits of coefficient b2 in I^2C address 0x2B.
6. Write the middle 8 bits of coefficient b2 in I^2C address 0x2C.
7. Write the bottom 8 bits of coefficient b2 in I^2C address 0x2D.
8. Write the top 8 bits of coefficient a1 in I^2C address 0x2E.
9. Write the middle 8 bits of coefficient a1 in I^2C address 0x2F.
10. Write the bottom 8 bits of coefficient a1 in I^2C address 0x30.
11. Write the top 8 bits of coefficient a2 in I^2C address 0x31.
12. Write the middle 8 bits of coefficient a2 in I^2C address 0x32.
13. Write the bottom 8 bits of coefficient a2 in I^2C address 0x33.
14. Write the top 8 bits of coefficient b0 in I^2C address 0x34.
15. Write the middle 8 bits of coefficient b0 in I^2C address 0x35.
16. Write the bottom 8 bits of coefficient b0 in I^2C address 0x36.
17. Write 1 to the WA bit in I^2C address 0x37.

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side effects. When using this technique, the 6-bit address specifies the address of the biquad b1 coefficient (for example, 0, 5, 10, 20, 35 decimal), and the STA381BW generates the RAM addresses as offsets from this base value to write the complete set of coefficient data.

6.24.18 User-defined EQ

The STA381BW can be programmed for four EQ filters (biquads) per each of the two input channels. The biquads use the following equation:

$$Y[n] = 2 * (b_0 / 2) * X[n] + 2 * (b_1 / 2) * X[n-1] + b_2 * X[n-2] - 2 * (a_1 / 2) * Y[n-1] - a_2 * Y[n-2]$$
$$= b_0 * X[n] + b_1 * X[n-1] + b_2 * X[n-2] - a_1 * Y[n-1] - a_2 * Y[n-2]$$

where Y[n] represents the output and X[n] represents the input. Multipliers are 24-bit signed fractional multipliers, with coefficient values in the range of 0x800000 (-1) to 0x7FFFFF (0.9999998808).

Coefficients stored in the user-defined coefficient RAM are referenced in the following manner:

CxHy0 = $b_1 / 2$

CxHy1 = b_2

CxHy2 = $-a_1 / 2$

CxHy3 = $-a_2$

CxHy4 = $b_0 / 2$

where x represents the channel and the y the biquad number. For example, C2H41 is the b_2 coefficient in the fourth biquad for channel 2.

Additionally, the STA381BW can be programmed for a high-pass filter (processing channels 1 and 2) and a low-pass filter (processing channel 3) to be used for bass-management crossover when the XO setting is 000 (user-defined). Both of these filters when defined by the user (rather than using the preset crossover filters) are second order filters that use the biquad equation given above. They are loaded into the C12H0-4 and C3Hy0-4 areas of RAM noted in *Table 73*.

Channel 1 and channel 2 biquads use by default the extended coefficient range (-4, +4); Xover filters use only the standard coefficients range (-1, +1).

By default, all user-defined filters are pass-through where all coefficients are set to 0, except the channel 1 and 2 $b_0/2$ coefficient which is set to 0x100000 (representing 0.5) and Xover $b_0/2$ coefficient which is set to 0x400000 (representing 0.5).

6.24.19 Pre-scale

The STA381BW provides a multiplication for each input channel for the purpose of scaling the input prior to EQ. This pre-EQ scaling is accomplished by using a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. The scale factor for this multiplication is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass management. All channels can use the channel-1 pre-scale factor by setting the biquad link bit. By default, all pre-scale factors are set to 0x7FFFFF.

6.24.20 Post-scale

The STA381BW provides one additional multiplication after the last interpolation stage and the distortion compensation on each channel. This post-scaling is accomplished by using a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. The scale factor for this multiplication is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass management. This post-scale factor can be used in conjunction with an ADC-equipped microcontroller to perform power-supply error correction. All channels can use the channel-1 post-scale factor by setting the post-scale link bit. By default, all post-scale factors are set to 0x7FFFFF. When line output is being used, channel-3 post-scale will affect both channels 3 and 4.

Table 73. RAM block for biquads, mixing, scaling and bass management

Index (decimal)	Index (hex)	Description	Coefficient	Default
0	0x00	Channel 1 - Biquad 1	C1H10(b1/2)	0x000000
1	0x01		C1H11(b2)	0x000000
2	0x02		C1H12(a1/2)	0x000000
3	0x03		C1H13(a2)	0x000000
4	0x04		C1H14(b0/2)	0x100000
5	0x05	Channel 1 - Biquad 2	C1H20	0x000000
…	…	…	…	…
19	0x13	Channel 1 - Biquad 4	C1H44	0x100000
20	0x14	Channel 2 - Biquad 1	C2H10	0x000000
21	0x15		C2H11	0x000000
…	…	…	…	…
39	0x27	Channel 2 - Biquad 4	C2H44	0x100000
40	0x28	Channel 1/2 - Biquad 5 for XO = 000 High-pass 2nd order filter for XO≠000	C12H0(b1/2)	0x000000
41	0x29		C12H1(b2)	0x000000
42	0x2A		C12H2(a1/2)	0x000000
43	0x2B		C12H3(a2)	0x000000
44	0x2C		C12H4(b0/2)	0x400000
45	0x2D	Channel 3 - Biquad for XO = 000 Low-pass 2nd order filter for XO≠000	C3H0(b1/2)	0x000000
46	0x2E		C3H1(b2)	0x000000
47	0x2F		C3H2(a1/2)	0x000000
48	0x30		C3H3(a2)	0x000000
49	0x31		C3H4(b0/2)	0x400000
50	0x32	Channel 1 - Pre-Scale	C1PreS	0x7FFFFF
51	0x33	Channel 2 - Pre-Scale	C2PreS	0x7FFFFF
52	0x34	Channel 1 - Post-Scale	C1PstS	0x7FFFFF
53	0x35	Channel 2 - Post-Scale	C2PstS	0x7FFFFF
54	0x36	Channel 3 - Post-Scale	C3PstS	0x7FFFFF
55	0x37	Reserved	reserved	0x5A9DF7
56	0x38	Channel 1 - Mix 1	C1MX1	0x7FFFFF
57	0x39	Channel 1 - Mix 2	C1MX2	0x000000
58	0x3A	Channel 2 - Mix 1	C2MX1	0x000000
59	0x3B	Channel 2 - Mix 2	C2MX2	0x7FFFFF
60	0x3C	Channel 3 - Mix 1	C3MX1	0x400000
61	0x3D	Channel 3 - Mix 2	C3MX2	0x400000
62	0x3E	UNUSED		
63	0x3F	UNUSED		

6.25 Fault-detect recovery constant registers (addr 0x3C - 0x3D)

D7	D6	D5	D4	D3	D2	D1	D0
FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0	0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0	0	0	0	1	1	0	0

The FDRC bits specify the 16-bit fault-detect recovery time delay. When FAULT is asserted, the TRISTATE output is immediately asserted low and held low for the time period specified by this constant. A constant value of 0x0001 in this register is approximately 0.083 ms. The default value of 0x300C gives approximately 1 sec.

0x0000 is a reserved value.

6.26 Extended configuration register (addr 0x47)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	PS48DB	XAR1	XAR2	BQ5	BQ6	BQ7
0		0	0	0	1	1	1

The extended configuration register provides access to biquad 5, 6 and 7.

6.26.1 Extended post-scale range

Table 74. Extended post-scale range

PS48DB	Mode
0	Post-scale value is applied as defined in the coefficient RAM
1	Post-scale value is applied with a +48 dB offset with respect to the coefficient RAM value

Post-scale is an attenuation by default. When PS48DB is set to 1, a 48-dB offset is applied to the coefficient RAM value, so post-scale can act as a gain too.

6.26.2 Extended attack rate

The attack rate shown in *Table 67* can be extended to provide up to an 8 dB/ms attack rate on both limiters.

Table 75. Extended attack rate, limiter 1

XAR1	Mode
0	Limiter1 attack rate is configured using *Table 67*
1	Limiter1 attack rate is 8 dB/ms

Table 76. Extended attack rate, limiter 2

XAR2	Mode
0	Limiter2 attack rate is configured using Table 67
1	Limiter2 attack rate is 8 dB/ms

6.26.3 Extended biquad selector

Bass and treble controls can be configured as user-defined filters when the equalization coefficients link is activated (BQL = 1) and the corresponding BQx bit is set to 1.

Table 77. Extended biquad selector, biquad 5

BQ5	Mode
0	Reserved
1	User-defined biquad 5 coefficients are selected

Table 78. Extended biquad selector, biquad 6

BQ6	Mode
0	Pre-set bass filter selected as per Table 66
1	User-defined biquad 6 coefficients are selected

Table 79. Extended biquad selector, biquad 7

BQ7	Mode
0	Pre-set treble filter selected as per Table 66
1	User-defined biquad 7 coefficients are selected

When filters from the 5th to 7th are configured as user-programmable, the corresponding coefficients are stored respectively in addresses 0x20-0x24 (BQ5), 0x25-0x29 (BQ6), 0x2A-0x2E (BQ7) as given in Table 73.

Note: The BQx bits are ignored if BQL = 0 or if DEMP = 1 (relevant for BQ5) or CxTCB = 1 (relevant for BQ6 and BQ7).

6.27 PLL configuration registers (address 0x52; 0x53; 0x54; 0x55; 0x56; 0x57)

D7	D6	D5	D4	D3	D2	D1	D0
PLL_FRAC[15:8]							
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
PLL_FRAC[7:0]							
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
PLL_DITH[1:0]		PLL_NDIV[5:0]					
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
PLL_DPD	PLL_FCT	PLL_STB	PLL_STBBYP	PLL_IDIV[3:0]			
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	PLL_DIRP	PLL_PWD	PLL_BYP	OSC_PD	Reserved	BOOST32K
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	BYPSTATE	PDSTATE	OSCOK	LOWCK
NA	NA	NA	NA	NA	NA	NA	NA

By default, the STA381BW is able to configure the embedded PLL automatically depending on the MCS bits (reg 0x00). For certain applications and to provide flexibility to the user, a manual PLL configuration can be used (setting PLL_DIRP to ‘1’)

The output PLL frequency formula is:

$$\mathrm{Fin} \times \left(\frac{(\mathrm{NDIV})}{(\mathrm{IDIV}+1)} + \left(\frac{\mathrm{FRAC}}{65536} \right) \right)$$

where Fin is the input clock frequency from the pad.

Table 80. PLL factors

PLL parameter	Min	Max
FRAC	0	65535
IDIV	0	3
NDIV	5	55

Table 81. PLL register 0x54 bits

Bit	R/W	RST	Name	Description
7	R/W	0	PLL_DITH[1:0]	"00": PLL clock dithering disabled "01": PLL clock dithering enabled (triangular) "10": PLL clock dithering enabled (rectangular) "11": reserved
6	R/W	0		
5	R/W	0	PLL_NDIV	PLL loop divider
4	R/W	0		
3	R/W	0		
2	R/W	0		
1	R/W	0		
0	R/W	0		

Table 82. PLL register 0x55 bits

Bit	R/W	RST	Name	Description
7	R/W	0	PLL_DPD	'0': any PLL dividers change is implemented via PLL power-down '1': PLL divider change will happen without PLL power-down
6	R/W	0	PLL_FCT	'0': PLL use integer ratio '1': PLL use fractional ratio
5	R/W	0	PLL_STB	PLL synchronous divider changes strobe
4	R/W	0	PLL_STBBYP	'0': PLL_STB is active '1': PLL_STB control is bypassed
3	R/W	0	PLL_IDIV[3:0]	Input PLL divider
2	R/W	0		
1	R/W	0		
0	R/W	0		

Table 83. PLL register 0x56 bits

Bit	R/W	RST	Name	Description
5	R/W	0	PLL_DIRP	'0': PLL configuration is determined by the MCS bits '1': PLL configuration is determined by FRAC, IDIV and NDIV
4	R/W	0	PLL_PWD	'0': PLL normal behavior '1': PLL is in power-down mode
3	R/W	0	PLL_BYP	'0': sys clock is from PLL '1': sys clock is from external pin (PLL is bypassed)
2	R/W	0	OSC_PD	'0': Normal behavior '1': Internal oscillator is in power-down
0	R/W	0	BOOST32K	'0': Input oversampling selected by the IR bits '1': Input oversampling is selected x3

Table 84. PLL register 0x57 bits

Bit	R/W	RST	Name	Description
3	R/W		BYPSTATE	PLL bypass state
2	R/W		PDSTATE	PLL PD state
1	R/W		OSCOK	OSCI locked
0	R/W		LOWCK	Clock input low-frequency check

6.28 Short-circuit protection mode registers SHOK (address 0x58)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	GNDSH	VCCSH	OUTSH
NA	NA	NA	NA	NA	NA	NA	NA

The following power bridge pins short-circuit protections are implemented in the STA381BW:

- OUTxx vs. GNDx
- OUTxx vs. VCCx
- OUT1B vs. OUT2A

The protection is enabled when reg. 0x50 bit 0 (SHEN) is set to ‘1’. The protection will check the short-circuit when the EAPD bit is toggled from ‘0’ to ‘1’ (i.e. the power bridge is switched on), and only if the test passes (no short), does the power bridge leave the tristate condition.

Register 0x58 (read-only registers) will give more information about the detected short type.

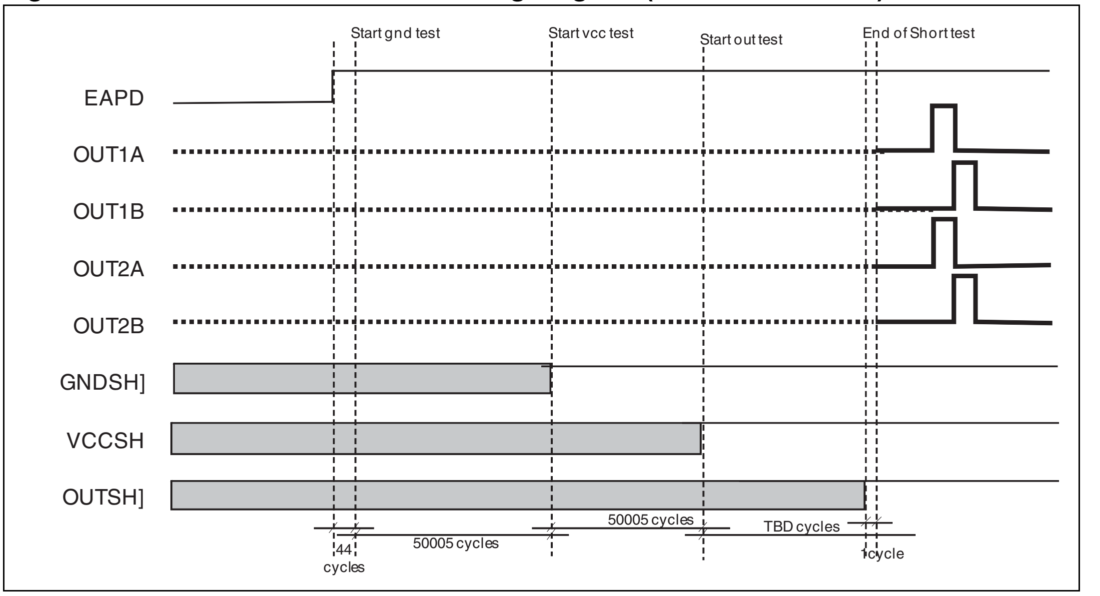
GNDSH equal to ‘0’ means that OUTxx is shorted to ground, while the same value on VCCSH means that OUTxx is shorted to Vcc, finally OUTSH=’0’ means that OUT1B is shorted to OUT2A.

To be noted that once the check is performed, and the tristate released, the short protection is not active anymore until the next EAPD 0->1 toggling which means that shorts that happened during normal operation cannot be detected.

To be noted that register SHOK is meaningful only after the EAPD bit is set to ‘1’ at least once.

The short-circuit protections implemented are effective only in BTL configuration, and they must not be activated if a single-ended application scheme is needed.

Figure 26. Short-circuit detection timing diagram (no short detected)



In *Figure 26* the short protection timing diagram is shown. The time information is expressed in clock cycles, where the clock frequency is defined as in section *Section 6.13.1: Master clock select*. The gray color is used for the short status bits to indicate that the bits are carrying the status of the previous EAPD 0->1 toggling (to be noted that after reset this state is meaningless since no EAPD transition occurs). The GND-related SHOK bits are updated as soon as the gnd test is completed, the VCC bits are updated after vcc test is completed, and the SOUT bit is updated after the shorted output test is completed. The gnd test, vcc test and output test, are always run (if the SHEN bit is active and EAPD toggled to ‘1’), and only if both tests are successful (no short) do the bridge outputs leave the tristate (indicated by dotted lines in the figure). If one of the three tests (or all) fail, the power bridge outputs are kept in the tristate until the procedure is restarted with a new EAPD toggling.

In this figure EAPD is intended to be bit 7 of register 0x05.

6.29 Extended coefficient range up to -4...4 (address 0x5A)

D7	D6	D5	D4	D3	D2	D1	D0
CEXT_B4[1]	CEXT_B4[0]	CEXT_B3[1]	CEXT_B3[0]	CEXT_B2[1]	CEXT_B2[0]	CEXT_B1[1]	CEXT_B1[0]
1	0	1	0	1	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	CEXT_B7[1]	CEXT_B7[0]	CEXT_B6[1]	CEXT_B6[0]	CEXT_B51]	CEXT_B5[0]
0	0	1	0	1	0	1	0

Biquads from 1 to 7 have in the STA381BW the possibility to extend the coefficient range from [-1,1) to [-4..4) which allows the use of high-shelf filters that may require a coefficient-dynamic greater in absolute value than 1.

Three ranges are available, [-1;1) [-2;2) [-4;4). By default, the extended range is activated. Each biquad has its independent setting according to the following table.

Table 85. **Coefficients extended range configuration**

CEXT_Bx[1]	CEXT_Bx[0]	Range
0	**0**	[-1;1)
0	**1**	[-2;2)
1	**0**	[-4;4)
1	**1**	**Reserved**

In this case the user can decide, for each filter stage, the right coefficient range. Note that for a given biquad the same range will be applied to the left and right (channel 1 and channel 2).

The crossover biquad does not have the availability of this feature, maintaining the [-1;1) range unchanged.

6.30 Miscellaneous registers (address 0x5C, 0x5D)

D7	D6	D5	D4	D3	D2	D1	D0
RPDNEN	Reserved	BRIDGOFF	Reserved	Reserved	CPWMEN	Reserved	Reserved
0	1	1	0	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
LPDP	LPD	LPDE	PNDLSL[2]	PNDLSL[1]	PNDLSL[0]	Reserved	SHEN
0	1	0	0	1	1	0	0

6.30.1 Rate power-down enable (RPDNEN) bit

In the STA381BW, by default, the power-down pin and I^2C power-down act on mute commands to perform the fade-out. This default can be changed so that the fade-out can be started using the master volume. The RPDNEN bit, when set, activates this feature.

6.30.2 Bridge immediately off (BRIDGOFF) bit (address 0x4B, bit D5)

A fade-out procedure is started in the STA381BW once the PWDN function is enabled, and after 13 million clock cycles (PLL internal frequency) the bridge is put in power-down (tristate mode). There is also the possibility to change this behavior so that the power bridge will be switched off immediately after the PWDN pin is tied to ground, without waiting for the 13 million clock cycles. The BRIDGOFF bit, when set, activates this function. Obviously the immediate power-down will generate a pop noise at the output, therefore this procedure must be used only in cases where pop noise is not relevant in the application. Note that this feature works only for hardware PWDN assertion and not for a power-down applied through the IIC interface. Refer to *Section 6.30.5* if programming a different number of clock cycles is needed.

6.30.3 Channel PWM enable (CPWMEN) bit

This bit, when set, activates a mute output in case the volume reaches a value lower than -76 dBFS.

6.30.4 External amplifier hardware pin enabler (LPDP, LPD LPDE) bits

Pin 42 (INTLINE), normally indicating a fault condition, using the following 3 register settings can be reconfigured as a hardware pin enabler for an external headphone or line amplifier.

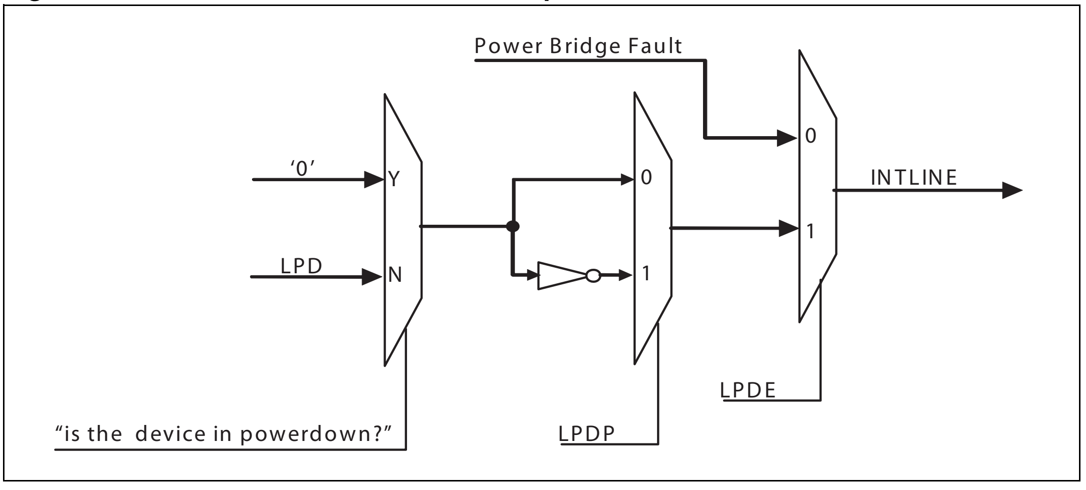
In particular the LPDE bit, when set, activates this function. Accordingly, the LPD value (0 or 1) is exported on pin 42 and in case of power-down assertion, pin 42 is tied to LPDP.

The LPDP bit, when set, negates the value programmed as the LPD value, refer to the following table.

Table 86. External amplifier enabler configuration bits

LPDP	LPD	LPDE	Pin 42 output
x	x	0	INT_LINE
0	0	1	0
0	1	1	1
1	0	1	1
1	1	1	0

Figure 27. Alternate function for INTLINE pin



6.30.5 Power-down delay selector (PNDLSL[2:0]) bits

The assertion of PWDN activates a counter that, by default, after 13 million clock cycles puts the power bridge in tristate mode, independently from the fade-out time. Using these registers it is possible to program this counter according to the following table.

Table 87. PNDLSL bits configuration

PNDLSL[2]	PNDLSL[1]	PNDLSL[2]	Fade-out time
0	0	0	Default time (13M PLL clock cycles)
0	0	1	Default time divided by 2
0	1	0	Default time divided by 4
0	1	1	Default time divided by 8
1	0	0	Default time divided by 16
1	0	1	Default time divided by 32
1	1	0	Default time divided by 64
1	1	1	Default time divided by 128

6.30.6 Short-circuit check enable bit

This bit, when enabled, will activate the short-circuit checks before any power bridge activation (EAPD bit 0->1). See section *Section 6.28: Short-circuit protection mode registers SHOK (address 0x58)* for more details.

6.31 Bad PWM detection registers (address 0x5E, 0x5F, 0x60)

D7	D6	D5	D4	D3	D2	D1	D0
BPTH[5]	BPTH[4]	BPTH[3]	BPTH[2]	BPTH[1]	BPTH[0]	reserved	reserved
0	0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
BPTIM[7]	BPTIM[6]	BPTIM[5]	BPTIM[4]	BPTIM[3]	BPTIM[2]	BPTIM[1]	BPTIM[0]
0	1	0	1	1	1	1	0

The STA381BW implements a detection on PWM outputs able to verify if the output signal has no zero-crossing in a configurable time window. This check can be useful to detect the DC level in the PWM outputs. To be noted that the checks are performed on logic level PWM (i.e. not the power bridge ones, nor the PWM on DDX3 and DDX4 IOs).

In case of ternary modulation, the detection threshold is computed as:

TH=[(BPTH*2+1)/128]*100%

If the measured PWM duty cycle is detected greater than or equal to TH for more than BPTIM PWM periods, the corresponding PWM bit will be set in register 0x01.

In case of binary modulation, there are two thresholds:

TH1=[(64+BPTH)/128]*100%

TH2=[(64-BPTH)/128]*100%

In this case if the measured PWM duty cycle is outside the TH1-TH2 range for more than BPTIM PWM periods, the corresponding bit will be set in register 0x4E.

6.32 Enhanced zero-detect mute and input level measurement (address 0x61-0x65, 0x3F, 0x40, 0x6F)

D7	D6	D5	D4	D3	D2	D1	D0
WTHH	WTHL	FINETH	HSEL[1:0]		ZMTH[2:0]		
0	0	0	0	0	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
RMS_CH0[7:0]							
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

D7	D6	D5	D4	D3	D2	D1	D0
RMS_CH0[15:8]							
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

D7	D6	D5	D4	D3	D2	D1	D0
RMS_CH1[7:0]							
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

D7	D6	D5	D4	D3	D2	D1	D0
RMS_CH1[15:8]							
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

The STA381BW implements an RMS-based zero-detect function (on serial input interface data) able to detect in a very reliable way the presence of an input signal, so that the power bridge outputs can be automatically connected to ground.

When active, the function will mute the output PWM when the input level becomes less than “threshold - hysteresis”. Once muted, the PWM will be unmuted when the input level is detected greater than “threshold + hysteresis”.

The measured level is then reported (for each input channel) on registers ZCCCFG1 - ZCCCFG2, ZCCCFG3 - ZCCCFG4 according to the following equation:

Value_in_dB = $20 \cdot Log_{10}(Reg\_value/(2^{16} \cdot 0.635))$

Table 88. Zero-detect threshold

ZMTH[2:0]	Equivalent input level (dB)
000	-78
001	-84
010	-90
011	-96
100	-102
101	-108
110	-114
111	-114

Table 89. Zero-detect hysteresis

HSEL[1:0]	Equivalent input level hysteresis(dB)
00	3
01	4
10	5
11	6

The thresholds and hysteresis table above can be overridden and the low-level threshold and high-level threshold can be set by the MTH[21:0] bits.

To activate the manual thresholds the FINETH bit has to be set to ‘1’.

To configure the low threshold, the WTHL bit must be set to ‘1’ so that any write operation to the MTH bits will set the low threshold.

To configure the low threshold, the WTHH bit must be set to ‘1’ so that any write operation to the MTH bits will set the low threshold.

If the zero-mute block does not detect mute, it will mute the output when the current RMS value falls below the low threshold.

If the zero-mute block does not detect mute, it will unmute the output when the current RMS value rises above the high threshold.

Table 90. Manual threshold register 0x3F, 0x40 and 0x6F

D7	D6	D5	D4	D3	D2	D1	D0
ReservedT	Reserved	MTH[21:16]					
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
MTH[15:8]							
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
MTH[7:0]							
0	0	0	0	0	0	0	0

6.33 Headphone/Line out configuration register (address 0x66)

D7	D6	D5	D4	D3	D2	D1	D0
HPLN	Reserved	Reserved	Reserved	CPFEN	CPOK	ABFAULT	DCROK
0	0	1	0	0	NA	NA	NA

Table 91. Headphone/Line out configuration bits

Bit	R/W	RST	Name	Description
7	R/W	0	HPLN	When F3X is connected to the internal HP/Line driver this bit selects the gain of the F3X->analog out path. ‘0’: HP out. When the MVOL+Channel Vol is 0 dBFs, a 0 dBFs input will generate a 40 mW output on a 32 ohm load (+/- 3.3V supply). ‘1’: Line out. When the MVOL+Channel Vol is 0 dBFs, a 0 dBFs input will generate a 2 Vrms output (+/- 3.3 V supply)
3	R/W	0	CPFEN	‘0’: Charge pump auto-enable when unmute ‘1’: Charge pump is always enabled
2	R	NA	CPOK	‘0’: Charge pump is not working ‘1’: Charge pump is working and it is OK
1	R	NA	ABFAULT	‘0’: No fault on class-AB ‘1’: Overcurrent fault detected on class-AB
0	R	NA	DCROK	‘1’: Core supply OK

6.34 F3XCFG (address 0x69; 0x6A)

D7	D6	D5	D4	D3	D2	D1	D0
F3XLNK	reserved	reserved	reserved	reserved	reserved	reserved	reserved
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
F3X_FAULT	reserved	reserved	F3X_SM_SLOPE[2:0]			F3X_MUTE	F3X_ENA
1	1	1	0	1	1	1	0

Table 92. F3X configuration register 1

Bit	R/W	RST	Name	Description
7	R/W	0	F3XLNK	'0': F3X normal control mode '1': F3X mute/unmute linked to HP/Line mute

Table 93. F3X configuration register 2

Bit	R/W	RST	Name	Description
7	R	1	F3X_FAULT	'0': Normal operation
4	R/W	0	F3X_SM_SLOPE	'000': 0 ms '001': 25 ms '010': 50 ms '011': 100 ms '100': 200 ms '101': 250 ms '110': 500 ms '111': 1000 ms
3	R/W	1		
2	R/W	1		
1	R/W	1	F3X_MUTE	'1': Mute
0	R/W	0	F3X_ENA	'1': F3X enable

6.35 STCompressor^{TM} configuration register (address 0x6B; 0x6C)

Table 94. Register STCCFG0

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	CRC_RES	Reserved	Reserved
0	0	0	1	0	0	0	0

Table 95. STCCFG0 register

Bit	R/W	RST	Name	Description
2	R/W	0	CRC_RES	‘0’ = CRC comparison successful ‘1’ = CRC comparison error

Table 96. Register STCCFG1

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	STC_LNK	Reserved
0	0	0	0	0	0	0	0

Table 97. STCCFG1 register

Bit	R/W	RST	Name	Description
1	R/W	0	STC_LNK	‘0’ = normal operations ‘1’ = stereo link enabled. See *Section 4.3.8: Stereo link*

6.36 Charge pump synchronization (address 0x70)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	CHPI	INITCNT[3:0]				CHPRD
0	0	0	1	1	0	0	1

Table 98. Charge pump sync configuration bits

Bit	R/W	RST	Name	Description
5	R/W	0	CHPI	‘0’: Charge pump phase: 0 deg ‘1’: Charge pump phase: 180 deg
4	R/W	1	INITCNT[3:0]	Change charge pump phase at one clock step
3	R/W	1		
2	R/W	0		
1	R/W	0		
0	R/W	1	CHPRD	‘0’: Charge pump synchronized with PWM frame ‘0’: Charge pump not synchronized with PWM frame

The charge pump can be synchronized with the PWM frame in order to minimize the crosstalk between the charge pump and the PWM waveform.

This functionality cannot be activated when the PWMS bit (address 0x15 bit D4) is set to 1.

6.37 Coefficient RAM CRC protection (address 0x71-0x7D)

D7	D6	D5	D4	D3	D2	D1	D0
BQCKE[7]	BQCKE[6]	BQCKE[5]	BQCKE[4]	BQCKE[3]	BQCKE[2]	BQCKE[1]	BQCKE[0]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BQCKE[15]	BQCKE[14]	BQCKE[13]	BQCKE[12]	BQCKE[11]	BQCKE[10]	BQCKE[9]	BQCKE[8]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BQCKE[23]	BQCKE[22]	BQCKE[21]	BQCKE[20]	BQCKE[19]	BQCKE[18]	BQCKE[17]	BQCKE[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKE[7]	XCCKE[6]	XCCKE[5]	XCCKE[4]	XCCKE[3]	XCCKE[2]	XCCKE[1]	XCCKE[0]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKE[15]	XCCKE[14]	XCCKE[13]	XCCKE[12]	XCCKE[11]	XCCKE[10]	XCCKE[9]	XCCKE[8]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKE[23]	XCCKE[22]	XCCKE[21]	XCCKE[20]	XCCKE[19]	XCCKE[18]	XCCKE[17]	XCCKE[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BQCKR[7]	BQCKR[6]	BQCKR[5]	BQCKR[4]	BQCKR[3]	BQCKR[2]	BQCKR[1]	BQCKR[0]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BQCKR[15]	BQCKR[14]	BQCKR[13]	BQCKR[12]	BQCKR[11]	BQCKR[10]	BQCKR[9]	BQCKR[8]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BQCKR[23]	BQCKR[22]	BQCKR[21]	BQCKR[20]	BQCKR[19]	BQCKR[18]	BQCKR[17]	BQCKR[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKR[23]	XCCKR[22]	XCCKR[21]	XCCKR[20]	XCCKR[19]	XCCKR[18]	XCCKR[17]	XCCKR[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKR[23]	XCCKR[22]	XCCKR[21]	XCCKR[20]	XCCKR[19]	XCCKR[18]	XCCKR[17]	XCCKR[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKR[23]	XCCKR[22]	XCCKR[21]	XCCKR[20]	XCCKR[19]	XCCKR[18]	XCCKR[17]	XCCKR[16]

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCAUTO	XCRES	XCCMP	XCGO	BCAUTO	BCCRES	BCCMP	BCCGO
0	0	0	0	0	0	0	0

The STA381BW implements an automatic CRC computation for the biquad and MDRC/XOver coefficient memory (*Table 73*). Memory cell contents from address 0x00 to 0x27 will be bit XORed to obtain the BQCHKE checksum, while cells from 0x28 to 0x31 will be XORed to obtain the XCCHKE checksum. Both checksums (24-bit wide) are exported on I^2C registers from 0x60 to 0x65. The checksum computation will start as soon as the BCGO (for biquad RAM bank) or the XCGO bit (for MDRC/XOver coefficients) is set to 1. The checksum is computed at the processing sample rate if the IR bits equal “01” or “10”, otherwise the checksum is computed to half of the processing sample rate.

When BCCMP or XCCMP is set to ‘1’, the relative checksum (BQCHKE and XCCHKE) is continuously compared with BQCHKR and XCCHKR respectively. If the checksum matches its own reference value, the respective result bits (BCRES and XCRES) will be set to ‘0’. The compare bits have no effect if the respective GO bit is not set.

In case of checksum errors (i.e. the internally computed didn’t match the reference), an automatic device reset action can be activated. This function is enabled when the BCAUTO or XCAUTO bit is set to ‘1’. The automatic reset bits have no effect if the respective compare bits are not set.

The recommended procedure for automatic reset activation is the following:

- Download the set of coefficients (RAM locations 0x00…0x27)
- Download the externally computed biquad checksum into registers *BQCHKR*
- Enable the checksum of the biquad coefficients by setting the *BCGO* bit. The checksum will start to be automatically computed by the STA381BW and its value exposed on registers *BQCHECKE.* The checksum value is computed and updated.
- Enable the checksum comparison by setting the *BCCMP* bit. The internally computed checksum will start to be compared with the reference one and the result will be exposed on the *BCRES* bit. The following operation will be executed on each audio frame:

```
if ((BQCHKE == BQCHKR))
{
    BC_RES = 0;// Checksum is ok, reset the error bit
}
```

else

{

BC_RES = 1;// Checksum error detected, set the error bit

}

- Wait until the BCRES bit goes to 0, meaning that the checksum result bit has started to be updated and everything is ok. Time-out of this operation (e.g. >1 ms) will indicate checksum failure, and the MCU will handle this event
- Enable automatic reset of the device in case of checksum error by setting the *BCAUTO* bit. The *BCRES* bit will then be automatically checked by the STA381BW, on each audio frame, and a reset event will be triggered in case of checksum mismatch.
- Periodically check the *BC_RES* status. A value of 1 indicates a checksum mismatch has occurred and, therefore, that the device went through a reset cycle.

The previous example is intended for biquad CRC bank calculation, but it can be easily extended to MDRC/XOver CRC computation.

6.38 MISC4 (address 0x7E)

D7	D6	D5	D4	D3	D2	D1	D0
SMAP	reserved	reserved	reserved	reserved	reserved	WRA	CH12
1	0	0	0	0	0	0	0

Table 99. Misc register 4

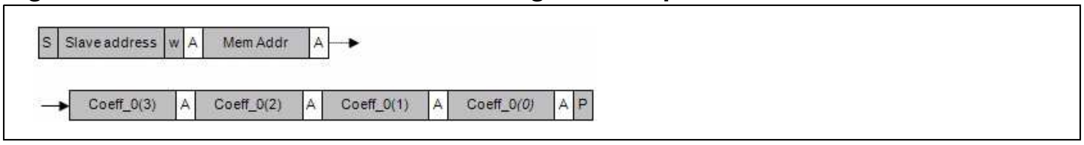
Bit	R/W	RST	Name	Description
7	R/W	1	SMAP	‘1’ = NEW MAP ‘0’ = STMAP
1	R/W	0	WRA	‘0’ = normal operations ‘1’ = enables the write-all procedure when using the RAM coefficients direct access
0	R/W	0	CH12	‘0’ = normal operations ‘1’ = enables the RAM coefficients direct access

The STA381BW allows direct access to the RAM coefficients bypassing the indirect access mechanism described in *Section 6.24: User-defined coefficient control registers (addr 0x27 - 0x37)*. Direct access is implemented as follows.

Direct single-write procedure

1. Set reg 0x7E bit 0 to 1 and bit 1 to 0 to enable the direct RAM access in single-write mode.
2. Write the coefficient value to the device using an I^{2}C bus single-write operation as discribed in *Figure 28*.

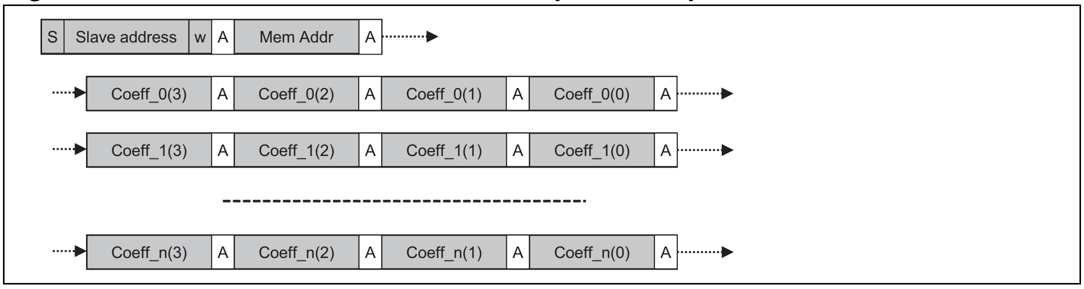
Figure 28. Coefficients direct access single-write operation



Direct multi-write procedure

1. Set the reg 0x7E bit 0 to 1 and bit 1 to 1 to enable direct RAM access in multi-write mode.
2. Write the coefficients value to the device using an I^{2}C bus multi-write operation as discribed in *Figure 29*. Please note that by using the multi-write procedure, it is possible to write the entire RAM contents at once.

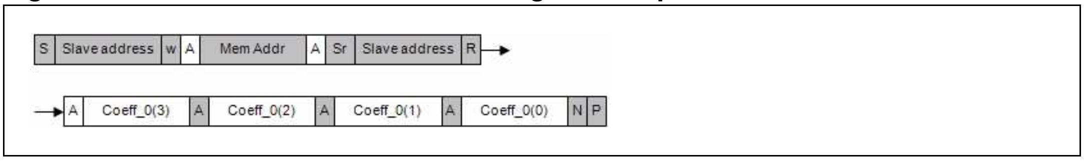
Figure 29. Coefficients direct access multiple-write operation



Direct single-read procedure

1. Set reg 0x7E bit 0 to 1 and bit 1 to 0 to enable the direct RAM access in single-read mode.
2. Read the coefficient value from the device using an I^{2}C bus single-read operation as discribed in *Figure 30*.

Figure 30. Coefficients direct access single-read operation



Please be aware that the STA381BW supports 24-bit coefficients, for this reason in the above figures Coeff_x(0) is always equal to 0x00 when either reading or writing. The multi-write procedure embeds a wrap-around mechanism: when trying to write into a location exceeding the maximum coefficient address, the multi-write procedure will start from location 0x00.

7 Register description: Sound Terminal compatibility

To keep compatibility with previous Sound Terminal devices, the 0x7E bit D7 must be set to 0 after device turn-on and after any reset (via SW or via external pin).

Missing addresses are to be considered as reserved.

Table 100. I²C registers summary

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
00	CONFA	FDRB			IR1	IR0	MCS2	MCS1	MCS0
01	CONFB	C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
02	CONFC			CSZ3	CSZ2	CSZ1	CSZ0		
03	CONFD	SME	ZDE		BQL	PSL	DSPB		
04	CONFE	SVE	ZCE		PWMS	AME	NSBW		
05	CONFF	EAPD	PWDN		LDTE	BCLE	IDE	OCFG1	OCFG0
06	MUTE LOC	LOC1	LOC0		BQB_ALL	C3M	C2M	C1M	MMUTE
07	MVOL	MVOL[7:0]							
08	CH1VOL	CH1VOL[7:0]							
09	CH2VOL	CH2VOL[7:0]							
0A	CH3VOL	CH3VOL[7:0]							
0C	AUTO	XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0E	C1CFG	C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VBP	C1EQBP	C1TCB
0F	C2CFG	C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VBP	C2EQBP	C2TCB
10	C3CFG	C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VBP		
11	TONE	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
12	L1AR	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
13	L1ATRT	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
14	L2AR	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
15	L2ATRT	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
16	CFADDR			CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
17	B1CF1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
18	B1CF2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
19	B1CF3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
1A	B2CF1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
1B	B2CF2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
1C	B2CF3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
1D	A1CF1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
1E	A1CF2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8

Table 100. I²C registers summary (continued)

1F	A1CF3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
20	A2CF1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
21	A2CF2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
22	A2CF3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
23	B0CF1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
24	B0CF2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
25	B0CF3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
26	CFUD					RA	R1	WA	W1
2B	FDRC1	FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
2C	FDRC2	FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
2D	STATUS	PLLUL	FAULT						
2E	MTH2			MTH[21:16]					
2F	MTH1	MTH[15:8]							
31	EQCFG	XOB							
32	EATH1	EATHEN1	EATH1[6:0]						
33	ERTH1	ERTHEN1	ERTH1[6:0]						
34	EATH2	EATHEN2	EATH2[6:0]						
35	ERTH2	ERTHEN2	ERTH2[6:0]						
36	CONFX	MDRCE		PS48DB	XAR1	XAR2	BQ5	BQ6	BQ7
37	SVUP			SVUP_EN	SVUP_RATE[4:0]				
38	SVDN			SVDN_EN	SVDN_RATE[4:0]				
3F	EVOLRES	VRES_EN	VRESTG_EN	EXVRES_CH3[1:0]		EXVRES_CH2[1:0]		EXVRES_CH1[1:0]	
40	EVOLRES2							EXVRES_MVOL[1:0]	
41	PLLFRAC1	PLL_FRAC[15:8]							
42	PLLFRAC0	PLL_FRAC[7:0]							
43	PLLDIV	PLL_DITH[1:0]		PLL_NDIV[5:0]					
44	PLLCFG0	PLL_DPD	PLL_FCT	PLL_STB	PLL_STBBYP	PLL_IDIV[3:0]			
45	PLLCFG1			PLL_DIRP	PLL_PWD	PLL_BYP	OSC_PD		BOOST32K
46	PLLSTATE					BYPSTATE	PDSTATE	OSCOK	LOWCK
47	SHOK						GNDSH	VCCSH	OUTSH
49	CXT41	CEXT_B4[1:0]		CEXT_B3[1:0]		CEXT_B2[1:0]		CEXT_B1[1:0]	
4A	CXT75			CEXT_B7[1:0]		CEXT_B6[1:0]		CEXT_B5[1:0]	
4B	MISC1	RPDNEN		BRIDGOFF			CPWMEN		

Table 100. I²C registers summary (continued)

4C	MISC2	LPDP	LPD	LPDE	PNDLSL[2:0]				SHEN
4D	BPTH	BPTH(5:0)							
4E	BADPWM	BP4B	BP4A	BP3B	BP3A	BP2B	BP2A	BP1B	BP1A
4F	BPTIM	BPTIM[7:0]							
50	ZCCFG0	WTHH	WTHL	FINETH	HSEL[1:0]		ZMTH[2:0]		
51	ZCCFG1	RMS_CH0[7:0]							
52	ZCCFG2	RMS_CH0[15:8]							
53	ZCCFG3	RMS_CH1[7:0]							
54	ZCCFG4	RMS_CH1[15:8]							
55	HPCFG	HPLN		MUTE		CPFEN	CPOK	ABFAULT	DCROK
58	F3XCFG1	F3XLNK							
59	F3XCFG2	F3X_ FAULT			F3X_SM_SLOPE[2:0]			F3X_ MUTE	F3X_ENA
5A	STCCFG0		LIM_ BYP	STC_BYP	STC_ENA		NP_ CRCRES		NP_CRC_ GO
5B	STCCFG1							STC_LNK	BRC_EN
5E	MTH0	MTH[7:0]							
5F	CHPSINC			CHPI	INITCNT[3:0]				CHPRD
60	BQCHKE0	BQ_CKE[7:0]							
61	BQCHKE1	BQ_CKE[15:8]							
62	BQCHKE2	BQ_CKE[23:16]							
63	XCCHKE0	XC_CKE[7:0]							
64	XCCHKE1	XC_CKE[15:8]							
65	XCCHKE2	XC_CKE[23:16]							
66	BQCHKR0	BQ_CKR[7:0]							
67	BQCHKR1	BQ_CKR[15:8]							
68	BQCHKR2	BQ_CKR[23:16]							
69	XCCHKR0	XC_CKR[7:0]							
6A	XCCHKR1	XC_CKR[15:8]							
6B	XCCHKR2	XC_CKR[23:16]							
6C	CHKCTRL	XCAUTO	XCRES	XCCMP	XCGO	BCAUTO	BCRES	BCCMP	BCGO
6E	MISC3						SRESET		
7E	MISC4	SMAP							

7.1 Configuration register A (addr 0x00)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	Reserved	Reserved	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	1	1	1

7.1.1 Master clock select

Table 101. Master clock select

Bit	R/W	RST	Name	Description
0	R/W	1	MCS0	Selects the ratio between the input I^2S sampling frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	1	MCS2	

The STA381BW supports sampling rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. Therefore the internal clock is:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin or BICKI pin (depending on MCS settings) must be a multiple of the input sampling frequency (f_s).

The relationship between the input clock (either XTI or BICKI) and the input sampling rate is determined by both the MCSx and the IR (input rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally. In *Table 102* MCS 111 and 110 indicate that BICKI has to be used as the clock source, while XTI is used in all the other cases.

Table 102. Input sampling rates

Input sampling rate *fs* (kHz)	IR	MCS[2:0]							
		111	110	101	100	011	010	001	000
32, 44.1, 48	00	64*fs(*)	NA	576 * fs	128 * fs	256 * fs	384 * fs	512 * fs	768 * fs
88.2, 96	01	64*fs(*)	32*fs(*)	NA	64 * fs	128 * fs	192 * fs	256 * fs	384 * fs
176.4, 192	1X	64*fs(*)	32*fs(*)	NA	32 * fs	64 * fs	96 * fs	128 * fs	192 * fs

Note: (*) Clock is BICKI

7.1.2 Interpolation ratio select

Table 103. Internal interpolation ratio

Bit	R/W	RST	Name	Description
4:3	R/W	00	IR [1:0]	Selects internal interpolation ratio based on input I^2S sampling frequency

The STA381BW has variable interpolation (oversampling) settings such that internal processing and FFX output rates remain consistent. The first processing block interpolates by either 3 times (see *Section 4.2*), 2 times or 1 time (pass-through) or provides a 2 times downsample. The oversampling ratio of this interpolation is determined by the IR bits.

Table 104. IR bit settings as a function of the input sampling rate

Input sampling rate fs (kHz)	IR	1st stage interpolation ratio
32	00	2-times oversampling
44.1	00	2-times oversampling
48	00	2-times oversampling
88.2	01	Pass-through
96	01	Pass-through
176.4	10	2-times downsampling
192	10	2-times downsampling

7.1.3 Fault-detect recovery bypass

Table 105. Fault-detect recovery bypass

Bit	R/W	RST	Name	Description
7	R/W	0	FDRB	0: fault-detect recovery enabled 1: fault-detect recovery disabled

The on-chip STA381BW power output block provides feedback to the digital controller using inputs to the power control block. The FAULT input is used to indicate a fault condition (either overcurrent or thermal). When FAULT is asserted (set to 0), the power control block attempts a recovery from the fault by asserting the tri-state output (setting it to 0 which directs the power output block to begin recovery), holds it at 0 for period of time in the range of 0.1 ms to 1 second as defined by the fault-detect recovery constant register (FDRC registers 0x2B-0x2C), then toggles it back to 1. This sequence is repeated as long as the fault indication exists. This feature is enabled by default, but can be bypassed by setting the FDRB control bit to 1.

7.2 Configuration register B (addr 0x01)

D7	D6	D5	D4	D3	D2	D1	D0
C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
1	0	0	0	0	0	0	0

7.2.1 Serial data interface

The STA381BW audio serial input was designed to interface with standard digital audio components and to accept a number of serial data formats. The STA381BW always acts as the slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data 1 and 2 SDI12.

The SAI bits (D3 to D0) and the SAIFB bit (D4) are used to specify the serial data format. The default serial data format is I^2S, MSB-first. Available formats are shown in the tables that follow.

7.2.2 Serial audio input interface format

Table 106. Serial audio input interface

Bit	R/W	RST	Name	Description
0	R/W	0	SAI0	Determines the interface format of the input serial digital audio interface
1	R/W	0	SAI1	
2	R/W	0	SAI2	
3	R/W	0	SAI3	

7.2.3 Serial data first bit

Table 107. Serial data first bit

SAIFB	Format
0	MSB-first
1	LSB-first

Table 108. Support serial audio input formats for MSB-first (SAIFB = 0)

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	0000	0	I^2S 15-bit data
	0001	0	Left/right-justified 16-bit data
48 * fs	0000	0	I^2S 16- to 23-bit data
	0001	0	Left-justified 16- to 24-bit data
	0010	0	Right-justified 24-bit data
	0110	0	Right-justified 20-bit data
	1010	0	Right-justified 18-bit data
	1110	0	Right-justified 16-bit data
64 * fs	0000	0	I^2S 16- to 24-bit data
	0001	0	Left-justified 16- to 24-bit data
	0010	0	Right-justified 24-bit data
	0110	0	Right-justified 20-bit data
	1010	0	Right-justified 18-bit data
	1110	0	Right-justified 16-bit data

Table 109. Supported serial audio input formats for LSB-first (SAIFB = 1)

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	1100	1	I^2S 15-bit data
	1110	1	Left/right-justified 16-bit data
48 * fs	0100	1	I^2S 23-bit data
	0100	1	I^2S 20-bit data
	1000	1	I^2S 18-bit data
	1100	1	LSB first I^2S 16-bit data
	0001	1	Left-justified 24-bit data
	0101	1	Left-justified 20-bit data
	1001	1	Left-justified 18-bit data
	1101	1	Left-justified 16-bit data
	0010	1	Right-justified 24-bit data
	0110	1	Right-justified 20-bit data
	1010	1	Right-justified 18-bit data
	1110	1	Right-justified 16-bit data
64 * fs	0000	1	I^2S 24-bit data
	0100	1	I^2S 20-bit data
	1000	1	I^2S 18-bit data
	1100	1	LSB first I^2S 16-bit data
	0001	1	Left-justified 24-bit data
	0101	1	Left-justified 20-bit data
	1001	1	Left-justified 18-bit data
	1101	1	Left-justified 16-bit data
	0010	1	Right-justified 24-bit data
	0110	1	Right-justified 20-bit data
	1010	1	Right-justified 18-bit data
	1110	1	Right-justified 16-bit data

To make the STA381BW work properly, the serial audio interface LRCKI clock must be synchronous to the PLL output clock which means that:

- the frequency of PLL clock / frequency of LRCKI = N ±4 cycles, where N depends on the settings in *Table 30 on page 58*
- the PLL must be locked.

If these two conditions are not met, and the IDE bit (reg 0x05 bit 2) is set to 1, the STA381BW will immediately mute the I^2S PCM data out (provided to the processing block) and it will freeze any active processing task.

To avoid any audio side effects (like pop noise), it is strongly recommended to soft-mute any audio streams flowing into the STA381BW data path before the desynchronization event happens. At the same time any processing related to the I^2C configuration should be issued only after the serial audio interface and the internal PLL are synchronous again.

Note: Any mute or volume change causes some delay in the completion of the I^2C operation due to the soft volume feature. The soft volume phase change must be finished before any clock desynchronization.

7.2.4 Delay serial clock enable

Table 110. Delay serial clock enable

Bit	R/W	RST	Name	Description
5	R/W	0	DSCKE	0: No serial clock delay 1: Serial clock delay by 1 core clock cycle to tolerate anomalies in some I^2S master devices

7.2.5 Channel input mapping

Table 111. Channel input mapping

Bit	R/W	RST	Name	Description
6	R/W	0	C1IM	0: Processing channel 1 receives left I^2S input 1: Processing channel 1 receives right I^2S input
7	R/W	1	C2IM	0: Processing channel 2 receives left I^2S input 1: Processing channel 2 receives right I^2S input

Each channel received via I^2S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

7.3 Configuration register C (addr 0x02)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	CSZ3	CSZ2	CSZ1	CSZ0	Reserved	Reserved
1	0	0	1	0	1	1	1

7.3.1 FFX compensating pulse size register

Table 112. FFX compensating pulse size bits

Bit	R/W	RST	Name	Description
2	R/W	1	CSZ0	When OM[1,0] = 11, this register determines the size of the FFX compensating pulse from 0 clock ticks to 15 clock periods.
3	R/W	1	CSZ1	
4	R/W	1	CSZ2	
5	R/W	0	CSZ3	

Table 113. Compensating pulse size

CSZ[3:0]	Compensating pulse size
0000	0 ns (0 ticks) compensating pulse size
0001	20 ns (1 tick) clock period compensating pulse size
…	…
1111	300 ns (15 ticks) clock period compensating pulse size

7.4 Configuration register D (addr 0x03)

D7	D6	D5	D4	D3	D2	D1	D0
SME	ZDE	Reserved	BQL	PSL	DSPB	Reserved	Reserved
0	0	0	1	1	0	0	0

7.4.1 DSP bypass

Table 114. DSP bypass

Bit	R/W	RST	Name	Description
2	R/W	0	DSPB	0: Normal operation 1: Bypass of biquad and bass/treble functions

Setting the DSPB bit bypasses the EQ function of the STA381BW.

7.4.2 Post-scale link

Table 115. Post-scale link

Bit	R/W	RST	Name	Description
3	R/W	1	PSL	0: Each channel uses individual post-scale value 1: Each channel uses channel 1 post-scale value

Post-scale functionality can be used for power supply error correction. For multi-channel applications running off the same power supply, the post-scale values can be linked to the value of channel 1 for ease of use and in order to update the values faster.

7.4.3 Biquad coefficient link

Table 116. Biquad coefficient link

Bit	R/W	RST	Name	Description
4	R/W	1	BQL	0: Each channel uses coefficient values 1: Each channel uses channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the channel-1 coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

7.4.4 Zero-detect mute enable

Table 117. Zero-detect mute enable

Bit	R/W	RST	Name	Description
6	R/W	0	ZDE	Setting of 1 enables the automatic zero-detect mute Setting of 0 disables the automatic zero-detect mute

Refer to *7.24: Enhanced zero-detect mute and input level measurement (address 0x50-0x54, 0x2E, 0x2F and 0x5E)*.

7.4.5 Submix mode enable

Table 118. Submix mode enable

Bit	R/W	RST	Name	Description
7	R/W	0	SME	0: Submix into left/right disabled 1: Submix into left/right enabled

7.5 Configuration register E (addr 0x04)

D7	D6	D5	D4	D3	D2	D1	D0
SVE	ZCE	Reserved	PWMS	AME	NSBW	Reserved	Reserved
1	0	0	0	0	0	1	0

7.5.1 Noise-shaper bandwidth selection

Table 119. Noise-shaper bandwidth selection

Bit	R/W	RST	Name	Description
2	R/W	0	NSBW	1: Third order NS 0: Fourth order NS

7.5.2 AM mode enable

Table 120. AM mode enable

Bit	R/W	RST	Name	Description
3	R/W	0	AME	0: Normal FFX operation 1: AM reduction mode FFX operation

The STA381BW features an FFX processing mode that minimizes the amount of noise generated in the frequency range of AM radio. This mode is intended for use when FFX is operating in a device with an active AM tuner. The SNR of the FFX processing is reduced to approximately 83 dB in this mode, which is still greater than the SNR of AM radio.

7.5.3 PWM speed mode

Table 121. PWM speed mode

Bit	R/W	RST	Name	Description
4	R/W	0	PWMS	0: Normal speed (384 kHz) all channels 1: Odd speed (341.3 kHz) all channels. Not suitable for binary BTL mode.

7.5.4 Zero-crossing enable

Table 122. Zero-crossing enable

Bit	R/W	RST	Name	Description
6	R/W	0	ZCE	‘1’: Volume adjustments only occur at digital zero-crossing ‘0’: Volume adjustments occur immediately

The ZCE bit enables zero-crossing adjustment. When volume is adjusted on digital zero-crossing, no clicks are audible.

7.5.5 Soft volume update enable

Table 123. Soft volume update enable

Bit	R/W	RST	Name	Description
7	R/W	1	SVE	1: Volume adjustments ramp according to SVR settings 0: Volume adjustments occur immediately

7.6 Configuration register F (addr 0x05)

D7	D6	D5	D4	D3	D2	D1	D0
EAPD	PWDN	Reserved	LDTE	BCLE	IDE	OCFG1	OCFG0
0	1	0	1	1	1	0	0

7.6.1 Output configuration

Table 124. Output configuration

Bit	R/W	RST	Name	Description
0	R/W	0	OCFG0	Selects the output configuration
1	R/W	0	OCFG1	

Table 125. Output configuration engine selection

OCFG[1:0]	Output configuration	PBTL enable
00	2-channel (full-bridge) power, 2-channel data-out: 1A/1B → 1A/1B 2A/2B → 2A/2B LineOut1 → 3A/3B LineOut2 → 4A/4B Line Out configuration determined by LOC register	No
01	2(half-bridge).1(full-bridge) on-board power: 1A → 1A Binary 0 ° 2A → 1B Binary 90° 3A/3B → 2A/2B Binary 45° 1A/B → 3A/B Binary 0° 2A/B → 4A/B Binary 90°	No
10	2-channel (full-bridge) power, 1-channel FFX: 1A/1B → 1A/1B 2A/2B → 2A/2B 3A/3B → 3A/3B EAPDEXT and TWARNEXT active	No
11	1-channel mono-parallel: 3A → 1A/1B w/ C3BO 45° 3B → 2A/2B w/ C3BO 45° 1A/1B → 3A/3B 2A/2B → 4A/4B	Yes

Note: To the left of the arrow is the processing channel. When using channel output mapping, any of the three processing channel outputs can be used for any of the three inputs.

Figure 31. OCFG = 00 (default value)

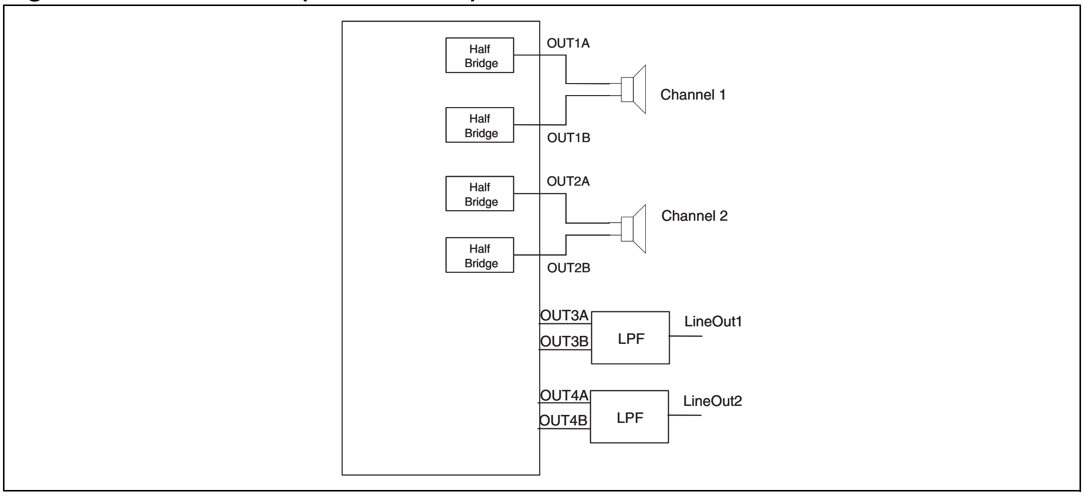


Figure 32. OCFG = 01

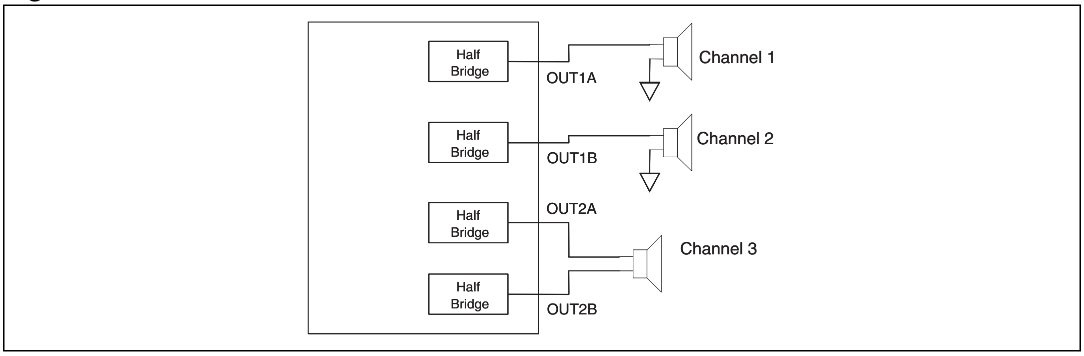


Figure 33. OCFG = 10

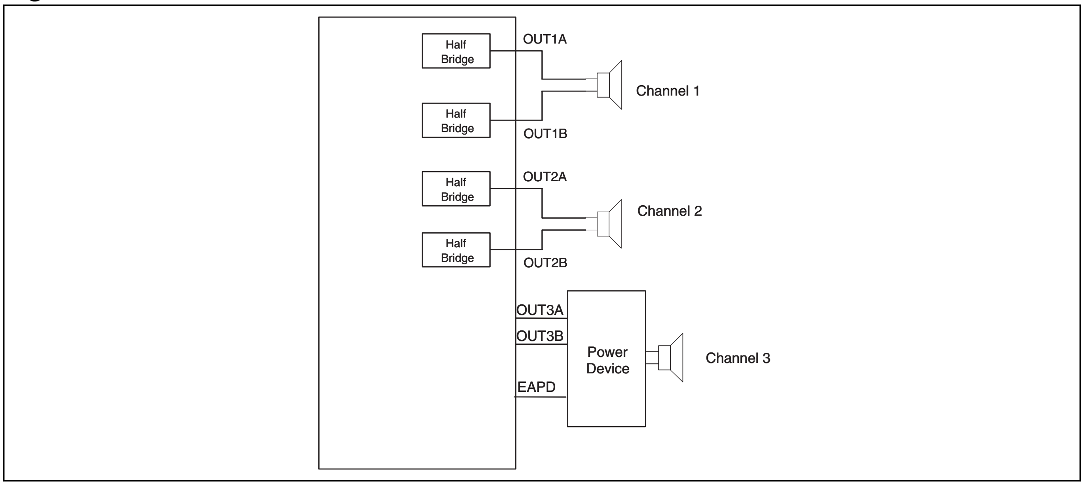
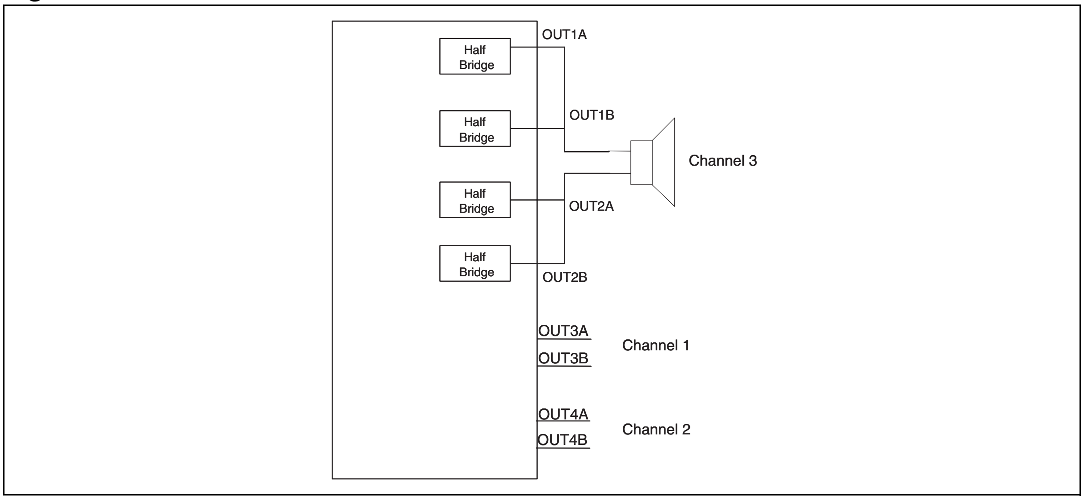
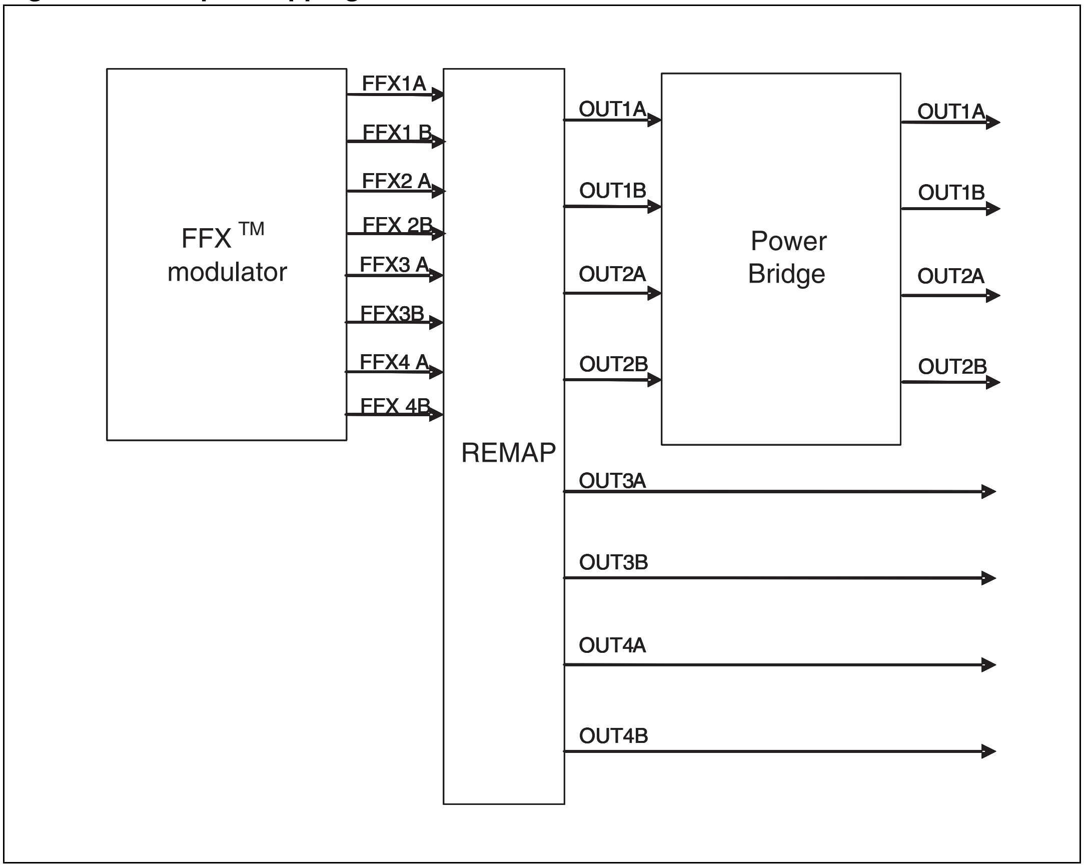


Figure 34. OCFG = 11



The STA381BW can be configured to support different output configurations. For each PWM output channel a PWM slot is defined. A PWM slot is always 1 / (8 * fs) seconds length. The PWM slot defines the maximum extension for the PWM rising and falling edge, that is, the rising edge as well as the falling edge cannot range outside the PWM slot boundaries.

Figure 35. Output mapping scheme



For each configuration the PWM signals from the digital driver are mapped in different ways to the power stage:

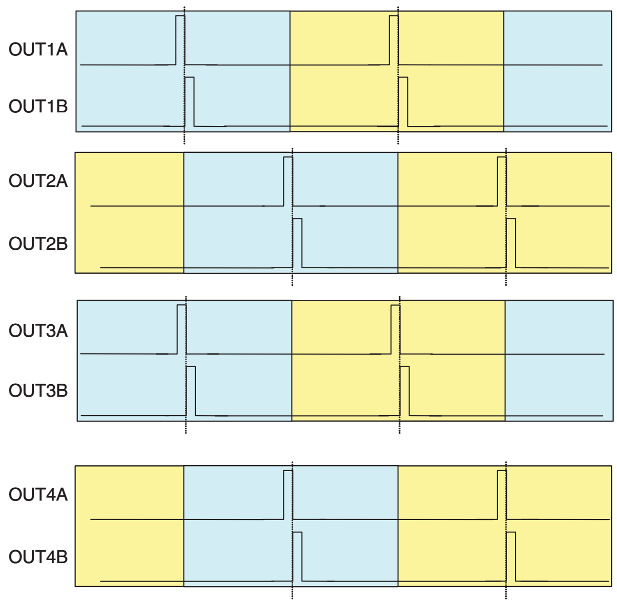
2.0 channels, two full-bridges (OCFG = 00)

- FFX1A -> OUT1A
- FFX1B -> OUT1B
- FFX2A -> OUT2A
- FFX2B -> OUT2B
- FFX3A -> OUT3A
- FFX3B -> OUT3B
- FFX4A -> OUT4A
- FFX4B -> OUT4B
- FFX1A/1B configured as C1B0 (default: ternary)
- FFX2A/2B configured as C2B0 (default: ternary)
- FFX3A/3B configured as C3B0 (default: ternary) line out
- FFX4A/4B configured as C4B0 (default: ternary) line out

On channel 3 line out (LOC bits = 00) the same data as channel 1 processing is sent. On channel 4 line out (LOC bits = 00) the same data as channel 2 processing is sent. In this configuration, neither volume control nor EQ has any effect on channels 3 and 4.

In this configuration the PWM slot phase is the following as shown in *Figure 36*.

Figure 36. 2.0 channels (OCFG = 00) PWM slots



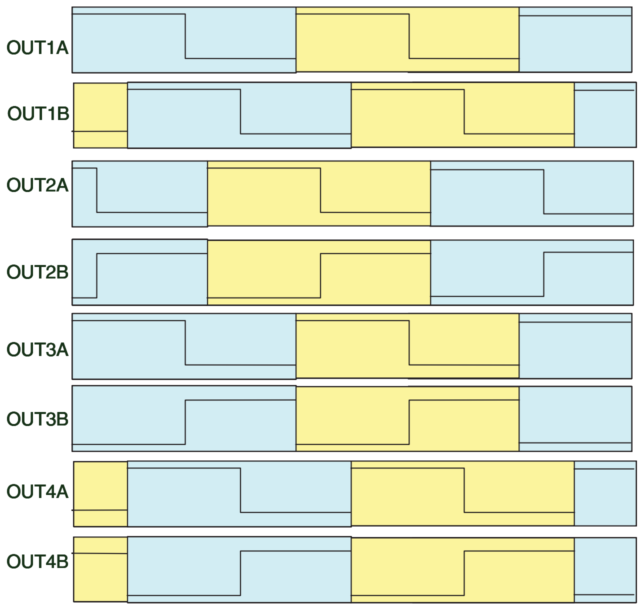
2.1 channels, two half-bridges + one full-bridge (OCFG = 01)

- FFX1A -> OUT1A
- FFX2A -> OUT1B
- FFX3A -> OUT2A
- FFX3B -> OUT2B
- FFX1A -> OUT3A
- FFX1B -> OUT3B
- FFX2A -> OUT4A
- FFX2B -> OUT4B
- FFX1A/1B configured as binary
- FFX2A/2B configured as binary
- FFX3A/3B configured as binary
- FFX4A/4B is not used

In this configuration, channel 3 has full control (volume, EQ, etc…). On OUT3/OUT4 channels channel 1 and channel 2 PWM are replicated.

In this configuration the PWM slot phase is the following as shown in *Figure 37*.

Figure 37. 2.1 channels (OCFG = 01) PWM slots



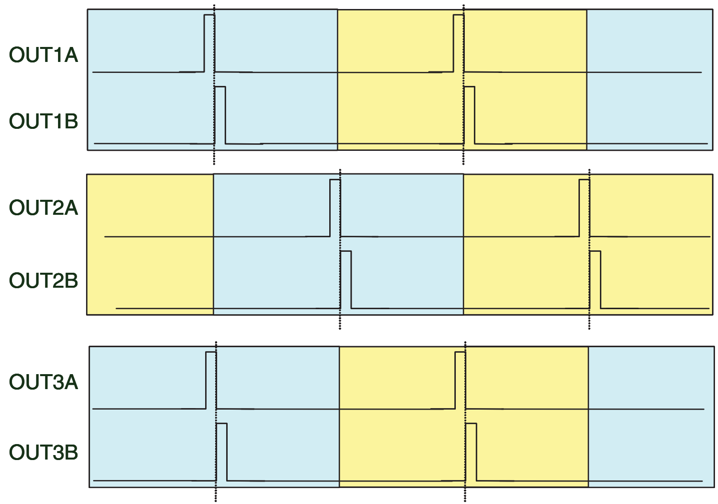
2.1 channels, two full-bridges + one external full-bridge (OCFG = 10)

- FFX1A -> OUT1A
- FFX1B -> OUT1B
- FFX2A -> OUT2A
- FFX2B -> OUT2B
- FFX3A -> OUT3A
- FFX3B -> OUT3B
- EAPD -> OUT4A
- TWARN -> OUT4B
- FFX1A/1B configured as C1B0 (default: ternary)
- FFX2A/2B configured as C2B0 (default: ternary)
- FFX3A/3B configured as C3B0 (default: ternary)
- FFX4A/4B is not used

In this configuration, channel 3 has full control (volume, EQ, etc…). On OUT4 channel the external bridge control signals are muxed.

In this configuration the PWM slot phase is the following as shown in *Figure 38*.

Figure 38. 2.1 channels (OCFG = 10) PWM slots



7.6.2 Invalid input detect mute enable

Table 126. Invalid input detect mute enable

Bit	R/W	RST	Name	Description
2	R/W	1	IDE	Setting of 1 enables the automatic invalid input detect mute

Setting the IDE bit enables this function, which looks at the input I^2S data and automatically mutes if the signals are perceived as invalid.

7.6.3 Binary output mode clock loss detection

Table 127. Binary output mode clock loss detection

Bit	R/W	RST	Name	Description
3	R/W	1	BCLE	Binary output mode clock loss detection enable

This bit detects loss of input MCLK in binary mode and will output 50% duty cycle.

7.6.4 LRCK double trigger protection

Table 128. LRCK double trigger protection

Bit	R/W	RST	Name	Description
4	R/W	1	LDTE	LRCLK double trigger protection enable

This bit actively prevents double triggering of LRCLK.

7.6.5 IC power-down

Table 129. IC power-down

Bit	R/W	RST	Name	Description
7	R/W	1	PWDN	0: IC power-down low-power condition 1: IC normal operation

The PWDN register is used to place the IC in a low-power state. When PWDN is written as 0, the output begins a soft-mute. After the mute condition is reached, EAPD is asserted to power down the power stage, then the master clock to all internal hardware except the I^2C block is gated. This places the IC in a very low power consumption state.

7.6.6 External amplifier power-down

Table 130. External amplifier power-down

Bit	R/W	RST	Name	Description
7	R/W	0	EAPD	0: External power stage power-down active 1: Normal operation

The EAPD register directly disables/enables the internal power circuitry.

When EAPD = 0, the internal power section is placed in a low-power state (disabled). This register also controls the EAPD/FFX4B output pin when OCFG = 10.

7.7 Volume control registers (addr 0x06 - 0x0A)

7.7.1 Mute/line output configuration register

D7	D6	D5	D4	D3	D2	D1	D0
LOC1	LOC0	Reserved	BQBALL	C3M	C2M	C1M	MMUTE
0	0	0	0	0	0	0	0

Table 131. Line output configuration

LOC[1:0]	Line output configuration
00	Line output fixed - no volume, no EQ
01	Line output variable - CH3 volume effects line output, no EQ
10	Line output variable with EQ - CH3 volume effects line output
11	Reserved

Line output is only active when OCFG = 00. In this case LOC determines the line output configuration. The source of the line output is always channel 1 and 2 inputs.

Bit	R/W	RST	Name	Description
4	R/W	0	BQBALL	Global biquad bypass 0: Biquad filters active 1: All the biquad filters are bypassed (pass-through)

Table 132. Mute configuration

Bit	R/W	RST	Name	Description
3	R/W	0	C3M	Channel 3 mute 0 - No mute condition. It is possible to set the channel volume 1 - Channel 3 in hardware mute
2	R/W	0	C2M	Channel 2 mute 0 - No mute condition. It is possible to set the channel volume 1 - Channel 2 in hardware mute

Bit	R/W	RST	Name	Description
1	R/W	0	C1M	Channel 1 mute 0 - No mute condition. It is possible to set the channel volume 1 - Channel 1 in hardware mute
0	R/W	0	MMUTE	Master mute 0 - Normal operation 1 - All channels are in mute condition

7.7.2 Master volume register

D7	D6	D5	D4	D3	D2	D1	D0
MVOL[7:0]							
1	1	1	1	1	1	1	1

7.7.3 Channel 1 volume

D7	D6	D5	D4	D3	D2	D1	D0
CH1VOL[7:0]							
0	1	1	0	0	0	0	0

7.7.4 Channel 2 volume

D7	D6	D5	D4	D3	D2	D1	D0
CH2VOL[7:0]							
0	1	1	0	0	0	0	0

7.7.5 Channel 3 / line output volume

D7	D6	D5	D4	D3	D2	D1	D0
CH3VOL[7:0]							
0	1	1	0	0	0	0	0

The volume structure of the STA381BW consists of individual volume registers for each channel and a master volume register that provides an offset to each channel’s volume setting. The individual channel volumes are adjustable in 0.5 dB steps from +48 dB to -80 dB.

As an example if CH3VOL = 0x00 or +48 dB and MVOL = 0x18 or -12 dB, then the total gain for channel 3 = +36 dB.

The master mute, when set to 1, mutes all channels at once, whereas the individual channel mute (CxM) mutes only that channel. Both the master mute and the channel mutes provide a “soft mute” with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate (approximately 96 kHz).

A “hard (instantaneous) mute” can be obtained by programming a value of 0xFF (255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register, any channel whose total volume is less than -80 dB is muted.

All changes in volume take place at zero-crossings when ZCE = 1 (*Configuration register E (addr 0x04)*) on a per-channel basis as this creates the smoothest possible volume transitions. When ZCE = 0, volume updates occur immediately.

Table 133. Master volume offset as a function of MVOL[7:0]

MVOL[7:0]	Volume offset from channel value
00000000 (0x00)	0 dB
00000001 (0x01)	-0.5 dB
00000010 (0x02)	-1 dB
...	...
01001100 (0x4C)	-38 dB
...	...
11111110 (0xFE)	-127.5 dB
11111111 (0xFF)	Hard master mute

Table 134. Channel volume as a function of CxVOL[7:0]

CxVOL[7:0]	Volume
00000000 (0x00)	+48 dB
00000001 (0x01)	+47.5 dB
00000010 (0x02)	+47 dB
...	...
01011111 (0x5F)	+0.5 dB
01100000 (0x60)	0 dB
01100001 (0x61)	-0.5 dB
...	...
11010111 (0xD7)	-59.5 dB
11011000 (0xD8)	-60 dB
11011001 (0xD9)	-61 dB
11011010 (0xDA)	-62 dB
...	...
11101100 (0xEC)	-80 dB
11101101 (0xED)	Hard channel mute
...	...
11111111 (0xFF)	Hard channel mute

7.8 Audio preset registers (addr 0x0C)

7.8.1 Audio preset register (addr 0x0C)

D7	D6	D5	D4	D3	D2	D1	D0
XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

7.8.2 AM interference frequency switching

Table 135. AM interference frequency switching bits

Bit	R/W	RST	Name	Description
0	R/W	0	AMAME	Audio preset AM enable 0: switching frequency determined by PWMS setting 1: switching frequency determined by AMAM settings

Table 136. Audio preset AM switching frequency selection

AMAM[2:0]	48 kHz/96 kHz input fs	44.1 kHz/88.2 kHz input fs
000	0.535 MHz - 0.720 MHz	0.535 MHz - 0.670 MHz
001	0.721 MHz - 0.900 MHz	0.671 MHz - 0.800 MHz
010	0.901 MHz - 1.100 MHz	0.801 MHz - 1.000 MHz
011	1.101 MHz - 1.300 MHz	1.001 MHz - 1.180 MHz
100	1.301 MHz - 1.480 MHz	1.181 MHz - 1.340 MHz
101	1.481 MHz - 1.600 MHz	1.341 MHz - 1.500 MHz
110	1.601 MHz - 1.700 MHz	1.501 MHz - 1.700 MHz

7.8.3 Bass management crossover

Table 137. Bass management crossover

Bit	R/W	RST	Name	Description
4	R/W	0	XO0	Selects the bass management crossover frequency. A 1^{st}-order high-pass filter (channels 1 and 2) or a 2^{nd}-order low-pass filter (channel 3) at the selected frequency is performed.
5	R/W	0	XO1	
6	R/W	0	XO2	
7	R/W	0	XO3	

Table 138. Bass management crossover frequency

XO[3:0]	Crossover frequency
0000	User-defined
0001	80 Hz
0010	100 Hz
0011	120 Hz
0100	140 Hz
0101	160 Hz
0110	180 Hz
0111	200 Hz
1000	220 Hz
1001	240 Hz
1010	260 Hz
1011	280 Hz
1100	300 Hz
1101	320 Hz
1110	340 Hz
1111	360 Hz

7.9 Channel configuration registers (addr 0x0E - 0x10)

D7	D6	D5	D4	D3	D2	D1	D0
C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VPB	C1EQBP	C1TCB
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VPB	C2EQBP	C2TCB
0	1	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VPB	Reserved	Reserved
1	0	0	0	0	0	0	0

7.9.1 Tone control bypass

Tone control (bass/treble) can be bypassed on a per-channel basis for channels 1 and 2.

Table 139. Tone control bypass

CxTCB	Mode
0	Perform tone control on channel x - normal operation
1	Bypass tone control on channel x

7.9.2 EQ bypass

EQ control can be bypassed on a per-channel basis for channels 1 and 2. If EQ control is bypassed on a given channel, the prescale and all filters (biquads, bass, treble in any combination) are bypassed for that channel.

Table 140. EQ bypass

CxEQBP	Mode
0	Perform EQ on channel x - normal operation
1	Bypass EQ on channel x

7.9.3 Volume bypass

Each channel contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register, then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel.

Table 141. Volume bypass register

CxVBP	Mode
0	Normal volume operations
1	Volume is bypassed

7.9.4 Binary output enable registers

Each individual channel output can be set to output a binary PWM stream. In this mode output A of a channel is considered the positive output and output B is the negative inverse.

Table 142. Binary output enable registers

CxBO	Mode
0	FFX 3-state output - normal operation
1	Binary output

7.9.5 Limiter select

Limiter selection can be made on a per-channel basis according to the channel limiter select bits. CxLS bits are considered in case of dual-band DRC and EQDRC usage (*7.16.1*).

Table 143. Channel limiter mapping as a function of CxLS bits

CxLS[1:0]	Channel limiter mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2

7.9.6 Output mapping

Output mapping can be performed on a per-channel basis according to the CxOM channel output mapping bits. Each input into the output configuration engine can receive data from any of the three processing channel outputs.

Table 144. Channel output mapping as a function of CxOM bits

CxOM[1:0]	Channel x output source from
00	Channel1
01	Channel 2
10	Channel 3

7.10 Tone control register (addr 0x11)

D7	D6	D5	D4	D3	D2	D1	D0
TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0	1	1	1	0	1	1	1

7.10.1 Tone control

Table 145. Tone control boost/cut as a function of BTC and TTC bits

BTC[3:0]/TTC[3:0]	Boost/cut
0000	-12 dB
0001	-12 dB
…	…
0111	-4 dB
0110	-2 dB
0111	0 dB
1000	+2 dB
1001	+4 dB
…	…
1101	+12 dB
1110	+12 dB
1111	+12 dB

7.11 Dynamic control registers (addr 0x12 - 0x15)

7.11.1 Limiter 1 attack/release rate

D7	D6	D5	D4	D3	D2	D1	D0
L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0	1	1	0	1	0	1	0

7.11.2 Limiter 1 attack/release threshold

D7	D6	D5	D4	D3	D2	D1	D0
L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0	1	1	0	1	0	0	1

7.11.3 Limiter 2 attack/release rate

D7	D6	D5	D4	D3	D2	D1	D0
L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0	1	1	0	1	0	1	0

7.11.4 Limiter 2 attack/release threshold

D7	D6	D5	D4	D3	D2	D1	D0
L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0	1	1	0	1	0	0	1

The STA381BW includes two independent limiter blocks (not to be mistaken with the STCompressor^{TM}, for further details about this feature please refer to *Section 4.2*). The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anticlipping mode or to actively reduce the dynamic range for a better listening environment such as a nighttime listening mode which is often needed for DVDs. The two modes are selected via the DRC bit in *Configuration register E (addr 0x04) on page 113*. Each channel can be mapped to either limiter or not mapped, meaning that the channel will clip when 0 dBfs is exceeded. Each limiter looks at the present value of each channel that is mapped to it, selects the maximum absolute value of all these channels, performs the limiting algorithm on that value, and then, if needed, adjusts the gain of the mapped channels in unison.

The limiter attack thresholds are determined by the LxAT registers if the EATHx[7] bits are set to 0, else the thresholds are determined by EATHx[6:0]. It is recommended in anticlipping mode to set this to 0 dBfs, which corresponds to the maximum unclipped output power of an FFX amplifier. Since gain can be added digitally within the STA381BW, it is possible to exceed 0 dBfs or any other LxAT setting. When this occurs, the limiter, when active, automatically starts reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. Gain reduction occurs on a peak-detect algorithm. Setting the EATHx[7] bits to 1 selects the anticlipping mode.

The limiter release thresholds are determined by the LxRT registers if the ERTHx[7] bits are set to 0, else the thresholds are determined by ERTHx[6:0]. Settings the ERTHx[7] bits to 1 automatically selects the anticlipping mode. The release of the limiter, when the gain is again increased, is dependent on an RMS-detect algorithm. The output of the volume/limiter block is passed through an RMS filter. The output of this filter is compared to the release threshold, determined by the release threshold register. When the RMS filter output falls below the release threshold, the gain is again increased at a rate dependent upon the release rate register. The gain can never be increased past its set value and, therefore, the release only occurs if the limiter has already reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range, this is helpful as overlimiting can reduce the dynamic range to virtually zero and cause program material to sound “lifeless”.

In AC mode, the attack and release thresholds are set relative to full-scale. In DRC mode, the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter, and the release threshold is set relative to the maximum volume setting plus the attack threshold.

Figure 39. Basic limiter and volume flow diagram

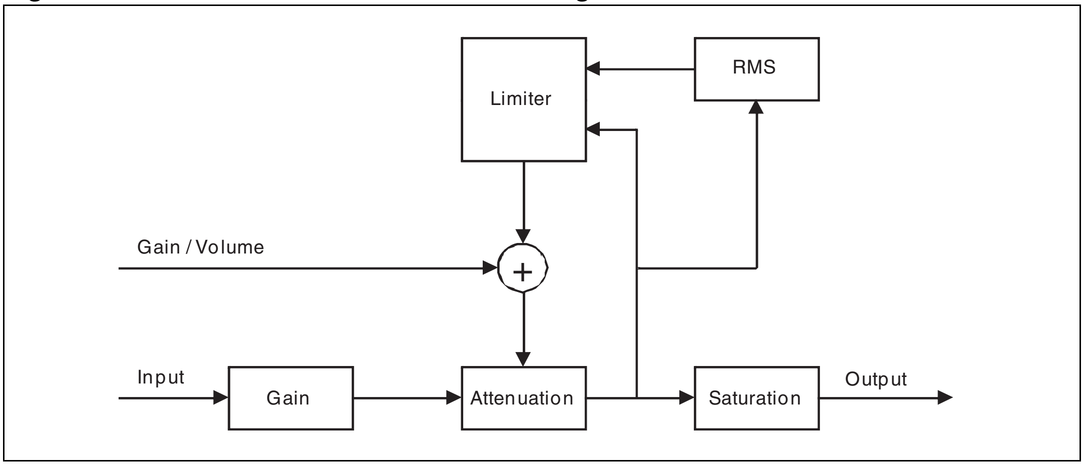


Table 146. Limiter attack rate as a function of LxA bits

LxA[3:0]	Attack rate dB/ms	
0000	3.1584	Fast
0001	2.7072	
0010	2.2560	
0011	1.8048	
0100	1.3536	
0101	0.9024	
0110	0.4512	
0111	0.2256	
1000	0.1504	
1001	0.1123	
1010	0.0902	
1011	0.0752	
1100	0.0645	
1101	0.0564	
1110	0.0501	
1111	0.0451	Slow

Table 147. Limiter release rate as a function of LxR bits

LxR[3:0]	Release rate dB/ms	
0000	0.5116	Fast
0001	0.1370	
0010	0.0744	
0011	0.0499	
0100	0.0360	
0101	0.0299	
0110	0.0264	
0111	0.0208	
1000	0.0198	
1001	0.0172	
1010	0.0147	
1011	0.0137	
1100	0.0134	
1101	0.0117	
1110	0.0110	
1111	0.0104	Slow

Anticlipping mode

Table 148. Limiter attack threshold as a function of LxAT bits (AC mode)

LxAT[3:0]	AC (dB relative to fs)
0000	-12
0001	-10
0010	-8
0011	-6
0100	-4
0101	-2
0110	0
0111	+2
1000	+3
1001	+4
1010	+5
1011	+6
1100	+7
1101	+8
1110	+9
1111	+10

Table 149. Limiter release threshold as a function of LxRT bits (AC mode)

LxRT[3:0]	AC (dB relative to fs)
0000	-∞
0001	-29 dB
0010	-20 dB
0011	-16 dB
0100	-14 dB
0101	-12 dB
0110	-10 dB
0111	-8 dB
1000	-7 dB
1001	-6 dB
1010	-5 dB
1011	-4 dB
1100	-3 dB
1101	-2 dB
1110	-1 dB
1111	-0 dB

Dynamic range compression mode

Table 150. Limiter attack threshold as a function of LxAT bits (DRC mode)

LxAT[3:0]	DRC (dB relative to volume)
0000	-31
0001	-29
0010	-27
0011	-25
0100	-23
0101	-21
0110	-19
0111	-17
1000	-16
1001	-15
1010	-14
1011	-13
1100	-12
1101	-10
1110	-7
1111	-4

Table 151. Limiter release threshold as a function of LxRT bits (DRC mode)

LxRT[3:0]	DRC (db relative to volume + LxAT)
0000	-∞
0001	-38 dB
0010	-36 dB
0011	-33 dB
0100	-31 dB
0101	-30 dB
0110	-28 dB
0111	-26 dB
1000	-24 dB
1001	-22 dB
1010	-20 dB
1011	-18 dB
1100	-15 dB
1101	-12 dB
1110	-9 dB
1111	-6 dB

7.11.5 Limiter 1 extended attack threshold (addr 0x32)

D7	D6	D5	D4	D3	D2	D1	D0
EATHEN1	EATH1[6]	EATH1[5]	EATH1[4]	EATH1[3]	EATH1[2]	EATH1[1]	EATH1[0]
0	0	1	1	0	0	0	0

The extended attack threshold value is determined as follows:

attack threshold = -12 + EATH1 / 4

To enable this feature, the EATHEN1 bit must be set to 1.

7.11.6 Limiter 1 extended release threshold (addr 0x33)

D7	D6	D5	D4	D3	D2	D1	D0
ERTHEN1	ERTH1[6]	ERTH1[5]	ERTH1[4]	ERTH1[3]	ERTH1[2]	ERTH1[1]	ERTH1[0]
0	0	1	1	0	0	0	0

The extended release threshold value is determined as follows:

release threshold = -12 + ERTH1 / 4

To enable this feature, the ERTHEN2 bit must be set to 1.

7.11.7 Limiter 2 extended attack threshold (addr 0x34)

D7	D6	D5	D4	D3	D2	D1	D0
EATHEN2	EATH2[6]	EATH2[5]	EATH2[4]	EATH2[3]	EATH2[2]	EATH2[1]	EATH2[0]
0	0	1	1	0	0	0	0

The extended attack threshold value is determined as follows:

attack threshold = -12 + EATH2 / 4

To enable this feature, the EATHEN2 bit must be set to 1.

7.11.8 Limiter 2 extended release threshold (addr 0x35)

D7	D6	D5	D4	D3	D2	D1	D0
ERTHEN2	ERTH2[6]	ERTH2[5]	ERTH2[4]	ERTH2[3]	ERTH2[2]	ERTH2[1]	ERTH2[0]
0	0	1	1	0	0	0	0

The extended release threshold value is determined as follows:

release threshold = -12 + ERTH2 / 4

To enable this feature, the ERTHEN2 bit must be set to 1.

Note: Attack/release threshold step is 0.125 dB in the range -12 dB to 0 dB.

7.12 User-defined coefficient control registers (addr 0x16 - 0x26)

7.12.1 Coefficient address register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0	0	0	0	0	0	0	0

7.12.2 Coefficient b1 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

7.12.3 Coefficient b1 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0	0	0	0	0	0	0	0

7.12.4 Coefficient b1 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0	0	0	0	0	0	0	0

7.12.5 Coefficient b2 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0	0	0	0	0	0	0	0

7.12.6 Coefficient b2 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0	0	0	0	0	0	0	0

7.12.7 Coefficient b2 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0	0	0	0	0	0	0	0

7.12.8 Coefficient a1 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

7.12.9 Coefficient a1 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0	0	0	0	0	0	0	0

7.12.10 Coefficient a1 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0	0	0	0	0	0	0	0

7.12.11 Coefficient a2 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0	0	0	0	0	0	0	0

7.12.12 Coefficient a2 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0	0	0	0	0	0	0	0

7.12.13 Coefficient a2 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0	0	0	0	0	0	0	0

7.12.14 Coefficient b0 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0	0	0	0	0	0	0	0

7.12.15 Coefficient b0 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0	0	0	0	0	0	0	0

7.12.16 Coefficient b0 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0	0	0	0	0	0	0	0

7.12.17 Coefficient write/read control register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				RA	R1	WA	W1
0				0	0	0	0

Coefficients for user-defined EQ, mixing, scaling, bass management and STCompressor^{TM} (see *Section 4.2*) are handled internally in the STA381BW via RAM. Access to this RAM is available to the user via an I^2C register interface. A collection of I^2C registers are dedicated to this function. One contains a coefficient base address, five sets of three store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the write/read of the coefficient(s) to/from RAM.

Note: The read and write operation on RAM coefficients works only if LRCKI (pin 29) is switching.

Reading a coefficient from RAM

1. Write 6 bits of the address to I^{2}C register 0x16.
2. Write 1 to the R1 bit in I^{2}C address 0x26.
3. Read the top 8 bits of the coefficient in I^{2}C address 0x17.
4. Read the middle 8 bits of the coefficient in I^{2}C address 0x18.
5. Read the bottom 8 bits of the coefficient in I^{2}C address 0x19.

Reading a set of coefficients from RAM

1. Write 6 bits of the address to I^{2}C register 0x16.
2. Write 1 to the RA bit in I^{2}C address 0x26.
3. Read the top 8 bits of the coefficient in I^{2}C address 0x17.
4. Read the middle 8 bits of the coefficient in I^{2}C address 0x18.
5. Read the bottom 8 bits of the coefficient in I^{2}C address 0x19.
6. Read the top 8 bits of coefficient b2 in I^{2}C address 0x1A.
7. Read the middle 8 bits of coefficient b2 in I^{2}C address 0x1B.
8. Read the bottom 8 bits of coefficient b2 in I^{2}C address 0x1C.
9. Read the top 8 bits of coefficient a1 in I^{2}C address 0x1D.
10. Read the middle 8 bits of coefficient a1 in I^{2}C address 0x1E.
11. Read the bottom 8 bits of coefficient a1 in I^{2}C address 0x1F.
12. Read the top 8 bits of coefficient a2 in I^{2}C address 0x20.
13. Read the middle 8 bits of coefficient a2 in I^{2}C address 0x21.
14. Read the bottom 8 bits of coefficient a2 in I^{2}C address 0x22.
15. Read the top 8 bits of coefficient b0 in I^{2}C address 0x23.
16. Read the middle 8 bits of coefficient b0 in I^{2}C address 0x24.
17. Read the bottom 8 bits of coefficient b0 in I^{2}C address 0x25.

Writing a single coefficient to RAM

1. Write 6 bits of the address to I^{2}C register 0x16.
2. Write the top 8 bits of the coefficient in I^{2}C address 0x17.
3. Write the middle 8 bits of the coefficient in I^{2}C address 0x18.
4. Write the bottom 8 bits of the coefficient in I^{2}C address 0x19.
5. Write 1 to the W1 bit in I^{2}C address 0x26.

Writing a set of coefficients to RAM

1. Write 6 bits of the starting address to I^2C register 0x16.
2. Write the top 8 bits of coefficient b1 in I^2C address 0x17.
3. Write the middle 8 bits of coefficient b1 in I^2C address 0x18.
4. Write the bottom 8 bits of coefficient b1 in I^2C address 0x19.
5. Write the top 8 bits of coefficient b2 in I^2C address 0x1A.
6. Write the middle 8 bits of coefficient b2 in I^2C address 0x1B.
7. Write the bottom 8 bits of coefficient b2 in I^2C address 0x1C.
8. Write the top 8 bits of coefficient a1 in I^2C address 0x1D.
9. Write the middle 8 bits of coefficient a1 in I^2C address 0x1E.
10. Write the bottom 8 bits of coefficient a1 in I^2C address 0x1F.
11. Write the top 8 bits of coefficient a2 in I^2C address 0x20.
12. Write the middle 8 bits of coefficient a2 in I^2C address 0x21.
13. Write the bottom 8 bits of coefficient a2 in I^2C address 0x22.
14. Write the top 8 bits of coefficient b0 in I^2C address 0x23.
15. Write the middle 8 bits of coefficient b0 in I^2C address 0x24.
16. Write the bottom 8 bits of coefficient b0 in I^2C address 0x25.
17. Write 1 to the WA bit in I^2C address 0x26.

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side effects. When using this technique, the 6-bit address specifies the address of the biquad b1 coefficient (for example, 0, 5, 10, 20, 35 decimal), and the STA381BW generates the RAM addresses as offsets from this base value to write the complete set of coefficient data.

7.12.18 User-defined EQ

The STA381BW can be programmed for four EQ filters (biquads) per each of the two input channels. The biquads use the following equation:

$$Y[n] = 2 * (b_0 / 2) * X[n] + 2 * (b_1 / 2) * X[n-1] + b_2 * X[n-2] - 2 * (a_1 / 2) * Y[n-1] - a_2 * Y[n-2]$$
$$= b_0 * X[n] + b_1 * X[n-1] + b_2 * X[n-2] - a_1 * Y[n-1] - a_2 * Y[n-2]$$

where Y[n] represents the output and X[n] represents the input. Multipliers are 24-bit signed fractional multipliers, with coefficient values in the range of 0x800000 (-1) to 0x7FFFFF (0.9999998808).

Coefficients stored in the user-defined coefficient RAM are referenced in the following manner:

CxHy0 = b_1 / 2

CxHy1 = b_2

CxHy2 = -a_1 / 2

CxHy3 = -a_2

CxHy4 = b_0 / 2

where x represents the channel and y the biquad number. For example, C2H41 is the b_2 coefficient in the fourth biquad for channel 2.

Additionally, the STA381BW can be programmed for a high-pass filter (processing channels 1 and 2) and a low-pass filter (processing channel 3) to be used for bass management crossover when the XO setting is 000 (user-defined). Both of these filters, when defined by the user (rather than using the preset crossover filters), are second order filters that use the biquad equation given above. They are loaded into the C12H0-4 and C3Hy0-4 areas of RAM noted in *Table 150*.

Channel 1 and channel 2 biquads use by default the extended coefficient range (-4, +4); Xover filters use only the standard coefficients range (-1, +1).

By default, all user-defined filters are pass-through where all coefficients are set to 0, except the channel 1 and 2 b_0/2 coefficient which is set to 0x100000 (representing 0.5) and xover b_0/2 coefficient which is set to 0x400000 (representing 0.5).

7.12.19 Pre-scale

The STA381BW provides a multiplication for each input channel for the purpose of scaling the input prior to EQ. This pre-EQ scaling is accomplished by using a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. The scale factor for this multiplication is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass management. All channels can use the channel-1 pre-scale factor by setting the biquad link bit. By default, all pre-scale factors are set to 0x7FFFFF.

7.12.20 Post-scale

The STA381BW provides one additional multiplication after the last interpolation stage and the distortion compensation on each channel. This post-scaling is accomplished by using a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. The scale factor for this multiplication is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass management. This post-scale factor can be used in conjunction with an ADC-equipped microcontroller to perform power-supply error correction. All channels can use the channel-1 post-scale factor by setting the post-scale link bit. By default, all post-scale factors are set to 0x7FFFFF. When line output is being used, channel-3 post-scale will affect both channels 3 and 4.

Table 152. RAM block for biquads, mixing, scaling and bass management

Index (decimal)	Index (hex)	Description	Coefficient	Default
0	0x00	Channel 1 - Biquad 1	C1H10(b1/2)	0x000000
1	0x01		C1H11(b2)	0x000000
2	0x02		C1H12(a1/2)	0x000000
3	0x03		C1H13(a2)	0x000000
4	0x04		C1H14(b0/2)	0x400000
5	0x05	Channel 1 - Biquad 2	C1H20	0x000000
...	...	...	...	...
19	0x13	Channel 1 - Biquad 4	C1H44	0x400000
20	0x14	Channel 2 - Biquad 1	C2H10	0x000000
21	0x15		C2H11	0x000000
...	...	...	...	...
39	0x27	Channel 2 - Biquad 4	C2H44	0x400000
40	0x28	Channel 1/2 - Biquad 5 for XO = 000 High-pass 1st order filter for XO≠000	C12H0(b1/2)	0x000000
41	0x29		C12H1(b2)	0x000000
42	0x2A		C12H2(a1/2)	0x000000
43	0x2B		C12H3(a2)	0x000000
44	0x2C		C12H4(b0/2)	0x400000
45	0x2D	Channel 3 - Biquad for XO = 000 Low-pass 2nd order filter for XO≠000	C3H0(b1/2)	0x000000
46	0x2E		C3H1(b2)	0x000000
47	0x2F		C3H2(a1/2)	0x000000
48	0x30		C3H3(a2)	0x000000
49	0x31		C3H4(b0/2)	0x400000
50	0x32	Channel 1 - Pre-Scale	C1PreS	0x7FFFFF
51	0x33	Channel 2 - Pre-Scale	C2PreS	0x7FFFFF
52	0x34	Channel 1 - Post-Scale	C1PstS	0x7FFFFF
53	0x35	Channel 2 - Post-Scale	C2PstS	0x7FFFFF
54	0x36	Channel 3 - Post-Scale	C3PstS	0x7FFFFF
55	0x37	Reserved	Reserved	0x5A9DF7
56	0x38	Channel 1 - Mix 1	C1MX1	0x7FFFFF
57	0x39	Channel 1 - Mix 2	C1MX2	0x000000
58	0x3A	Channel 2 - Mix 1	C2MX1	0x000000
59	0x3B	Channel 2 - Mix 2	C2MX2	0x7FFFFF
60	0x3C	Channel 3 - Mix 1	C3MX1	0x400000
61	0x3D	Channel 3 - Mix 2	C3MX2	0x400000
62	0x3E	UNUSED		
63	0x3F	UNUSED		

7.13 Fault-detect recovery constant registers (addr 0x2B - 0x2C)

D7	D6	D5	D4	D3	D2	D1	D0
FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0	0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0	0	0	0	1	1	0	0

The FDRC bits specify the 16-bit fault-detect recovery time delay. When FAULT is asserted, the TRISTATE output is immediately asserted low and held low for the time period specified by this constant. A constant value of 0x0001 in this register is approximately 0.083 ms. The default value of 0x300C gives approximately 1 sec.

0x0000 is a reserved value.

7.14 Device status register (addr 0x2D)

D7	D6	D5	D4	D3	D2	D1	D0
PLLUL	FAULT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This read-only register provides fault and thermal-warning status information from the power control block. Logic value 1 for faults or warning means normal state. Logic 0 means a fault or warning detected on power bridge. The PLLUL = 1 means that the PLL is not locked.

Table 153. Status register bits

Bit	R/W	RST	Name	Description
7	R	-	PLLUL	0: PLL locked 1: PLL not locked
6	R	-	FAULT	0: fault detected on power bridge 1: normal operation

7.15 EQ coefficients configuration register (addr 0x31)

D7	D6	D5	D4	D3	D2	D1	D0
XOB	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0	0	0	0	0	0	0	0

The XOB bit can be used to bypass the crossover filters. Logic 1 means that the function is not active. In this case, the high-pass crossover filter works as a pass-through on the data path (b=0, all the other coefficients at logic 0) while the low-pass filter is configured to have zero signal on channel 3 data processing (all the coefficients are at logic 0).

7.16 Extended configuration register (addr 0x36)

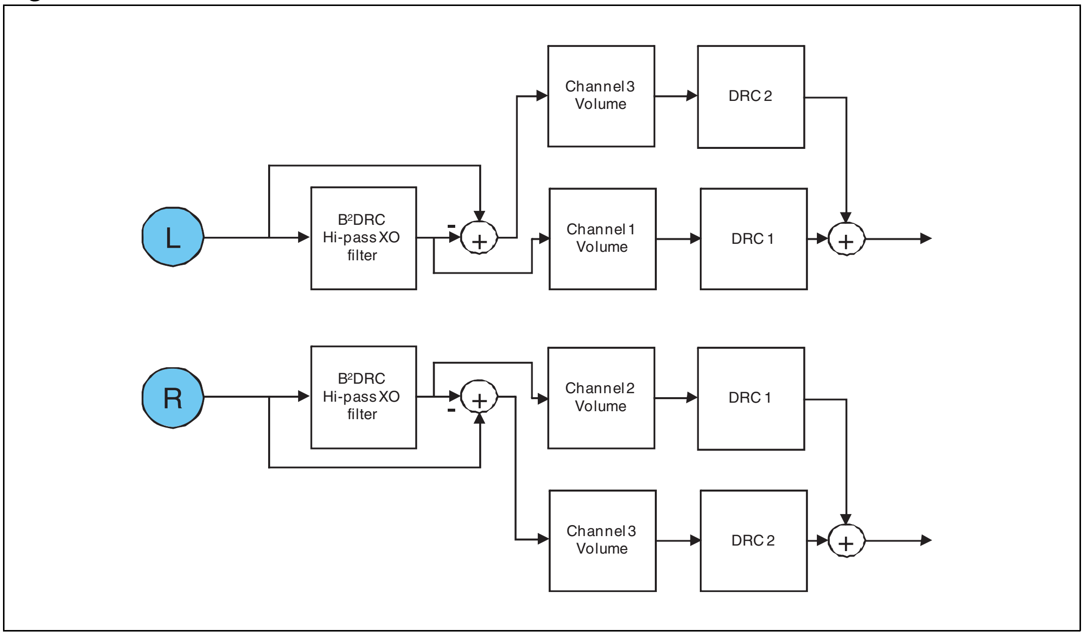
D7	D6	D5	D4	D3	D2	D1	D0
MDRCE	Reserved	PS48DB	XAR1	XAR2	BQ5	BQ6	BQ7
0	0	0	0	0	0	0	0

The extended configuration register provides access to B^2DRC and biquad 5, 6 and 7.

7.16.1 Dual-band DRC

The STA381BW device provides a dual-band DRC (B^2DRC) on the left and right channel data path, as depicted in *Figure 40*. The dual-band DRC is activated by setting MDRCE = 1.

Figure 40. B^2DRC scheme



The low-frequency information (LFE) is extracted from the left and right channels, removing the high frequencies using a programmable biquad filter, and then computing the difference with the original signal. Limiter 1 (DRC1) is then used to control the amplitude of the left/right high-frequency components, while limiter 2 (DRC2) is used to control the low-frequency components (see *Chapter 7.11*).

The cutoff frequency of the high-pass filters can be user-defined, XO[3:0] = 0, or selected from the pre-defined values.

DRC1 and DRC2 are then used to independently limit L/R high frequencies and LFE channel amplitude (see *Chapter 7.11*) as well as their volume control. To be noted that, in this configuration, the dedicated channel 3 volume control can actually act as a bass-boost enhancer as well (0.5 dB/step resolution).

The processed LFE channel is then recombined with the L and R channels in order to reconstruct the 2.0 output signal.

Sub-band decomposition

The sub-band decomposition for B^2DRC can be configured specifying the cutoff frequency. The cutoff frequency can be programmed in two ways, using the XO bits in register 0x0C, or using the "user programmable" mode (coefficients stored in RAM addresses 0x28 to 0x31).

For the user-programmable mode, use the formulas below to compute the high-pass filters:

b0 = (1 + alpha) / 2	a0 = 1
b1 = -(1 + alpha) / 2	a1 = -alpha
b2 = 0	a2 = 0

where alpha = $(1-\sin(\omega_0))/\cos(\omega_0)$, and ω_0 is the cutoff frequency.

A first-order filter is suggested to guarantee that for every ω_0 the corresponding low-pass filter obtained as difference (as shown in *Figure 24*) will have a symmetric (relative to the HP filter) frequency response, and the corresponding recombination after the DRC has low ripple. Second-order filters can be used as well, but in this case the filter shape must be carefully chosen to provide good low-pass response and minimum ripple recombination. For second-order filters, it is not possible to give a closed formula to get the best coefficients, but empirical adjustment should be done.

DRC settings

The DRC blocks used by B^2DRC are the same as those described in *Chapter 7.11*. B^2DRC configure automatically the DRC blocks in anticlipping mode. Attack and release thresholds can be selected using registers 0x32, 0x33, 0x34, 0x35, while attack and release rates are configured by registers 0x12 and 0x14.

Band downmixing

The low-frequency band is down-mixed to the left and right channels at the B^2DRC output. Channel volume can be used to weight the bands recombination to fine-tune the overall frequency response.

7.16.2 Extended post-scale range

Table 154. Extended post-scale range

PS48DB	Mode
0	Post-scale value is applied as defined in coefficient RAM
1	Post-scale value is applied with +48 dB offset with respect to the coefficient RAM value

Post-scale is an attenuation by default. When PS48DB is set to 1, a 48-dB offset is applied to the coefficient RAM value, so post-scale can act as a gain too.

7.16.3 Extended attack rate

The attack rate shown in *Table 146* can be extended to provide up to an 8 dB/ms attack rate on both limiters.

Table 155. Extended attack rate, limiter 1

XAR1	Mode
0	Limiter1 attack rate is configured using *Table 146*
1	Limiter1 attack rate is 8 dB/ms

Table 156. Extended attack rate, limiter 2

XAR2	Mode
0	Limiter2 attack rate is configured using *Table 146*
1	Limiter2 attack rate is 8 dB/ms

7.16.4 Extended BIQUAD selector

Bass and treble controls can be configured as user-defined filters when the equalization coefficients link is activated (BQL = 1) and the corresponding BQx bit is set to 1.

Table 157. Extended biquad selector, biquad 5

BQ5	Mode
0	Reserved
1	User-defined biquad 5 coefficients are selected

Table 158. Extended biquad selector, biquad 6

BQ6	Mode
0	Pre-set bass filter selected as per *Table 145*
1	User-defined biquad 6 coefficients are selected

Table 159. Extended biquad selector, biquad 7

BQ7	Mode
0	Pre-set treble filter selected as per *Table 145*
1	User-defined biquad 7 coefficients are selected

When filters from the 5th to 7th are configured as user-programmable, the corresponding coefficients are stored respectively in addresses 0x20-0x24 (BQ5), 0x25-0x29 (BQ6), 0x2A-0x2E (BQ7) as given in *Table 152*.

Note: BQx bits are ignored if BQL = 0 or if DEMP = 1 (relevant for BQ5) or CxTCB = 1 (relevant for BQ6 and BQ7).

7.17 EQ soft volume configuration registers (addr 0x37 - 0x38)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	SVUPE	SVUP[4]	SVUP[3]	SVUP[2]	SVUP[1]	SVUP[0]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	SVDWE	SVDW4]	SVDW[3]	SVDW[2]	SVDW[1]	SVDW[0]
0	0	0	0	0	0	0	0

The soft volume update has a fixed rate by default. Using register 0x37 and 0x38 it is possible to override the default behavior, allowing different volume change rates.

It is also possible to independently define the fade-in (volume is increased) and fade-out (volume is decreased) rates according to the desired behavior.

Table 160. Soft volume update enable, increase

SVUPE	Mode
0	When volume is increased, use the default rate
1	When volume is increased, use the rates defined by SVUP[4:0].

When SVUPE = 1 the volume-up rate is defined by the SVUP[4:0] bits according to the following formula:

volume-up rate = 48 / (N + 1) dB/ms

where N is the SVUP[4:0] value.

Table 161. Soft volume update enable, decrease

SVDWE	Mode
0	When volume is decreased, use the default rate
1	When volume is decreased, use the rates defined by SVDW[4:0].

When SVDWE = 1 the volume-down rate is defined by the SVDW[4:0] bits according to the following formula:

volume-down rate = 48 / (N + 1) dB/ms

where N is the SVDW[4:0] value.

Note: For volume-down rates greater than 6 dB/msec it is recommended to disable the CPWMEN bit and ZCE bit in order to avoid any audible pop noise.

7.18 Extra volume resolution configuration registers (address 0x3F; 0x40)

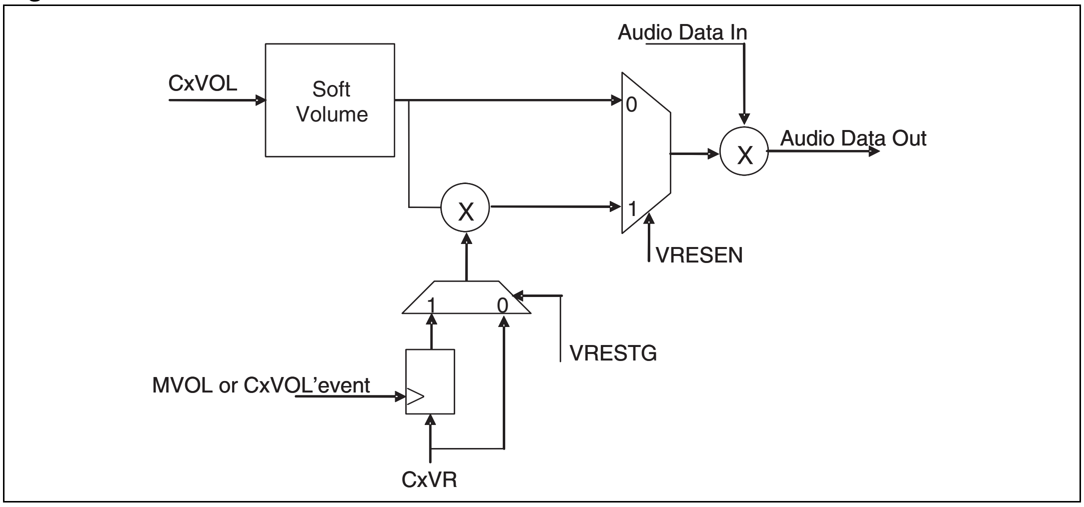
D7	D6	D5	D4	D3	D2	D1	D0
VRESEN	VRESTG	C3VR[1]	C3VR[0]	C2VR[1]	C2VR[0]	C1VR[1]	C1VR[0]
1	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	MVR[1]	MVR[0]
0	0	0	0	0	0	0	0

Extra volume resolution allows fine volume tuning by steps of 0.125 dB.

The feature is enabled when VRESEN=1, as depicted in *Figure 41*. The overall channel volume in this case will be CxVol+CxVR (in dB), while the master volume will be MVOL+MVR (in dB).

Figure 41. Extra resolution volume scheme



If VRESEN = 0 the channel volume will be defined only by the CxVol registers.

Fine tuning steps can be set according to the following table for channels 1, 2,3, and master volume.

Table 162. Volume fine-tuning steps

CxVR/MVR	Mode
00	0 dB
01	-0.125 dB
10	-0.25 dB
11	-0.375 dB

Two different behaviors can be configured by the VRESTG bit.

If VRESTG='0' the CxVR contribution will be applied immediately after the corresponding I^2C bits are written.

If VRESTG='1' the CxVR bits will be effective on channel volume only after the corresponding CxVol register or master volume register is written (even to the previous values).

Table 163. Extra volume resolution enable

VRESEN	VRESTG	Mode
0	0	Extra volume resolution disabled
0	1	Extra volume resolution disabled
1	0	Fine volume tuning enabled and applied immediately
1	1	Fine volume tuning enabled and applied when master or channel volume is updated

7.19 PLL configuration registers (address 0x41; 0x42; 0x43; 0x44; 0x45; 0X46)

D7	D6	D5	D4	D3	D2	D1	D0
PLL_FRAC[15:8]							
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
PLL_FRAC[7:0]							
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
PLL_DITH[1:0]		PLL_NDIV[5:0]					
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
PLL_DPD	PLL_FCT	PLL_STB	PLL_STBBYP	PLL_IDIV(3:0)			
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	PLL_DIRP	PLL_PWD	PLL_BYP	OSC_PD	Reserved	BOOST32K
0	0	0	0	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	BYPSTATE	PDSTATE	OSCOK	LOWCK
NA	NA	NA	NA	NA	NA	NA	NA

By default the STA381BW is able to configure the embedded PLL automatically depending on the MCS bits (reg 0x00). For certain applications and to provide flexibility to the user, a manual PLL configuration can be used (setting PLL_DIRP to '1').

The output PLL frequency formula is:

$$Fin \times \left(\frac{(NDIV)}{(IDIV+1)} + \left(\frac{FRAC}{65536}\right)\right)$$

where Fin is the input clock frequency from the pad.

Table 164. PLL factors

PLL parameter	Min	Max
FRAC	0	65535
IDIV	0	3
NDIV	5	55

Table 165. PLL register 0x43 bits

Bit	R/W	RST	Name	Description
7	R/W	0	PLL_DITH(1:0)	'00': PLL clock dithering disabled '01': PLL clock dithering enabled (triangular)) '10': PLL clock dithering enabled (rectangular) '11': Reserved
6	R/W	0		
5	R/W	0	NDIV	PLL loop divider
4	R/W	0		
3	R/W	0		
2	R/W	0		
1	R/W	0		
0	R/W	0		

Table 166. PLL register 0x44 bits

Bit	R/W	RST	Name	Description
7	R/W	0	PLL_DPD	'0': any PLL dividers change is implemented via PLL power-down '1': PLL divider change will happen without PLL power-down
6	R/W	0	PLL_FCT	'0': PLL use integer ratio '1': PLL use fractional ratio
5	R/W	0	PLL_STB	PLL synchronous divider changes strobe
4	R/W	0	PLL_STBBYP	'0': PLL_STB is active '1': PLL_STB control is bypassed
3	R/W	0	PLL_IDIV (3:0)	Input PLL divider
2	R/W	0		
1	R/W	0		
0	R/W	0		

Table 167. PLL register 0x45 bits

Bit	R/W	RST	Name	Description
5	R/W	0	PLL_DIRP	'0': PLL configuration is determined by MCS bits '1': PLL configuration is determined by FRAC, IDIV and NDIV
4	R/W	0	PLL_PWD	'0': PLL normal behavior '1': PLL is in power-down mode
3	R/W	0	PLL_BYP	'0': sys clock is from PLL '1': sys clock is from external pin (PLL is bypassed)
2	R/W	0	OSC_PD	'0': Normal behavior '1': Internal oscillator is in power-down
0	R/W	0	BOOST32K	'0': Input oversampling selected by IR bits '1': Input oversampling is selected x3

Table 168. PLL register 0x46 bits

Bit	R/W	RST	Name	Description
3	R		BYPSTATE	PLL bypass state
2	R		PDSTATE	PLL PD state
1	R		OSCOK	OSCI locked
0	R		LOWCK	Clock input frequency check

7.20 Short-circuit protection mode registers SHOK (address 0x47)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	GNDSH	VCCSH	OUTSH
NA	NA	NA	NA	NA	NA	NA	NA

The following power bridge pins short-circuit protections are implemented in the STA381BW:

- OUTxx vs GNDx
- OUTxx vs VCCx
- OUT1B vs OUT2A

The protection is enabled when reg. 0x4C bit 0 (SHEN) is set to '1'. The protection will check the short-circuit when the EAPD bit is toggled from '0' to '1' (i.e. the power bridge is switched on), and only if the test passes (no short) does the power bridge leave the tristate condition.

Register 0x47 (read-only registers) will give more information about the detected short type.

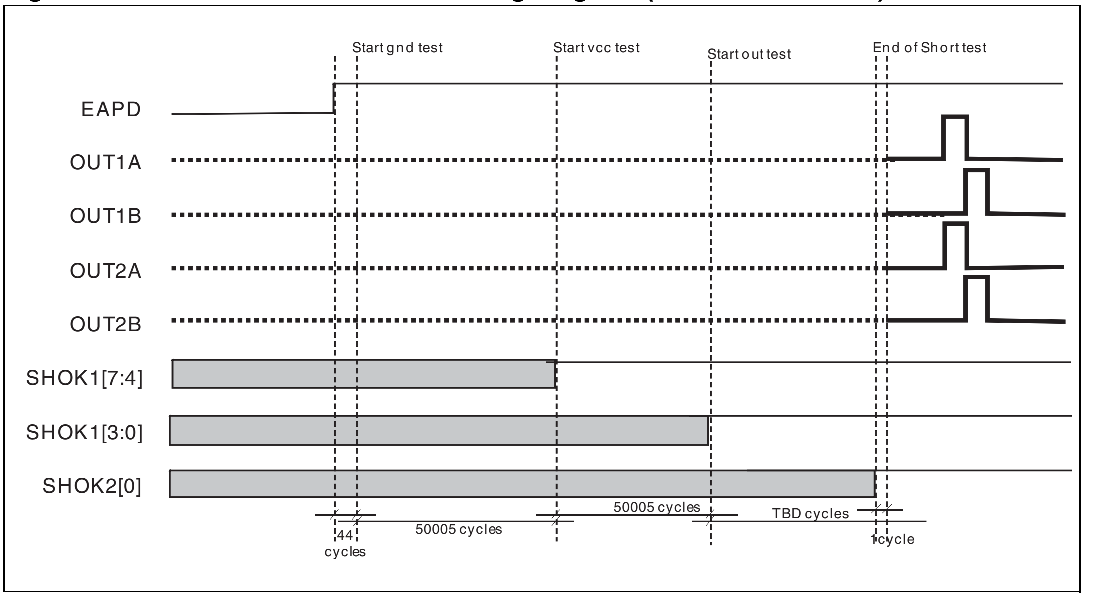
GNDSH equal to '0' means that OUTxx is shorted to ground, while the same value on VCCSH means that OUTxx is shorted to Vcc, finally OUTSH='0' means that OUT1B is shorted to OUT2A.

To be noted that once the check is performed, and the tristate released, the short protection is not active anymore until the next EAPD 0->1 toggling which means that shorts that happened during normal operation cannot be detected.

To be noted that register 0x47 is meaningful only after the EAPD bit is set to ‘1’ at least once.

The short-circuit protections implemented are effective only in BTL configuration, and they must not be activated if a single ended-application scheme is needed.

Figure 42. Short-circuit detection timing diagram (no short detected)



In *Figure 42* the short protection timing diagram is shown. The time information is expressed in clock cycles, where the clock frequency is defined as in section *7.1.1*. The gray color is used for the SHOKx bits to indicate that the bits are carrying the status of the previous EAPD 0->1 toggling (to be noted that after reset this state is meaningless since no EAPD transition occurs). GND-related SHOK bits are updated as soon as the gnd test is completed, VCC bits are updated after the vcc test is completed, and the SOUT bit is updated after the shorted output test is completed. The gnd test, vcc test and output test are always run (if the SHEN bit active and EAPD is toggled to ‘1’), and only if both tests are successful (no short) do the bridge outputs leave the tristate (indicated by dotted lines in the figure). If one of the three tests (or all) fail, the power bridge outputs are kept in tristate until the procedure is restarted with a new EAPD toggling.

In this figure EAPD is intended to be bit 7 of register 0x05.

7.21 Extended coefficient range up to -4...4 (address 0x49, 0x4A)

D7	D6	D5	D4	D3	D2	D1	D0
CEXT_B4[1]	CEXT_B4[0]	CEXT_B3[1]	CEXT_B3[0]	CEXT_B2[1]	CEXT_B2[0]	CEXT_B1[1]	CEXT_B1[0]
1	0	1	0	1	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	CEXT_B7[1]	CEXT_B7[0]	CEXT_B6[1]	CEXT_B6[0]	CEXT_B51]	CEXT_B5[0]
0	0	1	0	1	0	1	0

Biquads from 1 to 7 have in the STA381BW the possibility to extend the coefficient range from [-1,1) to [-4..4) which allows the implementation of high-shelf filters that may require a coefficient dynamic greater in absolute value than 1.

Three ranges are available, [-1;1) [-2;2) [-4;4). By default, the extended range is activated Each biquad has its independent setting according to the following table.

Table 169. Coefficients extended range configuration

CEXT_Bx[1]	CEXT_Bx[0]	Range
0	**0**	[-1;1)
0	**1**	[-2;2)
1	**0**	[-4;4)
1	**1**	**Reserved**

In this case the user can decide, for each filter stage, the right coefficients range. Note that for a given biquad, the same range will be applied to the left and right (channel 1 and channel 2).

Crossover biquad does not have the availability of this feature, maintaining the [-1;1) range unchanged.

7.22 Miscellaneous registers (address 0x4B, 0x4C)

D7	D6	D5	D4	D3	D2	D1	D0
RPDNEN		BRIDGOFF			CPWMEN	reserved	
0	1	1	0	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
LPDP	LPD	LPDE	PNDLSL[2]	PNDLSL[1]	PNDLSL[0]	reserved	SHEN
0	1	0	0	1	1	0	0

7.22.1 Rate power-down enable (RPDNEN) bit (address 0x4B, bit D7)

In the STA381BW, by default, the power-down pin and I^2C power-down act on mute commands to perform the fade-out. This default can be changed so that the fade-out can be started using master volume. The RPDNEN bit, when set, activates this feature.

7.22.2 Bridge immediately off (BRIDGOFF) bit (address 0x4B, bit D5)

A fade-out procedure is started in the STA381BW once the PWDN function is enabled, and after 13 million clock cycles (PLL internal frequency) the bridge is put in power-down (tristate mode). There is also the possibility to change this behavior so that the power bridge will be switched off immediately after the PWDN pin is tied to ground, without waiting for the 13 million clock cycles. The BRIDGOFF bit, when set, activates this function. Obviously the immediate power-down will generate a pop noise at the output, therefore this procedure must be used only in case pop noise is not relevant in the application. Note that this feature works only for hardware PWDN assertion and not for a power-down applied through the IIC interface. Refer to *Section 7.22.5* if programming a different number of clock cycles is needed.

7.22.3 Channel PWM enable (CPWMEN) bit (address 0x4B, bit D2)

This bit, when set, activates a mute output in case the volume reaches a value lower than -76 dBFS.

7.22.4 External amplifier hardware pin enabler (LPDP, LPD LPDE) bits (address 0x4C, bit D7, D6, D5)

Pin 42 (INTLINE), normally indicating a fault condition, using the following 3 register settings, can be reconfigured as hardware pin enabler for an external headphone or line amplifier.

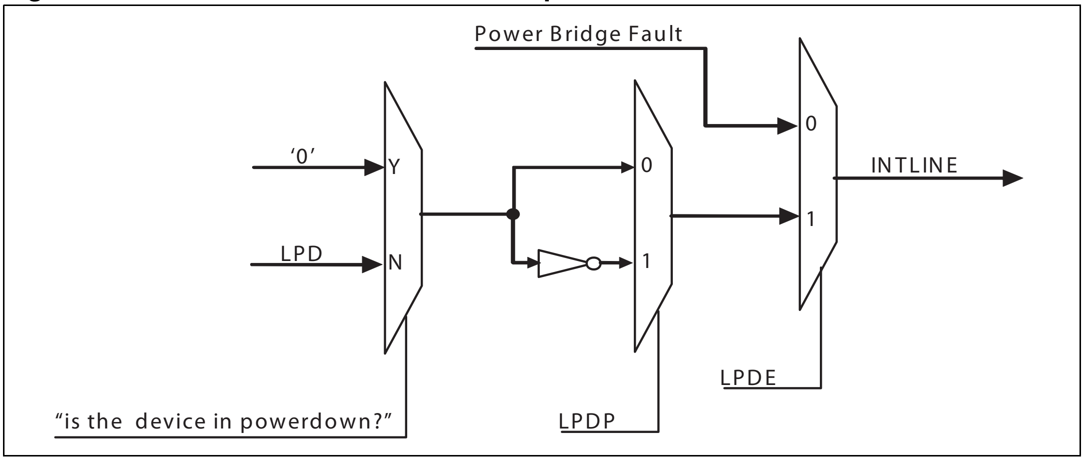
In particular the LPDE bit, when set, activates this function. Accordingly, the LPD value (0 or 1) is exported on pin 42 and in case of power-down assertion, pin 42 is tied to LPDP.

The LPDP bit, when set, negates the value programmed as the LPD value, refer to the following table.

Table 170. External amplifier enabler configuration bits

LPDP	LPD	LPDE	Pin 42 output
x	x	0	INT_LINE
0	0	1	0
0	1	1	1
1	0	1	1
1	1	1	0

Figure 43. Alternate function for INTLINE pin



7.22.5 Power-down delay selector (PNDLSL[2:0]) bits (address 0x4C, bit D4, D3, D2)

As per *Section 7.22.2*, the assertion of PWDN activates a counter that, by default, after 13 million clock cycles puts the power bridge in tristate mode, independently from the fade-out time. Using these registers it is possible to program this counter according to the following table.

Table 171. PNDLSL bits configuration

PNDLSL[2]	PNDLSL[1]	PNDLSL[2]	Fade-out time
0	0	0	Default time (13M PLL clock cycles)
0	0	1	Default time divided by 2
0	1	0	Default time divided by 4
0	1	1	Default time divided by 8
1	0	0	Default time divided by 16
1	0	1	Default time divided by 32
1	1	0	Default time divided by 64
1	1	1	Default time divided by 128

7.22.6 Short-circuit check enable bit (address 0x4C, bit D0)

This bit, when enabled, will activate the short-circuit checks before any power bridge activation (EAPD bit 0->1). See section *7.20* for more details.

7.23 Bad PWM detection registers (address 0x4D, 0x4E, 0x4F)

D7	D6	D5	D4	D3	D2	D1	D0
BPTH[5]	BPTH[4]	BPTH[3]	BPTH[2]	BPTH[1]	BPTH[0]	reserved	reserved
0	0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
BP4B	BP4A	BP3B	BP3A	BP2B	BP2A	BP1B	BP1A
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BPTIM[7]	BPTIM[6]	BPTIM[5]	BPTIM[4]	BPTIM[3]	BPTIM[2]	BPTIM[1]	BPTIM[0]
0	1	0	1	1	1	1	0

The STA381BW implements a detection on the PWM outputs able to verify if the output signal has no zero-crossing in a configurable time window. This check can be useful to detect DC levels in the PWM outputs. To be noted that the checks are performed on logic level PWM (i.e. not the power bridge ones, nor the PWM on DDX3 and DDX4 I/Os).

In case of ternary modulation, the detection threshold is computed as:

TH=[(BPTH*2+1)/128]*100%

If the measured PWM duty cycle is detected greater than or equal to TH for more than BPTIM PWM periods, the corresponding PWM bit will be set in register 0x4E.

In case of binary modulation, there are two thresholds:

TH1=[(64+BPTH)/128]*100%

TH2=[(64-BPTH)/128]*100%

In this case if the measured PWM duty cycle is outside the TH1-TH2 range for more than BPTIM PWM periods, the corresponding bit will be set in register 0x4E.

7.24 Enhanced zero-detect mute and input level measurement (address 0x50-0x54, 0x2E, 0x2F and 0x5E)

D7	D6	D5	D4	D3	D2	D1	D0
WTHH	WTHL	FINETH	HSEL[1:0]		ZMTH[2:0]		
0	0	0	0	0	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
RMS_CH0[7:0]							
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

D7	D6	D5	D4	D3	D2	D1	D0
RMS_CH0[15:8]							
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

D7	D6	D5	D4	D3	D2	D1	D0
RMS_CH1[7:0]							
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

D7	D6	D5	D4	D3	D2	D1	D0
RMS_CH1[15:8]							
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

The STA381BW implements an RMS-based zero-detect function (on serial input interface data) able to detect in a very reliable way the presence of an input signal, so that the power bridge outputs can be automatically connected to ground.

When active, the function will mute the output PWM when the input level become less than “threshold - hysteresis”. Once muted, the PWM will be unmuted when the input level is detected greater than “threshold + hysteresis”.

The measured level is then reported (for each input channel) on registers 0x51 - 0x52, 0x53 - 0x54 according to the following equation:

$Value\_in\_dB = 20*Log_{10}(Reg\_value/(2^{16}*0.635))$

Table 172. Zero-detect threshold

ZMTH[2:0]	Equivalent input level (dB)
000	-78
001	-84
010	-90
011	-96
100	-102
101	-108
110	-114
111	-114

Table 173. Zero-detect hysteresis

HSEL[1:0]	Equivalent input level hysteresis (dB)
00	3
01	4
10	5
11	6

The above thresholds and hysteresis table can be overridden and the low-level threshold and high-level threshold can be set by the MTH[21:0] bits.

To activate the manual thresholds the FINETH bit has to be set to ‘1’.

To configure the low threshold, the WTHL bit must be set to ‘1’ so that any write operation to the MTH bits will set the low threshold.

To configure the low threshold, the WTHH bit must be set to ‘1’ so that any write operation to the MTH bits will set the low threshold.

If the zero-mute block does not detect mute, it will mute the output when the current RMS value falls below the low threshold.

If the zero-mute block does not detect mute, it will unmute the output when the current RMS value rises above the high threshold.

Table 174. Manual threshold register 0x2E, 0x2F and 0x5E

D7	D6	D5	D4	D3	D2	D1	D0
ReservedT	Reserved	MTH[21:16]					
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
MTH[15:8]							
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
MTH[7:0]							
0	0	0	0	0	0	0	0

7.25 Headphone/Line out configuration register (address 0x55)

D7	D6	D5	D4	D3	D2	D1	D0
HPLN	Reserved	MUTE	Reserved	CPFEN	CPOK	ABFAULT	DCROK
0	0	1	0	0	NA	NA	NA

Table 175. Headphone/Line out configuration bits

Bit	R/W	RST	Name	Description
7	R/W	0	HPLN	When F3X is connected to the internal HP/Line driver this bit selects the gain of the F3X->analog out path. ‘0’: HP out. When the MVOL+Channel Vol is 0 dBFs, a 0 dBFs input will generate a 40 mW output on a 32 ohm load (+/- 3.3 V supply). ‘1’:Line out. When the MVOL+Channel Vol is 0 dBFs, a 0 dBFs input will generate a 2 Vrms output (+/- 3.3 V supply)
5	R/W	1	MUTE	‘1’: HP/Line out muted ‘0’: HP/Line out playing
3	R/W	0	CPFEN	‘0’: Charge pump auto enable when unmute ‘1’: Charge pump is always enabled
2	R	NA	CPOK	‘0’: Charge pump is not working ‘1’: Charge pump is working and it is OK
1	R	NA	ABFAULT	‘0’: No fault on class-AB ‘1’: Overcurrent fault detected on class-AB
0	R	NA	DCROK	‘1’: core supply OK

7.26 F3XCFG (address 0x58; 0x59)

D7	D6	D5	D4	D3	D2	D1	D0
F3XLNK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
F3X_FAULT	Reserved	Reserved	F3X_SM_SLOPE			F3X_MUTE	F3X_ENA
NA	1	1	0	1	1	1	0

Table 176. F3X configuration register 1

Bit	R/W	RST	Name	Description
7	R/W	0	F3XLNK	'0': F3X normal control mode '1': F3X mute/unmute linked to HP/Line mute

Table 177. F3X configuration register 2

Bit	R/W	RST	Name	Description
7	R	NA	F3X_FAULT	'0': Normal operation
4	R/W	0	F3X_SM_SLOPE	'000': 0 ms '001': 25 ms '010': 50 ms '011': 100 ms '100': 200 ms '101': 250 ms '110': 500 ms '111': 1000 ms
3	R/W	1		
2	R/W	1		
1	R/W	1	F3X_MUTE	'1': Mute
0	R/W	0	F3X_ENA	'1': F3X enable

7.27 STCompressor^{TM} configuration register (address 0x5A; 0x5B)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	LIM_BYP	STC_BYP	STC_ENA	reserved	NP_CRES	reserved	NP_CRC-GO
0	0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	STC_LNK	BRC_EN
0	0	0	0	0	0	0	0

Table 178. STCompressor^{TM} configuration bits1

Bit	R/W	RST	Name	Description
6	R/W	0	LIM_BYP	‘0’: STCompressor^{TM} DRC active ‘1’: STCompressor^{TM} DRC is bypassed
5	R/W	1	STC_BYP	‘0’: STCompressor^{TM} processing activated ‘1’: STCompressor^{TM} is in pass-through
4	R/W	1	STC_EN	‘0’: STCompressor^{TM} is switched off (no configuration is possible in this state) ‘1’: STCompressor^{TM} is enabled
2	R	0	NP_CRCRES	‘1’: CRC STCompressor ok ‘0’: CRC STCompressor error
0	R/W	0	NP_CRC_GO	‘1’: Start CRC STCompressor compute ON ‘0’: Idle

Table 179. STCompressor^{TM} configuration bits 2

Bit	R/W	RST	Name	Description
1	R/W	0	STC_LNK	‘0’: Channel 0 and channel 1 attenuation are applied independently ‘1’: Channel 0 and channel 1 attenuation are linked so that the higher one is applied to both channel 0 and channel 1
0	R/W	0	BRC_EN	‘1’: STCompressor band recombination enabled ‘0’: Disabled

7.28 Charge pump synchronization (address 0x5F)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	CHPI	INITCNT[3:0]				CHPRD
0	0	0	1	1	0	0	1

Table 180. Charge pump sync configuration bits

Bit	R/W	RST	Name	Description
5	R/W	0	CHPI	0: Charge pump phase: 0 deg 1: Charge pump phase: 180 deg
4	R/W	1	INITCNT[3:0]	Change charge pump phase at one clock step
3	R/W	1		
2	R/W	0		
1	R/W	0		
0	R/W	1	CHPRD	0: Charge pump synchronized with PWM frame 0: Charge pump not synchronized with PWM frame

The charge pump can be synchronized with the PWM frame in order to minimize the crosstalk between the charge pump and the PWM waveform.

This functionality cannot be activated when the PWMS bit (address 0x15 bit D4) is set to 1.

7.29 Coefficient RAM CRC protection (address 0x60-0x6C)

D7	D6	D5	D4	D3	D2	D1	D0
BQCKE[7]	BQCKE[6]	BQCKE[5]	BQCKE[4]	BQCKE[3]	BQCKE[2]	BQCKE[1]	BQCKE[0]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BQCKE[15]	BQCKE[14]	BQCKE[13]	BQCKE[12]	BQCKE[11]	BQCKE[10]	BQCKE[9]	BQCKE[8]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BQCKE[23]	BQCKE[22]	BQCKE[21]	BQCKE[20]	BQCKE[19]	BQCKE[18]	BQCKE[17]	BQCKE[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKE[7]	XCCKE[6]	XCCKE[5]	XCCKE[4]	XCCKE[3]	XCCKE[2]	XCCKE[1]	XCCKE[0]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKE[15]	XCCKE[14]	XCCKE[13]	XCCKE[12]	XCCKE[11]	XCCKE[10]	XCCKE[9]	XCCKE[8]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKE[23]	XCCKE[22]	XCCKE[21]	XCCKE[20]	XCCKE[19]	XCCKE[18]	XCCKE[17]	XCCKE[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BQCKR[7]	BQCKR[6]	BQCKR[5]	BQCKR[4]	BQCKR[3]	BQCKR[2]	BQCKR[1]	BQCKR[0]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BQCKR[15]	BQCKR[14]	BQCKR[13]	BQCKR[12]	BQCKR[11]	BQCKR[10]	BQCKR[9]	BQCKR[8]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
BQCKR[23]	BQCKR[22]	BQCKR[21]	BQCKR[20]	BQCKR[19]	BQCKR[18]	BQCKR[17]	BQCKR[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKR[23]	XCCKR[22]	XCCKR[21]	XCCKR[20]	XCCKR[19]	XCCKR[18]	XCCKR[17]	XCCKR[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKR[23]	XCCKR[22]	XCCKR[21]	XCCKR[20]	XCCKR[19]	XCCKR[18]	XCCKR[17]	XCCKR[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCCKR[23]	XCCKR[22]	XCCKR[21]	XCCKR[20]	XCCKR[19]	XCCKR[18]	XCCKR[17]	XCCKR[16]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
XCAUTO	XCRES	XCCMP	XCGO	BCAUTO	BCCRES	BCCMP	BCCGO
0	0	0	0	0	0	0	0

The STA381BW implements an automatic CRC computation for the biquad and MDRC/XOver coefficient memory. Memory cell contents from address 0x00 to 0x27 will be bit XORed to obtain the BQCHKE checksum, while cells from 0x28 to 0x31 will be XORed to obtain the XCCHKE checksum. Both checksums (24-bit wide) are exported on I^2C registers from 0x60 to 0x65. The checksum computation will start as soon as the BCGO (for biquad RAM bank) or the XCGO bit (for MDRC/XOver coefficients) is set to 1. The checksum is computed at the processing sample rate if the IR bits equal “01” or “10”, otherwise the checksum is computed to half the processing sample rate.

When BCCMP or XCCMP are set to ‘1’, the relative checksum (BQCHKE and XCCHKE) is continuously compared with BQCHKR and XCCHKR respectively. If the checksum matches its own reference value, the respective result bits (BCRES and XCRES) will be set to ‘0’. The compare bits have no effect if the respective GO bit is not set.

In case of checksum errors (i.e. the internally computed didn’t match the reference), an automatic device reset action can be activated. This function is enabled when the BCAUTO or XCAUTO bit is set to ‘1’. The automatic reset bits have no effect if the respective compare bits are not set.

The recommended procedure for the automatic reset activation is the following:

- Download the set of coefficients (RAM locations 0x00…0x27)
- Download the externally computed biquad checksum into registers *BQCHKR*
- Enable the checksum of the biquad coefficients by setting the *BCGO* bit. The checksum will start to be automatically computed by the STA381BW and its value exposed on registers *BQCHECKE.* The checksum value is computed and updated.
- Enable the checksum comparison by setting the *BCCMP* bit. The internally computed checksum will start to be compared with the reference one and the result will be exposed on the *BCRES* bit. The following operation will be executed on each audio frame:

```
if ((BQCHKE == BQCHKR))
{
    BC_RES = 0;// Checksum is ok, reset the error bit
}
else
{
    BC_RES = 1;// Checksum error detected, set the error bit
}
```

- Wait until the BCRES bit goes to 0, meaning that the checksum result bit has started to be updated and everything is ok. Time-out of this operation (e.g. > 1 ms) will indicate checksum failure, and the MCU will handle this event.
- Enable automatic reset of the device in case of checksum error by setting the *BCAUTO* bit. The *BCRES* bit will then be automatically checked by the STA381BW, on each audio frame, and the reset event will be triggered in case of checksum mismatch.
- Periodically check the *BC_RES* status. A value of 1 indicates that a checksum mismatch has occurred and, therefore, the device went through a reset cycle.

The previous example is intended for biquad CRC bank calculation, but it can be easily extended to MDRC/XOver CRC computation.

7.30 MISC3 (address 0x6E)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	SRESET	reserved	reserved
0	0	0	0	0	0	0	0

Table 181. Misc register 3

Bit	R/W	RST	Name	Description
2	R/W	0	SRESET	'0': normal operation '1': reset the device

After SRESET is written, the last IC acknowledge is skipped and the EAPD bit (reg 0x16 bit D7) is set to1 instead of the 0 default value obtained after the hardware reset.

7.31 MISC4 (address 0x7E)

D7	D6	D5	D4	D3	D2	D1	D0
SMAP	reserved	reserved	reserved	reserved	reserved	reserved	reserved
1	0	0	0	0	0	0	0

Table 182. MISC4

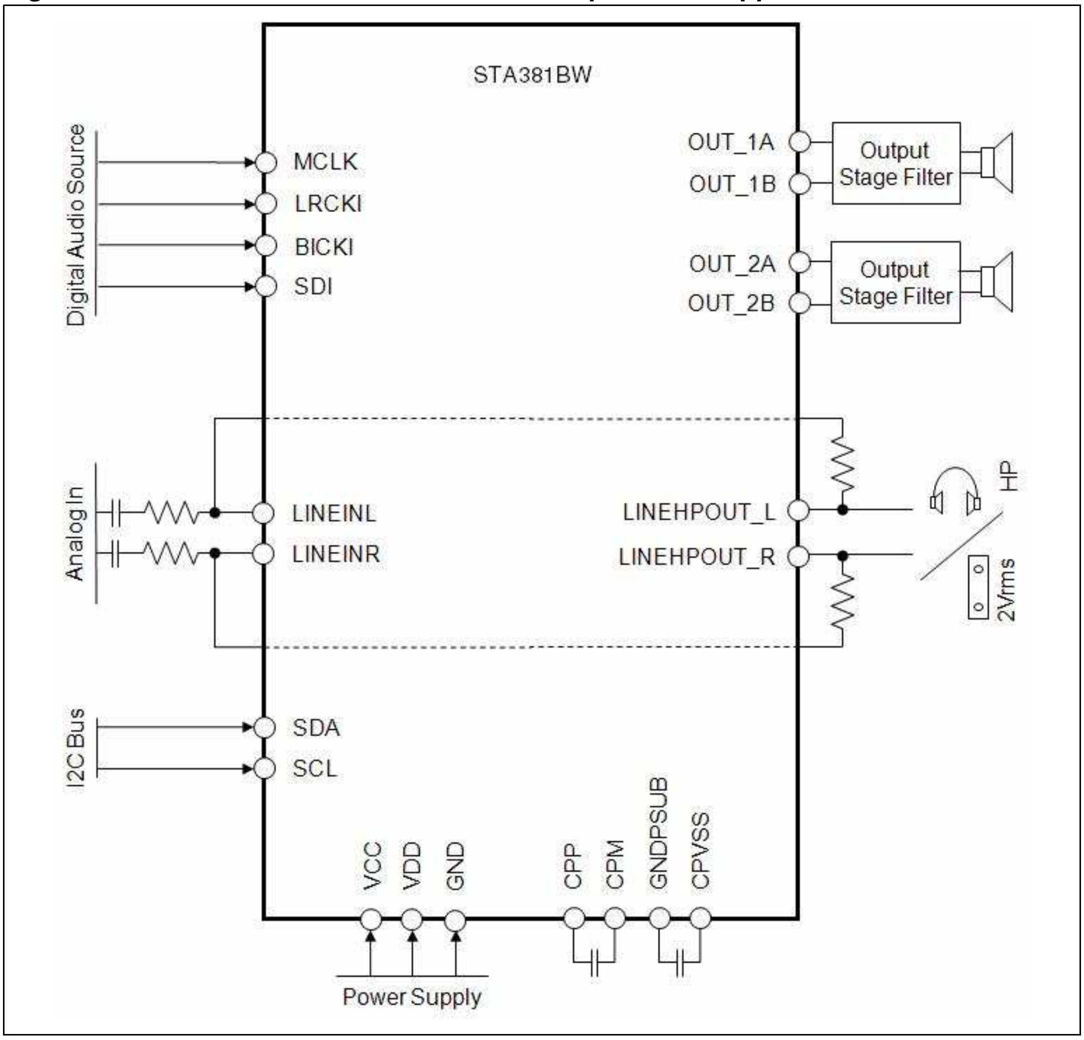
Bit	R/W	RST	Name	Description
7		1	SMAP	'1': NEWMAP '0': STMAP

8 Applications

8.1 Application schemes

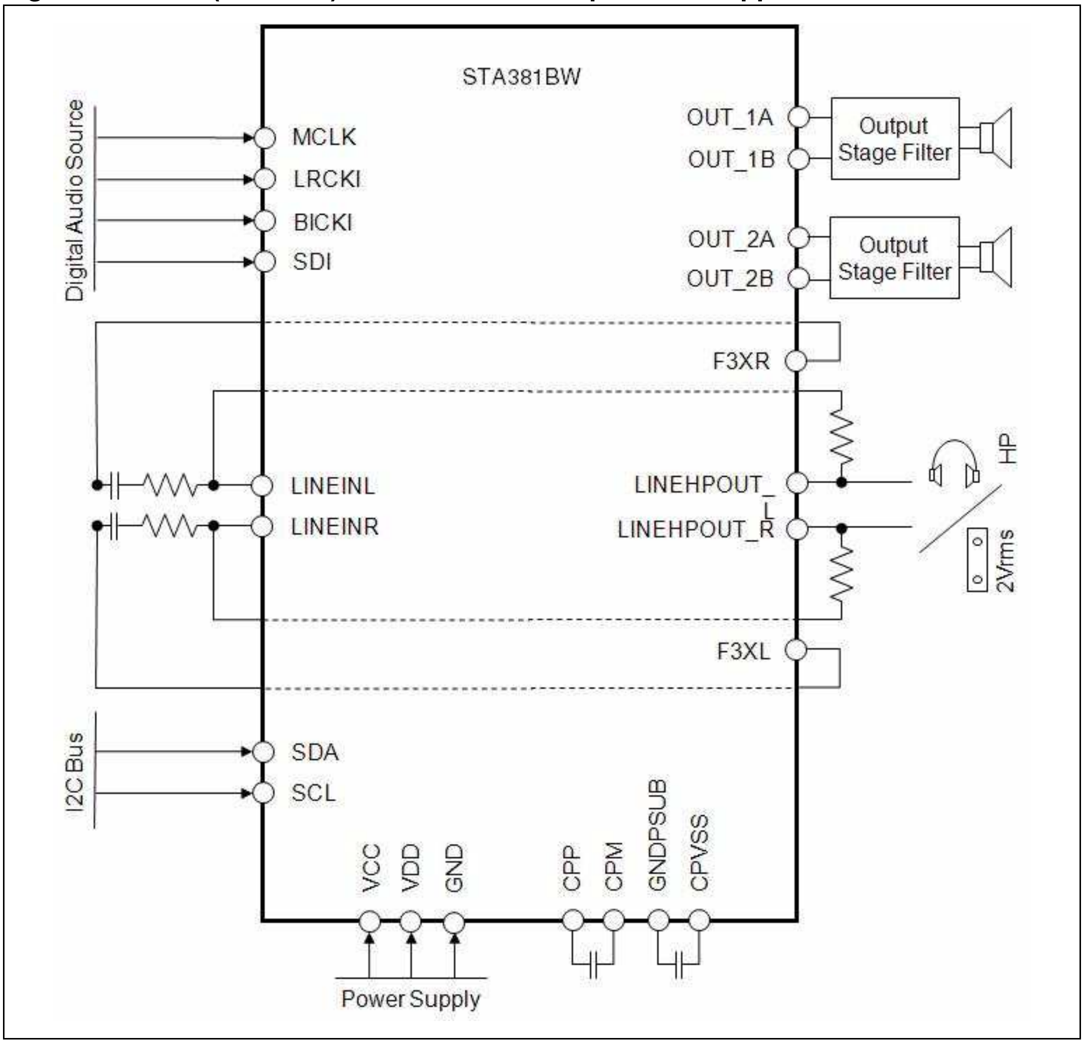
The following figures illustrate typical application schemes for the STA381BW. The line/headphone out can be fed either with an external analog source (*Figure 44*), or with the F3X output, allowing to have the audio content coming from the digital interface on both the power output and on the line/headphone out (*Figure 45*). Regardless of the LINEINx pins input, the F3Xx outputs can be connected to an external amplifier as an auxiliary analog output (*Figure 46*). The F3X audio content is provided by the device digital audio interface.

Figure 44. External audio source to line/headphone out application scheme



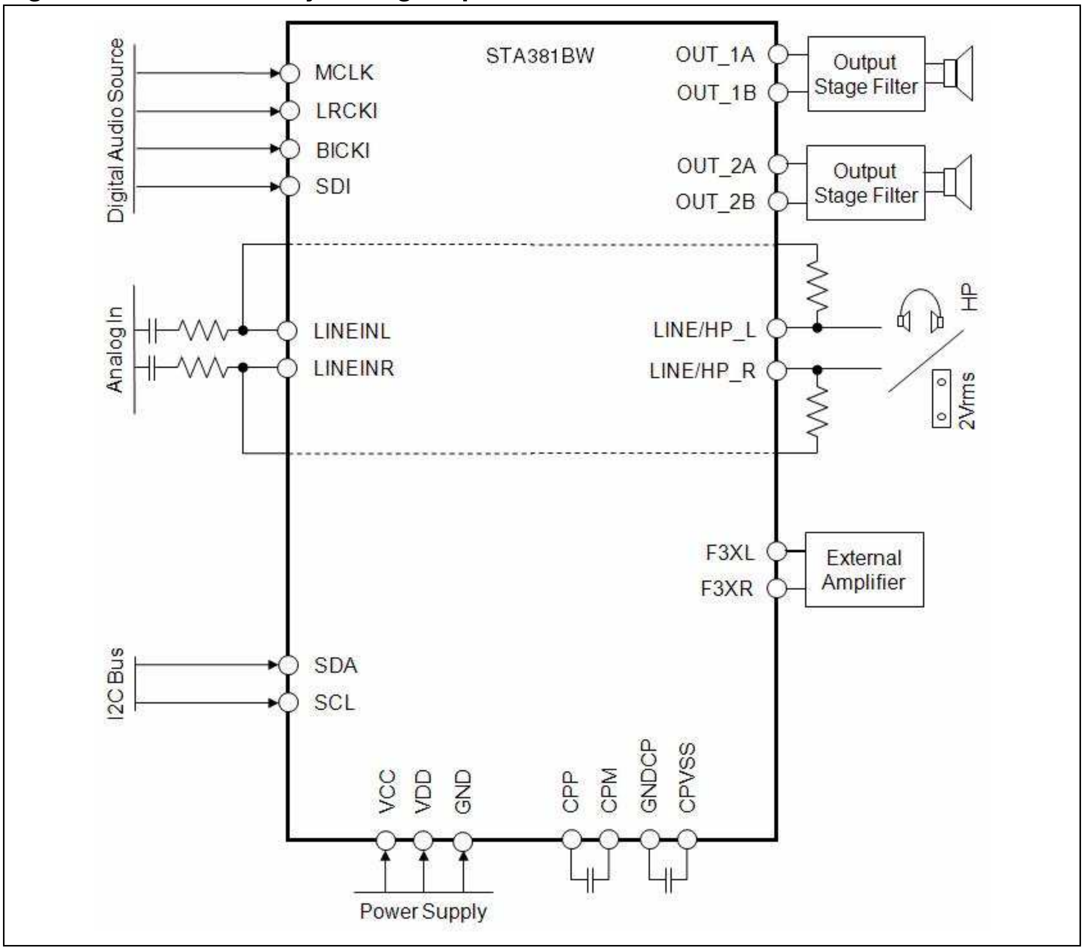
Note: For further information, please refer to application note AN3959, 2.0-channel demonstration board based on the STA381BW and STA381BWS.

Figure 45. F3X (from SAI) source to line/headphone out application scheme



Note: *For further information, please refer to application note AN3959, 2.0-channel demonstration board based on the STA381BW and STA381BWS.*

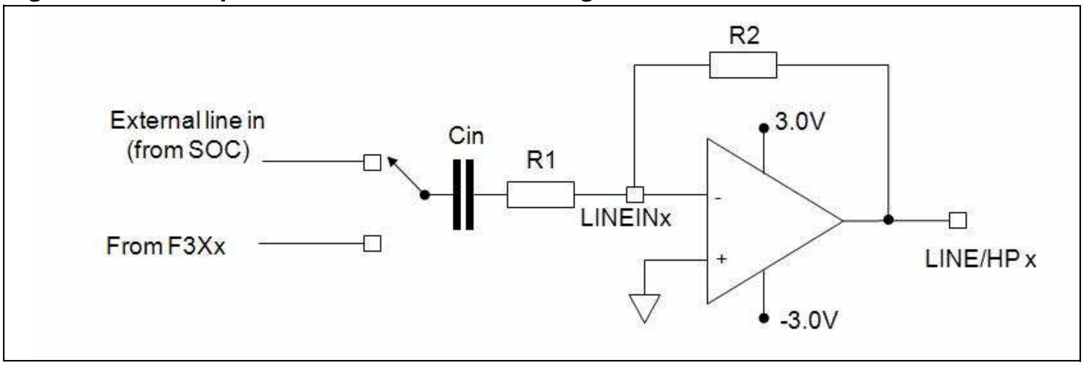
Figure 46. F3X auxiliary analog output



Note: *For further information, please refer to application note AN3959, 2.0-channel demonstration board based on the STA381BW and STA381BWS.*

8.2 Headphone and 2 Vrms line out

Figure 47. Headphone and line out block diagram



Note: *For further information, please refer to application note AN3959, 2.0-channel demonstration board based on the STA381BW and STA381BWS.*

Besides the digital input to the power output path, a line in to the headphone / 2Vrms line out path is provided. The headphone and line out block diagram is shown in *Figure 47*. The overall gain is determined by the external resistors R1 and R2 as:

Gain=R2/R1*2

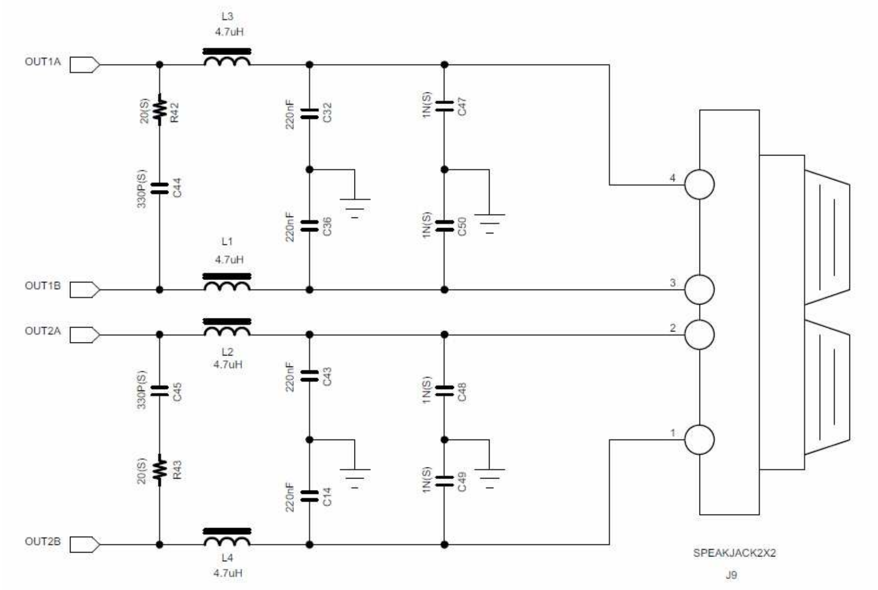
The LINEINR/LINEINL pins can be either connected to an external line in or to the F3XL/F3XR pins as depicted in *Figure 44* and *Figure 45*. Thanks to this latter option it is possible to route the digital input (SAI) content on both the power and the line out/headphone output.

Note: The charge pump of the headphone and line out cannot drive a purely capacitive load. Please refer to AN3959 (2.0-channel demonstration board based on the STA381BW and STA381BWS) for detailed information about headphone and line out filtering.

8.3 Typical output configuration

Figure 48 illustrates the typical output configuration used for BTL stereo mode. Please refer to the application note for all the other schematics for the recommended output configuration.

Figure 48. Output configuration for stereo BTL mode in filterlight configuration



Note: For further information, please refer to application note AN3959, 2.0-channel demonstration board based on the STA381BW and STA381BWS.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 49. VQFN48 (7 x 7 x 0.9 mm) package outline

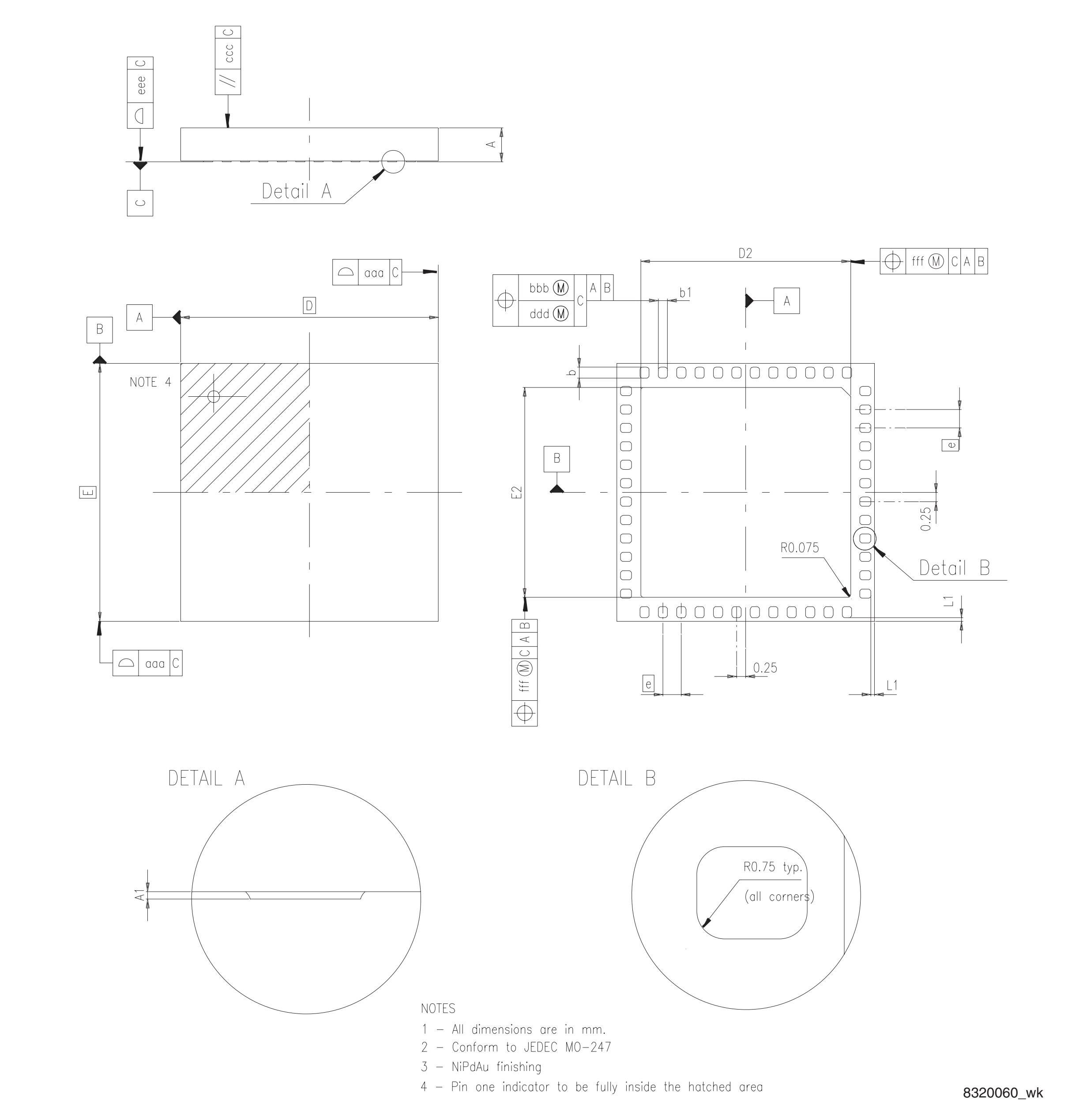


Table 183. VQFN48 (7 x 7 x 0.9 mm) package dimensions

Reference	mm		
	Min.	Typ.	Max
A	0.80	0.90	1.00
A1	0		0.05
D	6.90	7.00	7.10
D2	5.65	5.70	5.75
E	6.90	7.00	7.10
E2	5.65	5.70	5.75
b	0.25	0.30	0.35
b1	0.20	0.25	0.30
e (pad pitch)		0.50	
L1	0.05		0.15
aaa		0.15	
bbb		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
ccc		0.10	

10 Revision history

Table 184. Document revision history

Date	Revision	Changes
08-Jun-2011	1	Initial release
28-Jun-2011	2	Removed TQFP64 package option
02-Sep-2011	3	Added note to *Figure 44*, *45*, *46*, *47*, *48*, and *Section 8.2: Headphone and 2 Vrms line out*, referencing AN3959
20-Dec-2011	4	Updated names of pin 32 and 33 in *Figure 1: Block diagram*, *Figure 2: Pin connections VQFN48 (top view)* and *Table 2: Pin list* Document promoted from preliminary to full datasheet
17-Jan-2012	5	Added “VDD3V3CHP” to *Table 3* and *Table 5* Updated footnotes in *Table 7* Updated register names to “SVUP” and “SVDN” for addresses 37 and 38 in *Table 100* Updated text in *Table 46* and *Table 121: PWM speed mode* Updated *2.0 channels, two full-bridges (OCFG = 00) on page 118* Updated *2.1 channels, two full-bridges + one external full-bridge (OCFG = 10) on page 120* Updated high-pass filter in *Table 152* Textual changes to formulas in *Section 7.17: EQ soft volume configuration registers (addr 0x37 - 0x38)*
20-Jun-2012	6	Added overvoltage protection threshold (V_{OV}) to *Table 7: Electrical specifications - power section*
03-Aug-2012	7	Removed ECLE bit and sections concerning “Auto EAPD on clock loss” from datasheet Updated *Table 14: Default register map table: NEW MAP on page 42* Updated *Table 100: I^2C registers summary on page 103* Updated *Section 6.32: Enhanced zero-detect mute and input level measurement (address 0x61-0x65, 0x3F, 0x40, 0x6F) on page 94* Added *Table 90: Manual threshold register 0x3F, 0x40 and 0x6F on page 95* Added *Section 6.36: Charge pump synchronization (address 0x70) on page 98* Added *Table 98: Charge pump sync configuration bits on page 98* Updated *Section 7.24: Enhanced zero-detect mute and input level measurement (address 0x50-0x54, 0x2E, 0x2F and 0x5E) on page 155* Added *Table 174: Manual threshold register 0x2E, 0x2F and 0x5E on page 157* Added *Section 7.28: Charge pump synchronization (address 0x5F) on page 160* Added *Table 180: Charge pump sync configuration bits on page 160*