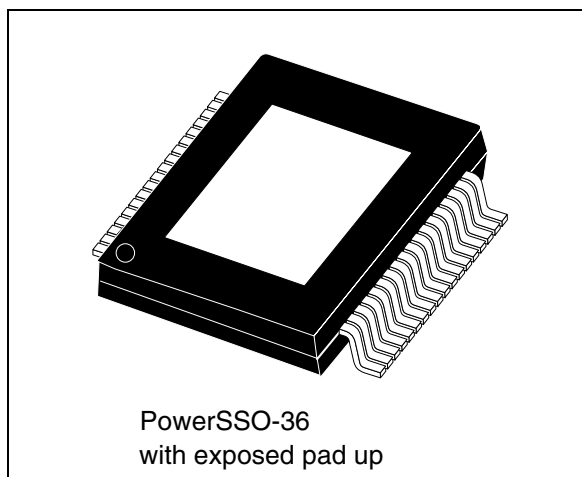


80 watt + 80 watt dual BTL class-D audio amplifier

Features

- 80 W + 80 W output power at
THD = 10% with $R_L = 6\ \Omega$ and $V_{CC} = 32\text{ V}$
- 70 W + 70 W output power at
THD = 10% with $R_L = 8\ \Omega$ and $V_{CC} = 34\text{ V}$
- Wide-range single-supply operation (14 - 36 V)
- High efficiency ($\eta = 90\%$)
- Four selectable, fixed gain settings of
nominally 25.6 dB, 31.6 dB, 35.1 dB and
37.6 dB
- Differential inputs minimize common-mode
noise
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- Externally synchronizable



Description

The TDA7498L is a dual BTL class-D audio amplifier with single power supply designed for home systems and active speaker applications.

It comes in a 36-pin PowerSSO package with exposed pad up (EPU) to facilitate mounting a separate heatsink.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
TDA7498L	-40 to 85 °C	PowerSSO-36 (EPU)	Tube
TDA7498LTR	-40 to 85 °C	PowerSSO-36 (EPU)	Tape and reel

Contents

1	Pin description	6
1.1	Pinout	6
1.2	Pin list	7
2	Electrical specifications	8
2.1	Absolute maximum ratings	8
2.2	Thermal data	8
2.3	Recommended operating conditions	8
2.4	Electrical specifications	8
3	Characterizations	11
3.1	Test circuit	11
3.2	Characterization curves	13
3.2.1	For $R_L = 6\ \Omega$	13
3.2.2	For $R_L = 8\ \Omega$	16
4	Applications information	19
4.1	Applications circuit	19
4.2	Mode selection	20
4.3	Gain setting	21
4.4	Input resistance and capacitance	21
4.5	Internal and external clocks	22
4.5.1	Master mode (internal clock)	22
4.5.2	Slave mode (external clock)	22
4.6	Output low-pass filter	23
4.7	Protection functions	24
4.8	Diagnostic output	24
5	Package mechanical data	25
6	Revision history	27

List of figures

Figure 1.	Internal block diagram (showing one channel only)	5
Figure 2.	Pin connections (top view, PCB view)	6
Figure 3.	Test circuit for characterizations	11
Figure 4.	Test board	12
Figure 5.	Output power (THD = 10%) vs. supply voltage	13
Figure 6.	THD vs. output power	13
Figure 7.	THD vs. frequency (1 W)	14
Figure 8.	THD vs. frequency (100 mW)	14
Figure 9.	Frequency response	14
Figure 10.	FFT performance (0 dBFS)	15
Figure 11.	FFT performance (-60 dBFS)	15
Figure 12.	Output power (THD = 10%) vs. supply voltage	16
Figure 13.	THD vs. output power	16
Figure 14.	THD vs. frequency (1 W)	17
Figure 15.	THD vs. frequency (100 mW)	17
Figure 16.	Frequency response	17
Figure 17.	FFT performance (0 dB)	18
Figure 18.	FFT performance (-60 dB)	18
Figure 19.	Applications circuit for 6- or 8- Ω speakers	19
Figure 20.	Standby and mute circuits	20
Figure 21.	Turn on/off sequence for minimizing speaker "pop"	20
Figure 22.	Input circuit and frequency response	21
Figure 23.	Master and slave connection	22
Figure 24.	Typical LC filter for a 8- Ω speaker	23
Figure 25.	Typical LC filter for a 6- Ω speaker	23
Figure 26.	Behavior of pin DIAG for various protection conditions	24
Figure 27.	PowerSSO36 EPU outline drawing	26

List of tables

Table 1. Device summary 1

Table 2. Pin description list 7

Table 3. Absolute maximum ratings 8

Table 4. Thermal data 8

Table 5. Recommended operating conditions 8

Table 6. Electrical specifications 9

Table 7. Mode settings 19

Table 8. Gain settings 20

Table 9. How to set up SYNCLK 21

Table 10. PowerSSO-36 EPU dimensions 24

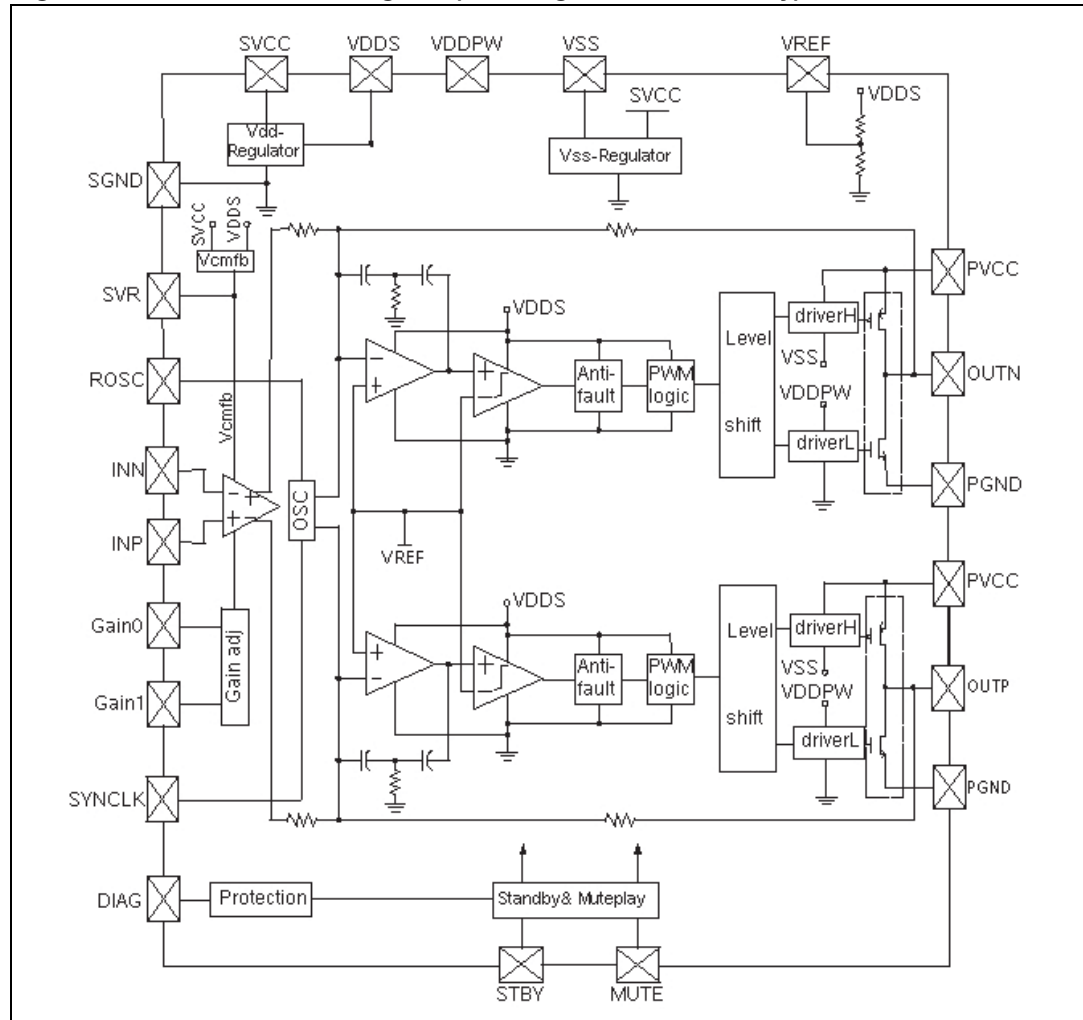
Table 11. Document revision history 26



1 Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7498L.

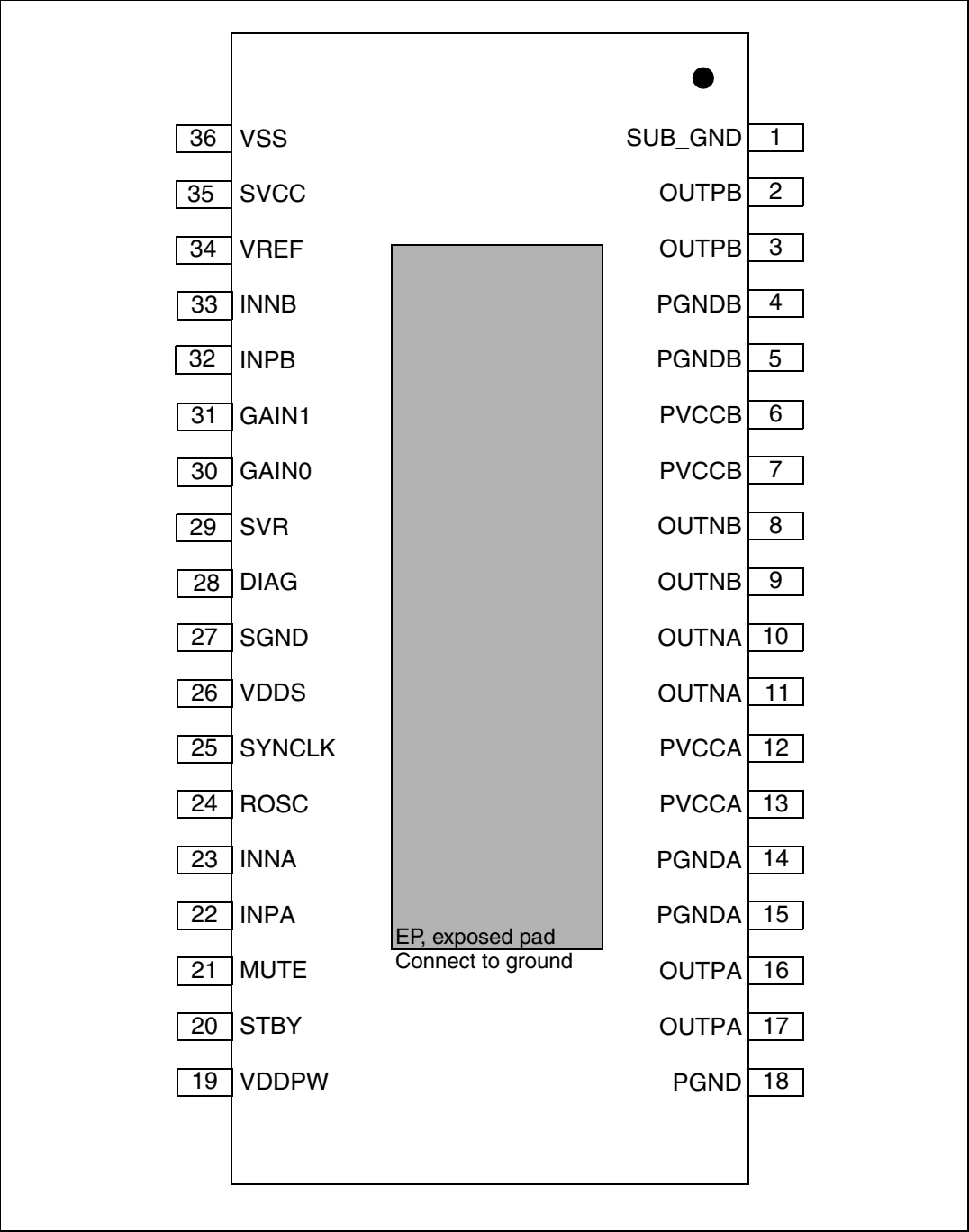
Figure 1. Internal block diagram (showing one channel only)



2 Pin description

2.1 Pinout

Figure 2. Pin connections (top view, PCB view)



2.2 Pin list

Table 2. Pin description list

Number	Name	Type	Description
1	SUB_GND	PWR	Connect to the frame
2,3	OUTPB	O	Positive PWM for right channel
4,5	PGNDB	PWR	Power stage ground for right channel
6,7	PVCCB	PWR	Power supply for right channel
8,9	OUTNB	O	Negative PWM output for right channel
10,11	OUTNA	O	Negative PWM output for left channel
12,13	PVCCA	PWR	Power supply for left channel
14,15	PGNDA	PWR	Power stage ground for left channel
16,17	OUTPA	O	Positive PWM output for left channel
18	PGND	PWR	Power stage ground
19	VDDPW	O	3.3-V (nominal) regulator output referred to ground for power stage
20	STBY	I	Standby mode control
21	MUTE	I	Mute mode control
22	INPA	I	Positive differential input of left channel
23	INNA	I	Negative differential input of left channel
24	ROSC	O	Master oscillator frequency-setting pin
25	SYNCLK	I/O	Clock in/out for external oscillator
26	VDDS	O	3.3-V (nominal) regulator output referred to ground for signal blocks
27	SGND	PWR	Signal ground
28	DIAG	O	Open-drain diagnostic output
29	SVR	O	Supply voltage rejection
30	GAIN0	I	Gain setting input 1
31	GAIN1	I	Gain setting input 2
32	INPB	I	Positive differential input of right channel
33	INNB	I	Negative differential input of right channel
34	VREF	O	Half VDDS (nominal) referred to ground
35	SVCC	PWR	Signal power supply decoupling
36	VSS	O	3.3-V (nominal) regulator output referred to power supply
-	EP	-	Exposed pad for heatsink, to be connected to ground

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC_MAX}	DC supply voltage for pins PVCCA, PVCCB	44	V
V _{L_MAX}	Voltage limits for input pins STBY, MUTE, INNA, INPA, INNB, INPB, GAIN0, GAIN1	-0.3 to 3.6	V
T _{j_MAX}	Operating junction temperature	0 to 150	°C
T _{stg}	Storage temperature	-40 to 150	°C

Warning: Stresses beyond those listed under “Absolute maximum ratings” make cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended operating condition” are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, the power supply with the nominal value rated in the recommended operating conditions, may rise beyond the maximum operating condition for a short time when no or very low current is sunk (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum rating is not exceeded.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
R _{th j-case}	Thermal resistance, junction to case	-	2	3	°C/W

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply voltage for pins PVCCA, PVCCB	14	-	36	V
T _{amb}	Ambient operating temperature	-20	-	85	°C

3.4 Electrical specifications

Unless otherwise stated, the results in [Table 6](#) below are given for the conditions:

$V_{CC} = 32\text{ V}$, R_L (load) = $6\ \Omega$, $R_{OSC} = R3 = 39\text{ k}\Omega$, $C8 = 100\text{ nF}$, $f = 1\text{ kHz}$, $G_V = 25.6\text{ dB}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.

Table 6. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_q	Total quiescent current	No LC filter, no load	-	40	60	mA
I_{qSTBY}	Quiescent current in standby	-	-	1	10	μA
V_{OS}	Output offset voltage	Play mode	-100	-	100	mV
		Mute mode	-60	-	60	
I_{OCP}	Overcurrent protection threshold	$R_L = 0\ \Omega$	5.0	6.0	-	A
T_{JS}	Junction temperature at thermal shutdown	-	-	150	-	$^\circ\text{C}$
R_i	Input resistance	Differential input	48	60	-	$\text{k}\Omega$
V_{OVP}	Overvoltage protection threshold	-	42	43	-	V
V_{UVP}	Undervoltage protection threshold	-	-	-	8	V
R_{dsON}	Power transistor on resistance	High side	-	0.2	-	Ω
		Low side	-	0.2	-	
P_o	Output power	THD = 10%	-	80	-	W
		THD = 1%	-	65	-	
P_o	Output power	$R_L = 8\ \Omega$, THD = 10%, $V_{CC} = 32\text{ V}$	-	65	-	W
P_D	Dissipated power	$P_o = 80\text{ W} + 80\text{ W}$, THD = 10%	-	16	-	W
η	Efficiency	$P_o = 80\text{ W} + 80\text{ W}$	-	90	-	%
THD	Total harmonic distortion	$P_o = 1\text{ W}$	-	0.1	-	%
G_V	Closed-loop gain	GAIN0 = L, GAIN1 = L	24.6	25.6	26.6	dB
		GAIN0 = L, GAIN1 = H	30.6	31.6	32.6	
		GAIN0 = H, GAIN1 = L	34.1	35.1	36.1	
		GAIN0 = H, GAIN1 = H	36.6	37.6	38.6	
ΔG_V	Gain matching	-	-1	-	1	dB
CT	Crosstalk	$f = 1\text{ kHz}$, $P_o = 1\text{ W}$	50	70	-	dB
eN	Total input noise	A Curve, $G_V = 20\text{ dB}$	-	15	-	μV
		$f = 22\text{ Hz to } 22\text{ kHz}$	-	25	50	
SVRR	Supply voltage rejection ratio	$f_r = 100\text{ Hz}$, $V_r = 0.5\text{ Vpp}$, $C_{SVR} = 10\ \mu\text{F}$	-	70	-	dB
T_r, T_f	Rise and fall times	-	-	50	-	ns

Table 6. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SW}	Switching frequency	Internal oscillator	290	310	330	kHz
f_{SWR}	Output switching frequency Range	With internal oscillator ⁽¹⁾	250	-	400	kHz
		With external oscillator ⁽²⁾	250	-	400	
V_{inH}	Digital input high (H)	-	2.3	-	-	V
V_{inL}	Digital input low (L)		-	-	0.8	
V_{STBY}	Pin STBY voltage high (H)	-	2.7	-	-	V
	Pin STBY voltage low (L)		-	-	0.5	
V_{MUTE}	Pin MUTE voltage high (H)	-	2.5	-	-	V
	Pin MUTE voltage low (L)		-	-	0.8	
A_{MUTE}	Mute attenuation	$V_{MUTE} < 0.8 \text{ V}$	-	70	-	dB

1. $f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4)$ kHz, $f_{SYNCLK} = 2 * f_{SW}$ with $R3 = 39 \text{ k}\Omega$ (see [Figure 20](#)).

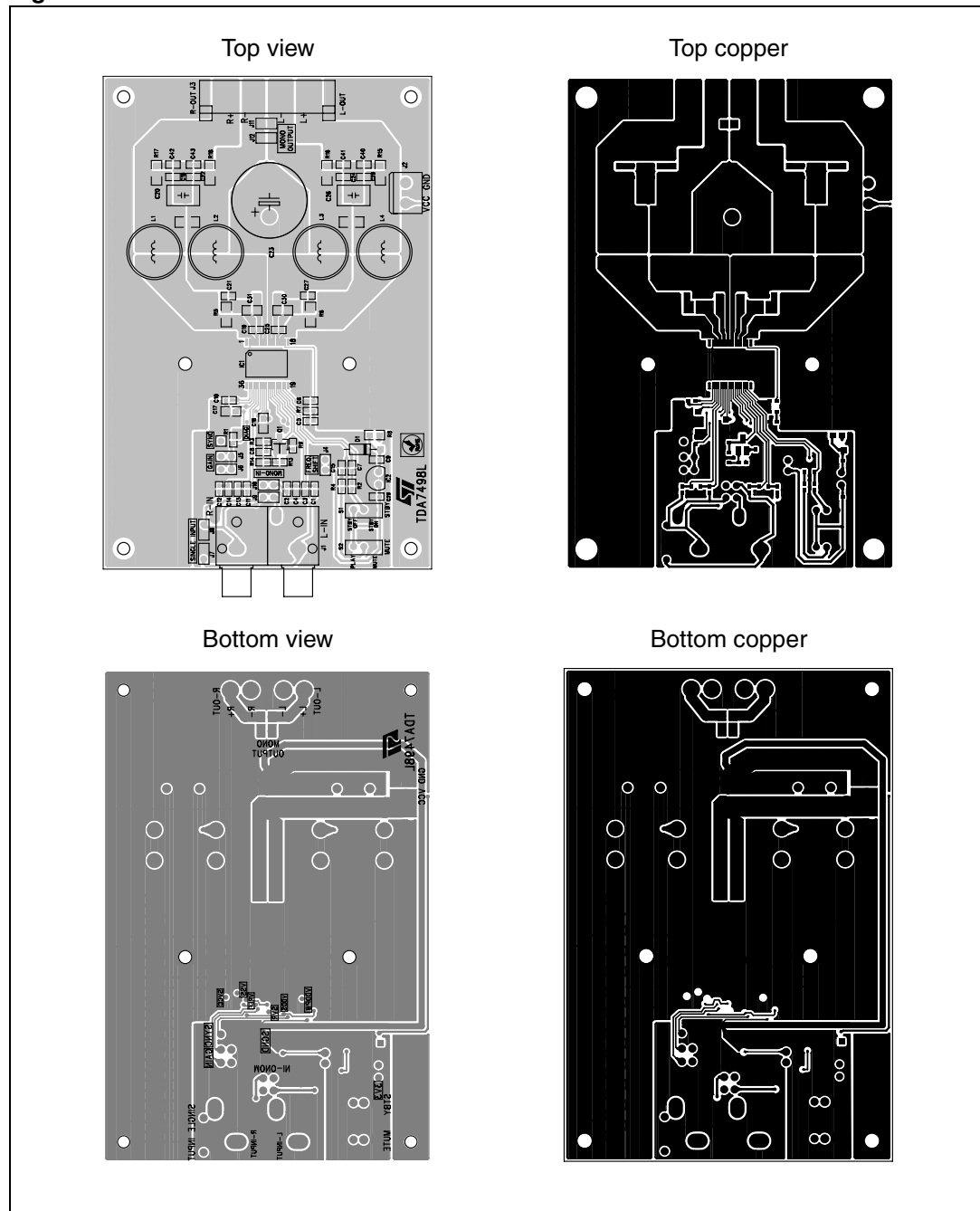
2. $f_{SW} = f_{SYNCLK} / 2$ with the external oscillator.

4 Characterization curves

[Figure 20 on page 18](#) shows the test circuit with which the characterization curves, shown in the next sections, were measured. [Figure 3](#) below shows the PCB layout.

4.1 PCB layout

Figure 3. Test board



4.2 Characterization curves

Unless otherwise stated the measurements were made under the following conditions:

$V_{CC} = 32\text{ V}$, $f = 1\text{ kHz}$, $G_V = 25.6\text{ dB}$, $R_{OSC} = 39\text{ k}\Omega$, $C_{OSC} = 100\text{ nF}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$

4.2.1 For $R_L = 6\text{ }\Omega$

Figure 4. Output power vs. supply voltage

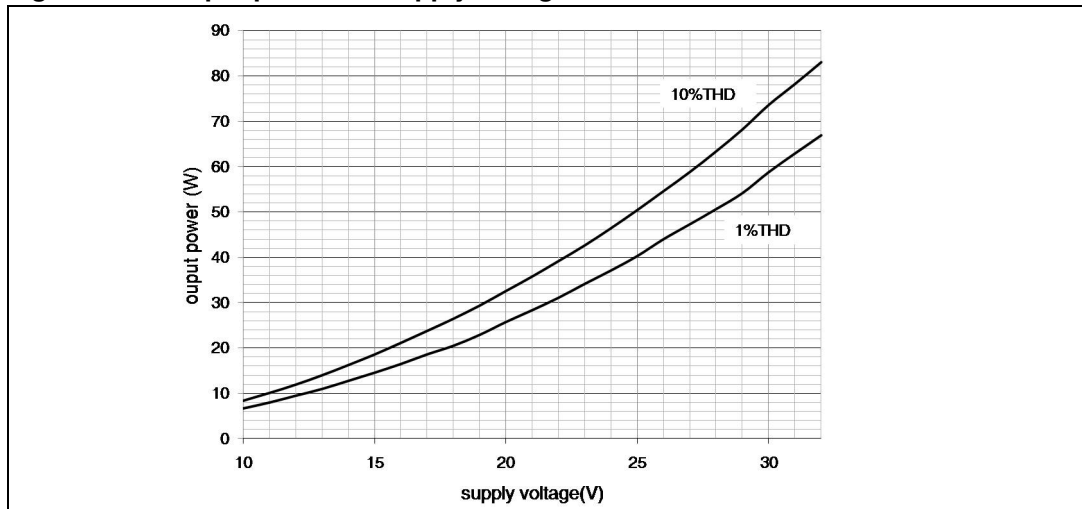


Figure 5. THD vs. output power (1 kHz)

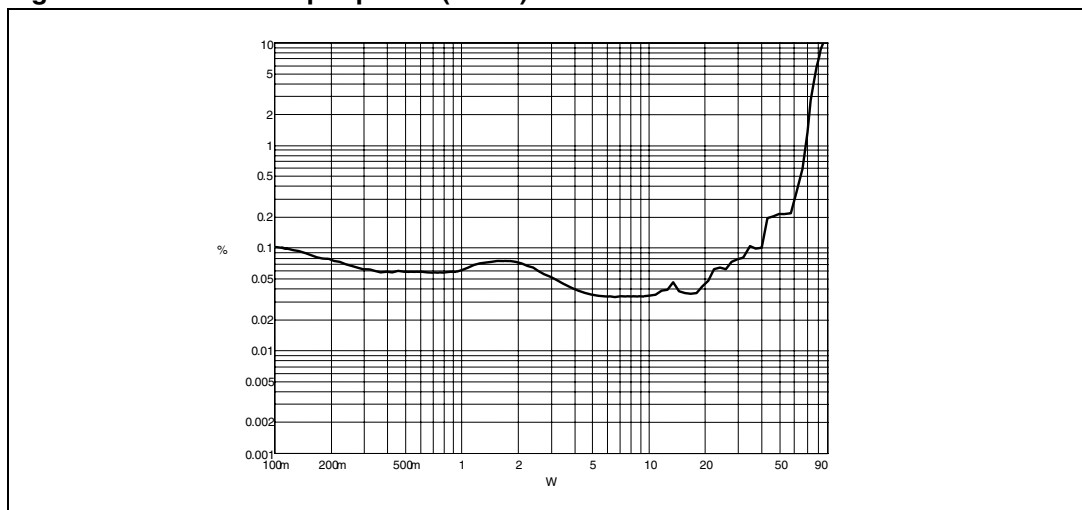


Figure 6. THD vs. output power (100 Hz)

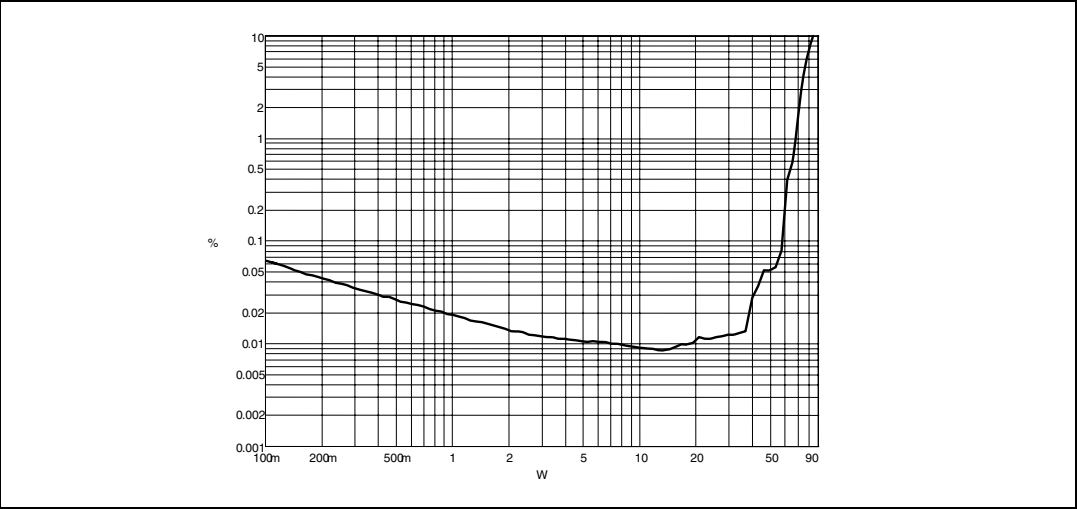


Figure 7. THD vs. frequency (1 W)

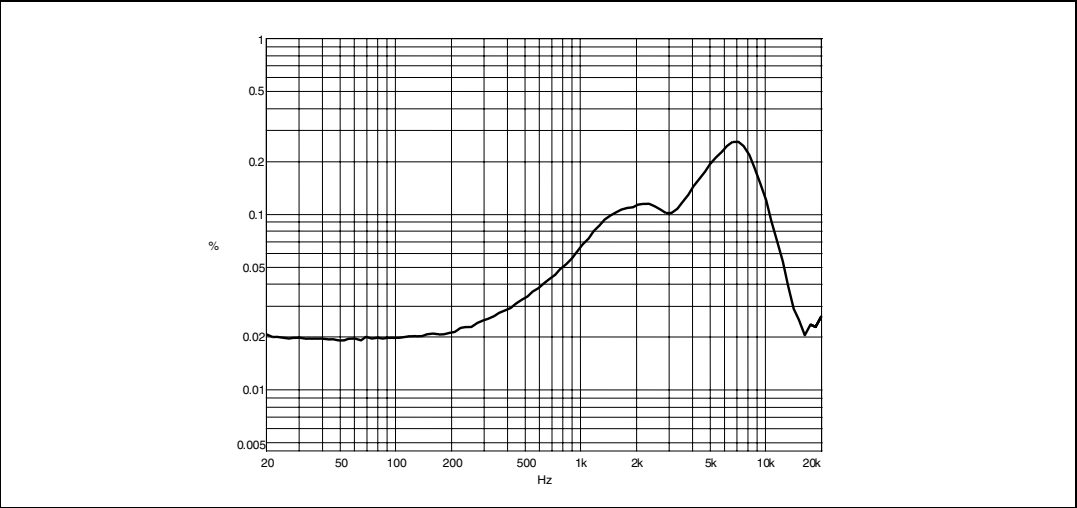


Figure 8. THD vs. frequency (100 mW)

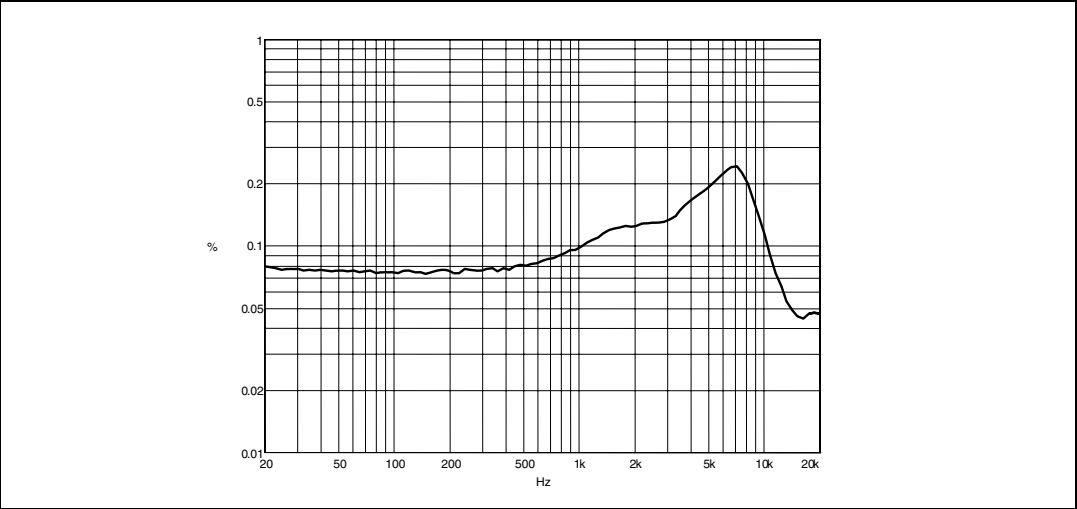


Figure 9. Frequency response

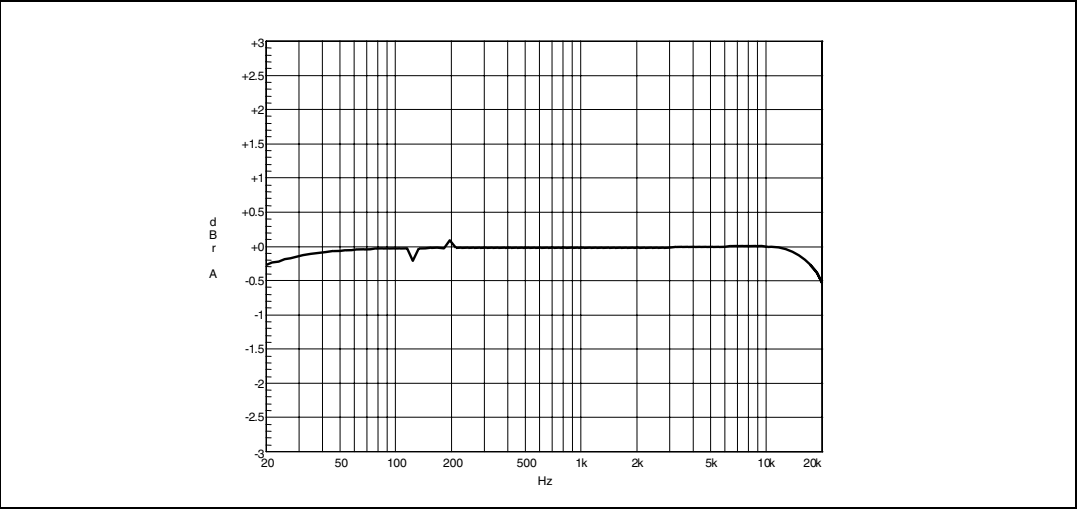


Figure 10. FFT performance (0 dBFS)

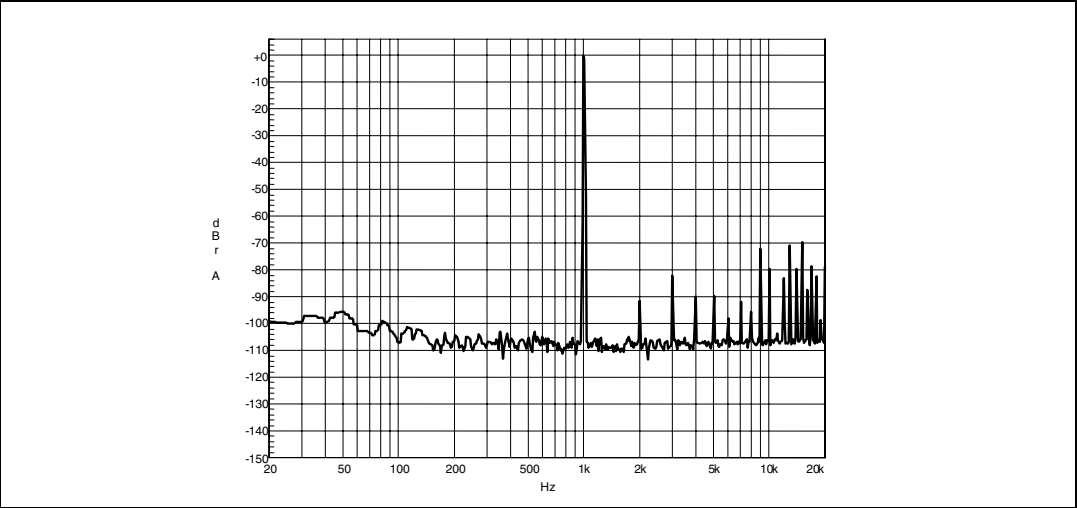
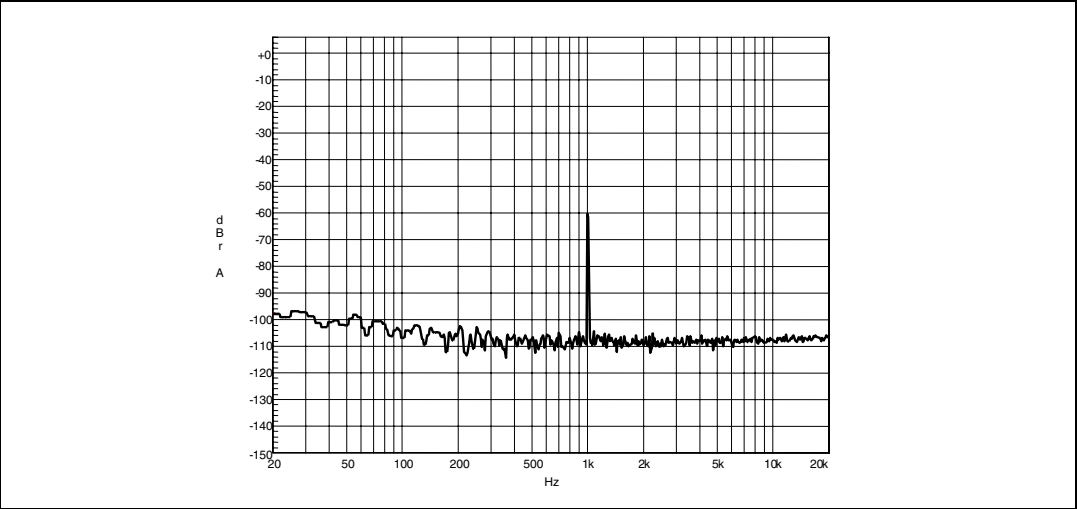


Figure 11. FFT performance (-60 dBFS)



4.2.2 For $R_L = 8 \Omega$

Figure 12. Output power vs. supply voltage

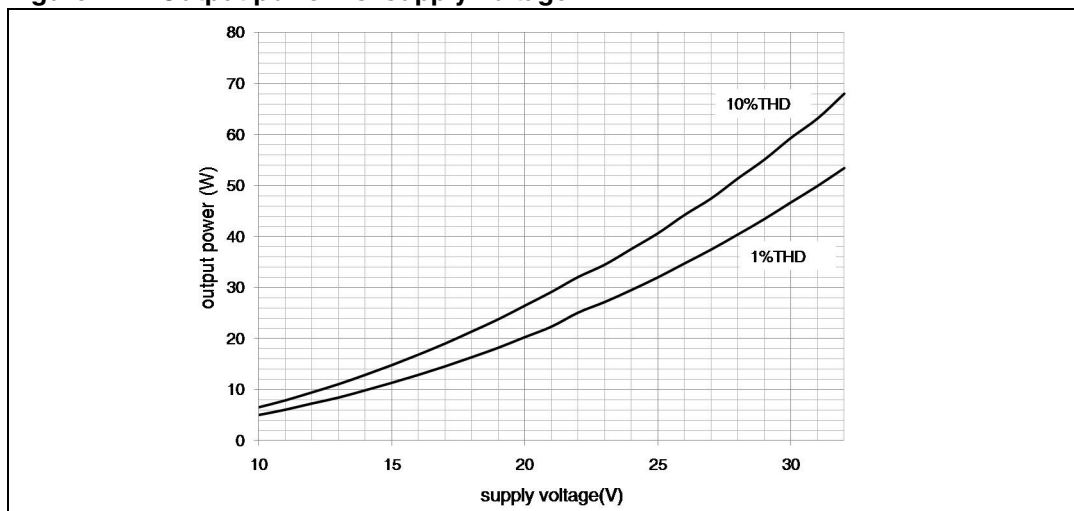


Figure 13. THD vs. output power (1 kHz)

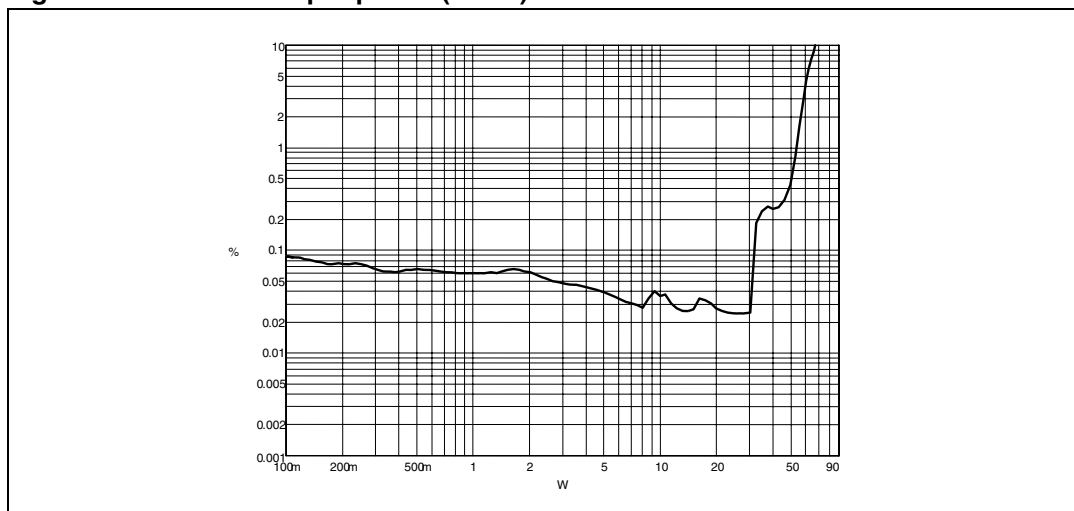


Figure 14. THD vs. output power (100 Hz)

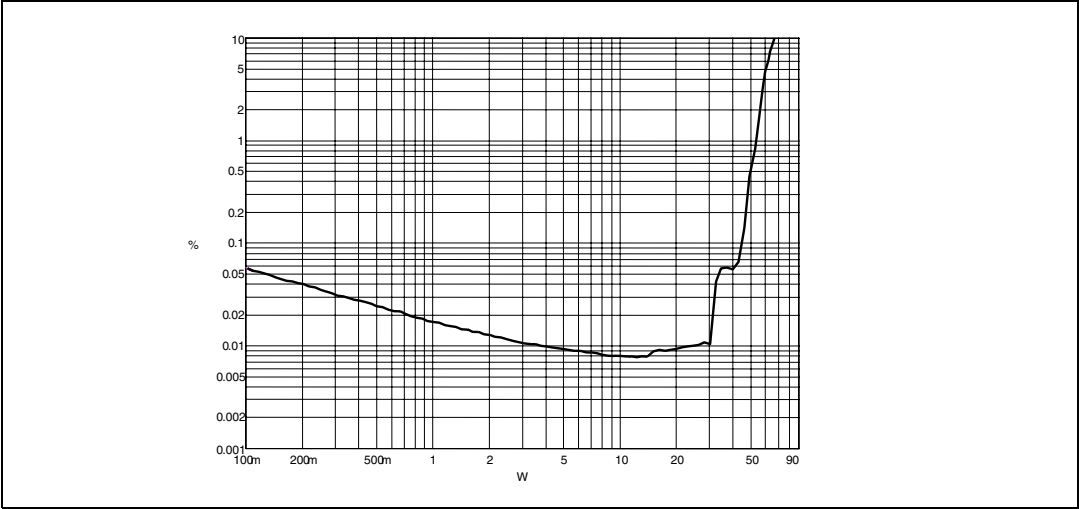


Figure 15. THD vs. frequency (1 W)

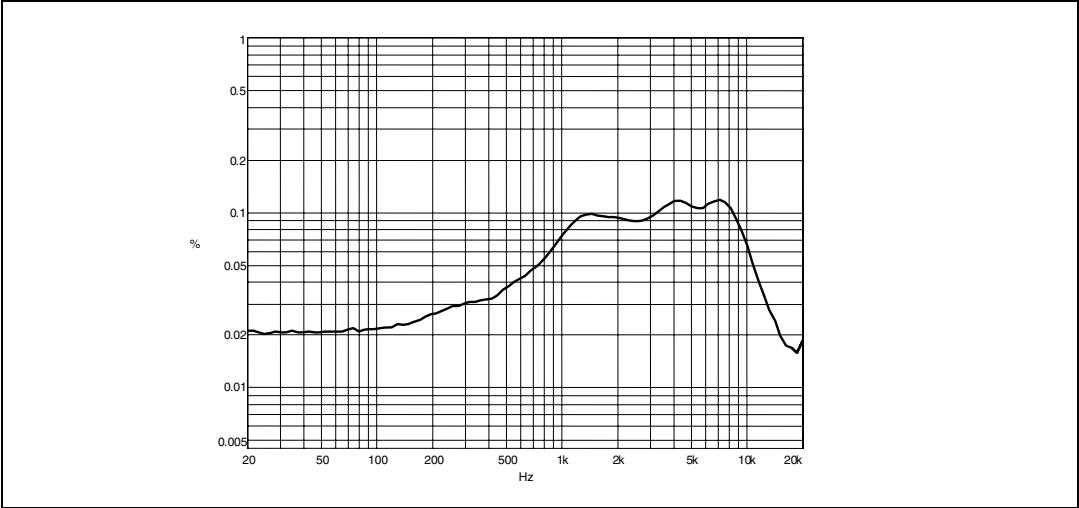


Figure 16. THD vs. frequency (100 mW)

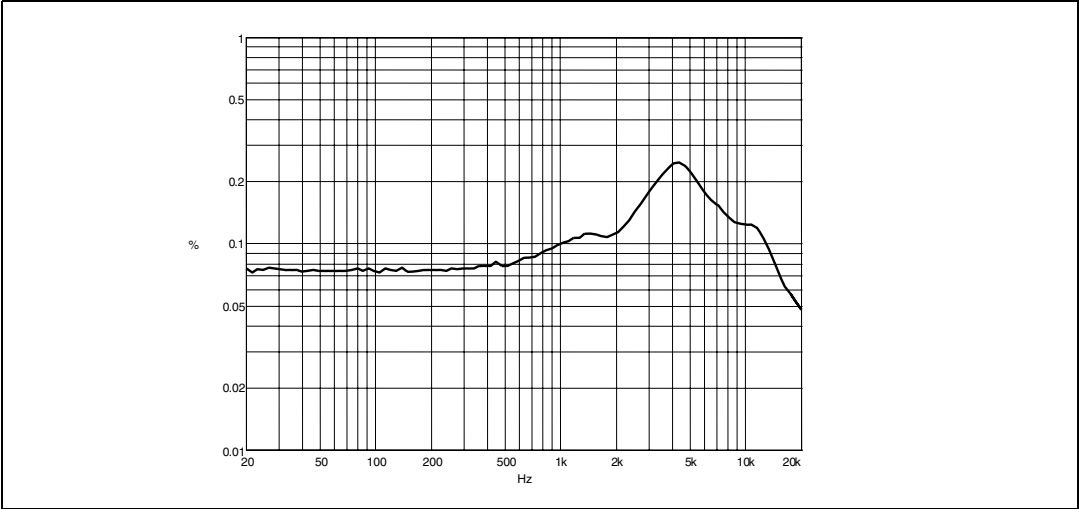


Figure 17. Frequency response

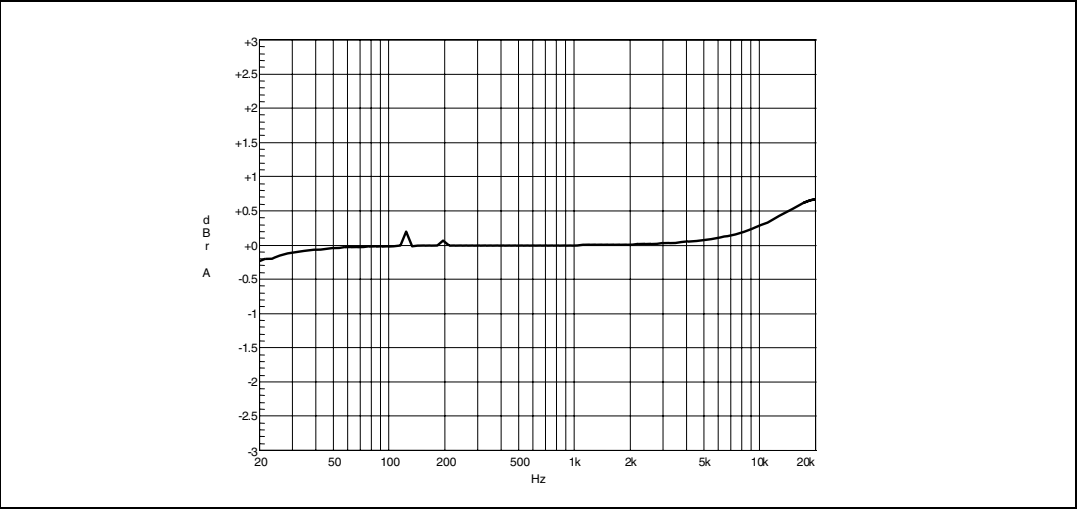


Figure 18. FFT performance (0 dBFS)

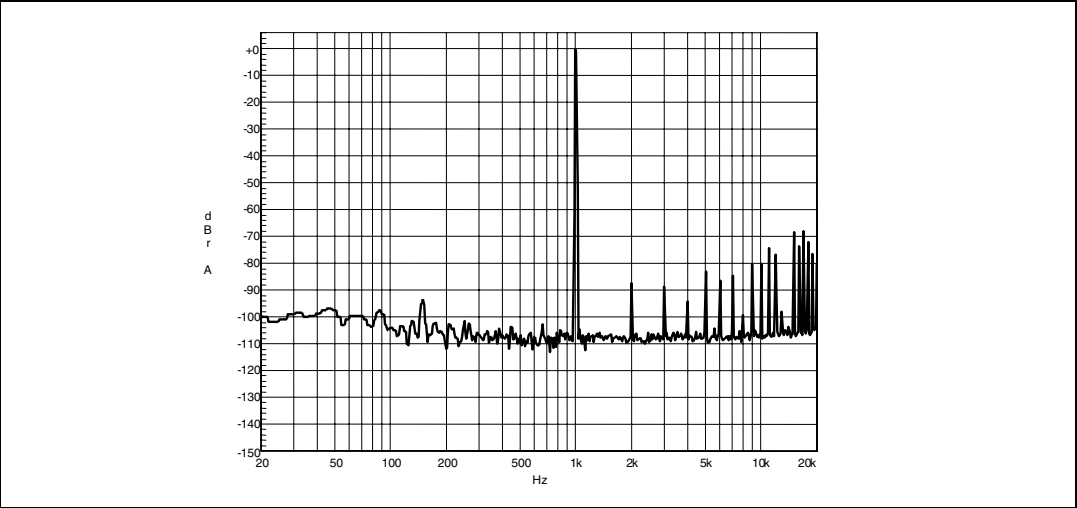
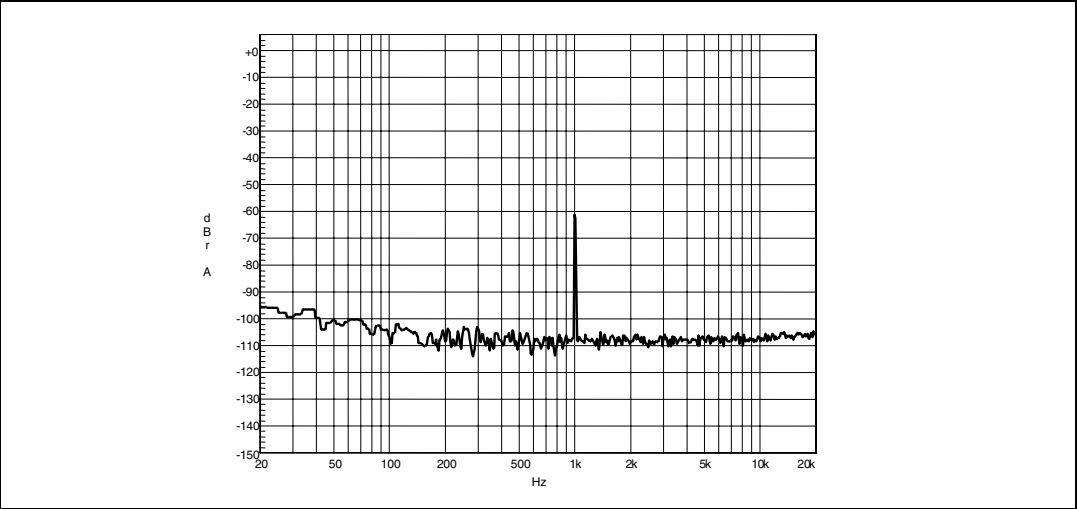


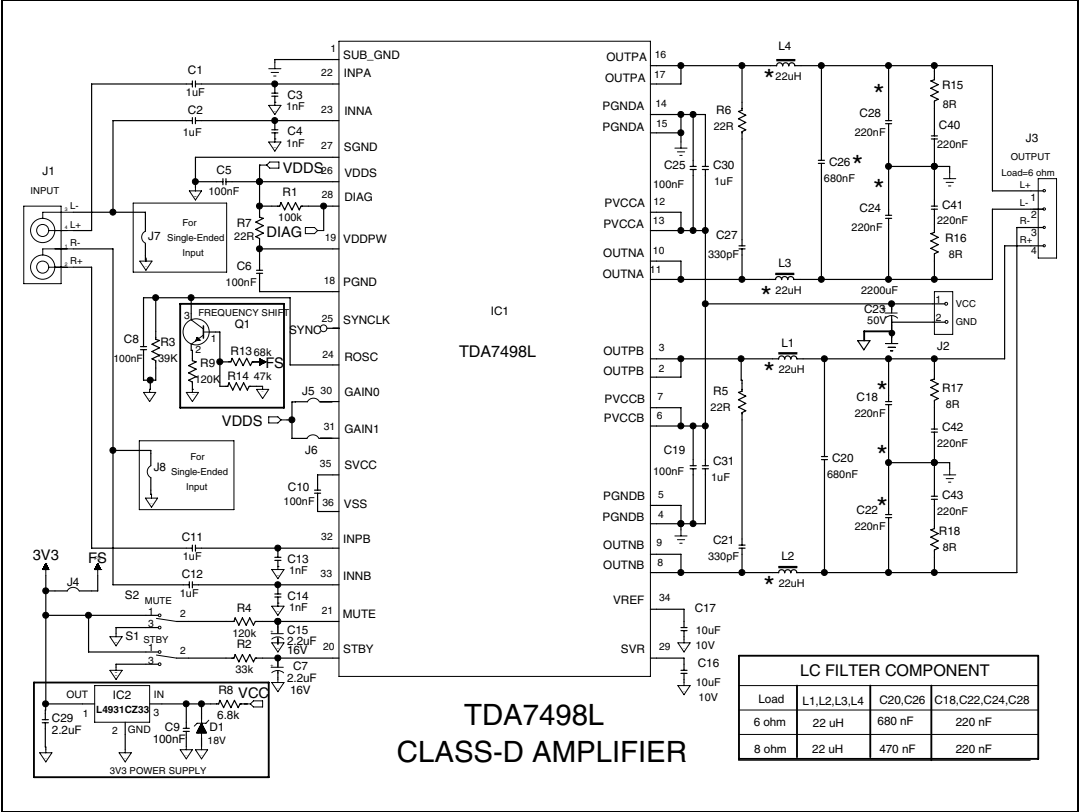
Figure 19. FFT performance (-60 dBFS)



5 Applications information

5.1 Applications circuit

Figure 20. Applications circuit



5.2 Mode selection

The three operating modes of the TDA7498L are set by the two inputs, STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

The protection functions of the TDA7498L are enabled by pulling down the voltages of the STBY and MUTE inputs shown in [Figure 21](#). The input current of the corresponding pins must be limited to 200 μ A.

Table 7. Mode settings

Mode	STBY	MUTE
Standby	L (1)	X (don't care)
Mute	H (1)	L
Play	H	H

1. Drive levels defined in [Table 6: Electrical specifications on page 9](#)

Figure 21. Standby and mute circuits

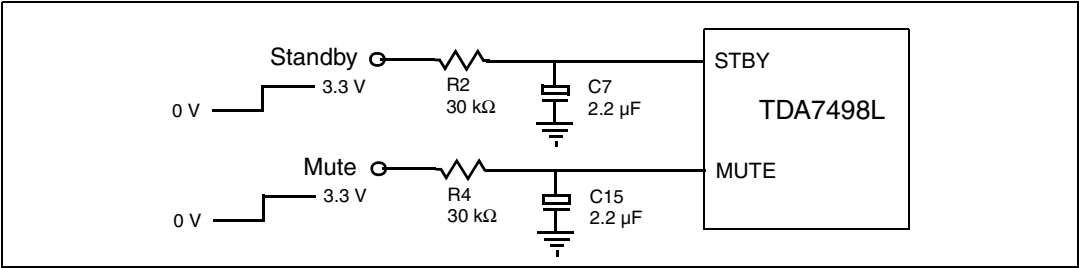
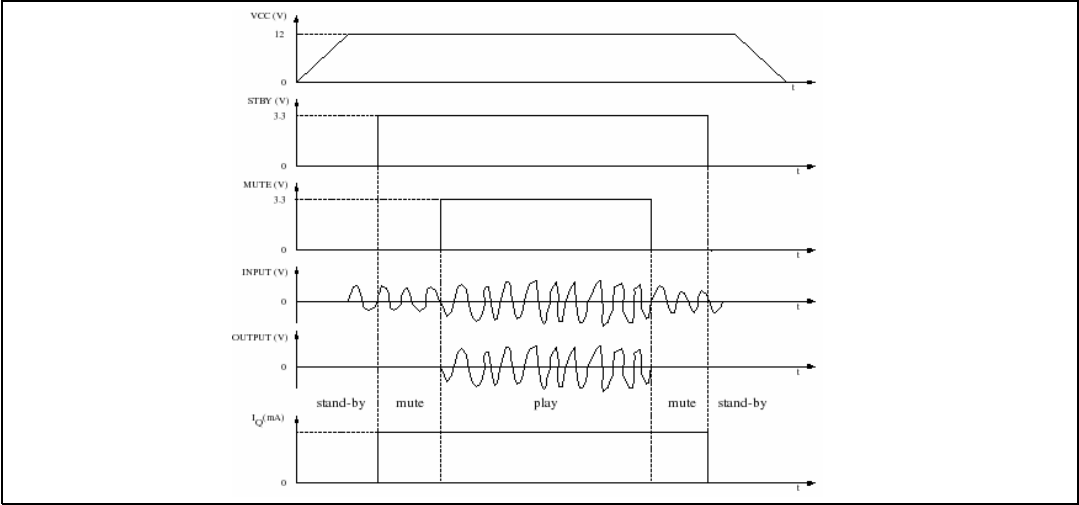


Figure 22. Turn on/off sequence for minimizing speaker “pop”



5.3 Gain setting

The gain of the TDA7498L is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin 31). Internally, the gain is set by changing the feedback resistors of the amplifier.

Table 8. Gain settings

GAIN0	GAIN1	Nominal gain, G_v (dB)
L	L	25.6
L	H	31.6
H	L	35.6
H	H	37.6

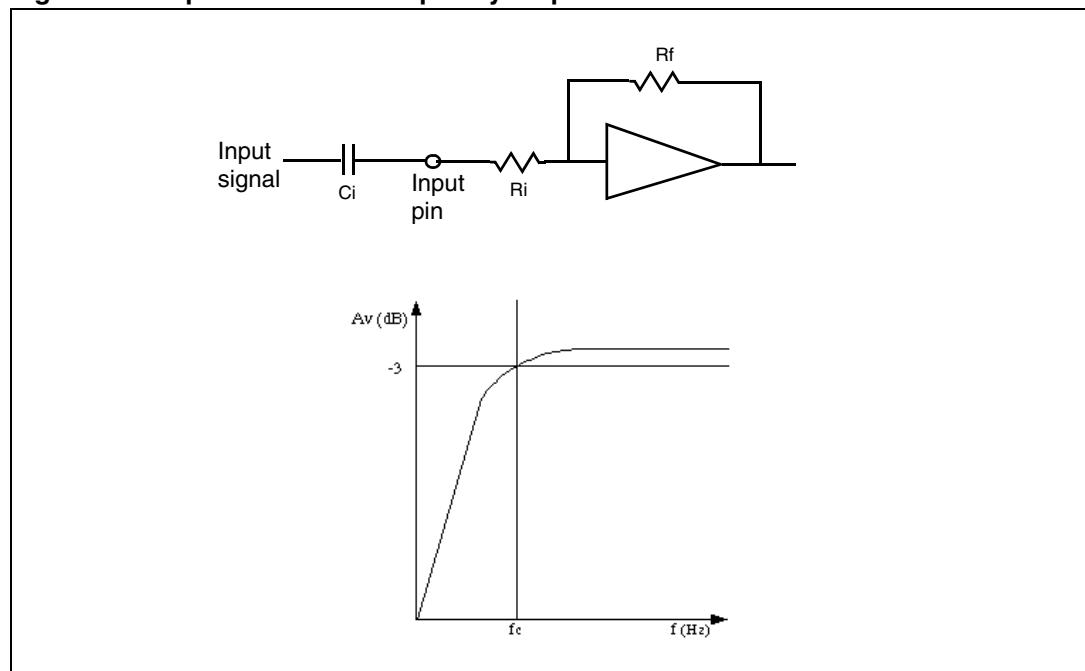
5.4 Input resistance and capacitance

The input impedance is set by an internal resistor $R_i = 60 \text{ k}\Omega$ (typical). An input capacitor (C_i) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in [Figure 23](#). For $C_i = 470 \text{ nF}$ the high-pass filter cutoff frequency is below 20 Hz:

$$f_c = 1 / (2 * \pi * R_i * C_i)$$

Figure 23. Input circuit and frequency response



5.5 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one TDA7498L as master clock, while the other devices are in slave mode, that is, externally clocked. The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

5.5.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency, f_{SW} , is controlled by the resistor, R_{OSC} , connected to pin ROSC:

$$f_{SW} = 10^6 / ((R_{OSC} * 16 + 182) * 4) \text{ kHz}$$

where R_{OSC} is in $k\Omega$.

In master mode, pin SYNCLK is used as a clock output pin whose frequency is:

$$f_{SYNCLK} = 2 * f_{SW}$$

For master mode to operate correctly then resistor R_{OSC} must be less than 60 $k\Omega$ as given below in [Table 9](#).

5.5.2 Slave mode (external clock)

In order to accept an external clock input the pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in [Table 9](#).

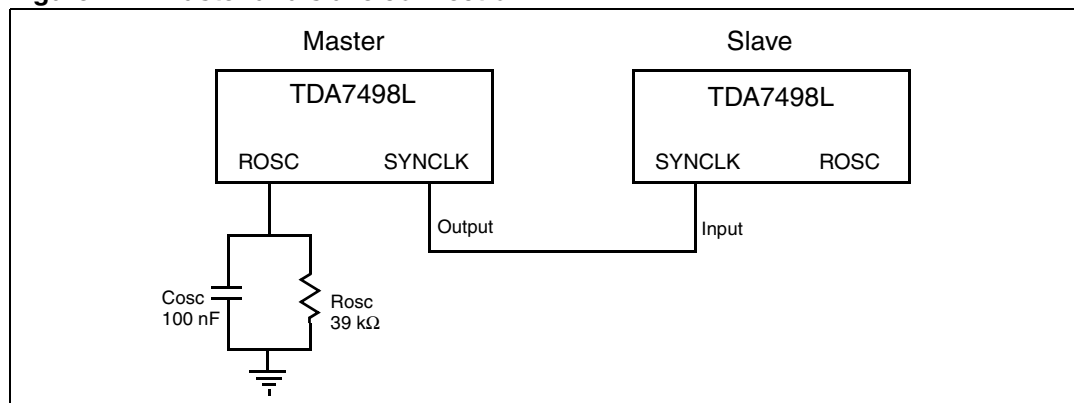
The output switching frequency of the slave devices is:

$$f_{SW} = f_{SYNCLK} / 2$$

Table 9. How to set up SYNCLK

Mode	ROSC	SYNCLK
Master	$R_{OSC} < 60 \text{ k}\Omega$	Output
Slave	Floating (not connected)	Input

Figure 24. Master and slave connection



5.6 Output low-pass filter

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cutoff frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L and C component values depending on the loudspeaker impedance. Some typical values, which give a cutoff frequency of 27 kHz, are shown in [Figure 25](#) and [Figure 26](#) below.

Figure 25. Typical LC filter for a 8-Ω speaker

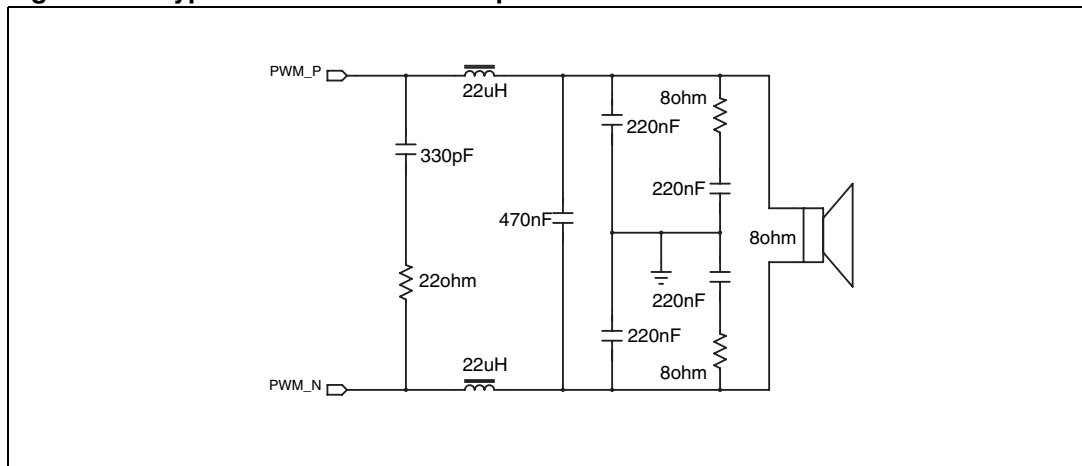
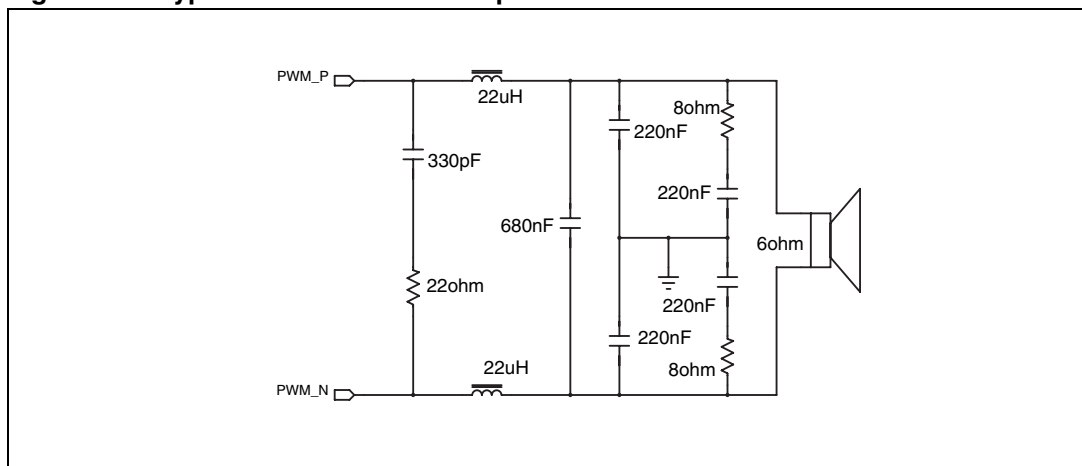


Figure 26. Typical LC filter for a 6-Ω speaker



5.7 Protection functions

The TDA7498L is fully protected against overvoltages, undervoltages, overcurrents and thermal overloads as explained here.

Overvoltage protection (OVP)

If the supply voltage exceeds the value for V_{OVP} given in [Table 6: Electrical specifications on page 9](#) the overvoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage falls back to within the operating range, the device restarts.

Undervoltage protection (UVP)

If the supply voltage drops below the value for V_{UVP} given in [Table 6: Electrical specifications on page 9](#) the undervoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers to within the operating range, the device restarts.

Overcurrent protection (OCP)

If the output current exceeds the value for I_{OCP} given in [Table 6: Electrical specifications on page 9](#) the overcurrent protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCP remains active. The restart time, T_{OC} , is determined by the R-C components connected to pin STBY.

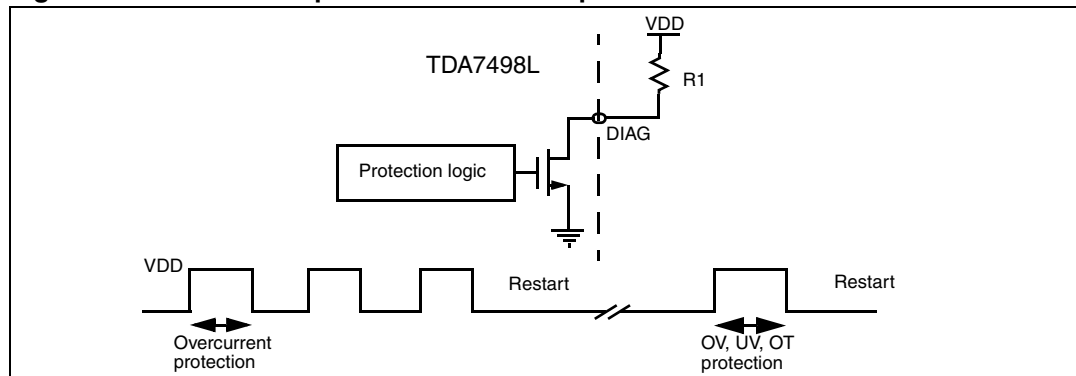
Thermal protection (OTP)

If the junction temperature, T_j , reaches 145 °C (nominally), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature reaches the value for T_j given in [Table 6: Electrical specifications on page 9](#) the device shuts down and the output is forced to the high-impedance state. When the device cools sufficiently, the device restarts.

5.8 Diagnostic output

The output pin DIAG is an open-drain transistor. When any protection is activated it switches to the high-impedance state. The pin can be connected to a power supply (< 36 V) by a pull-up resistor whose value is limited by the maximum sinking current (200 μ A) of the pin.

Figure 27. Behavior of pin DIAG for various protection conditions



6 Package mechanical data

The TDA7498L comes in a 36-pin PowerSSO package with exposed pad up.

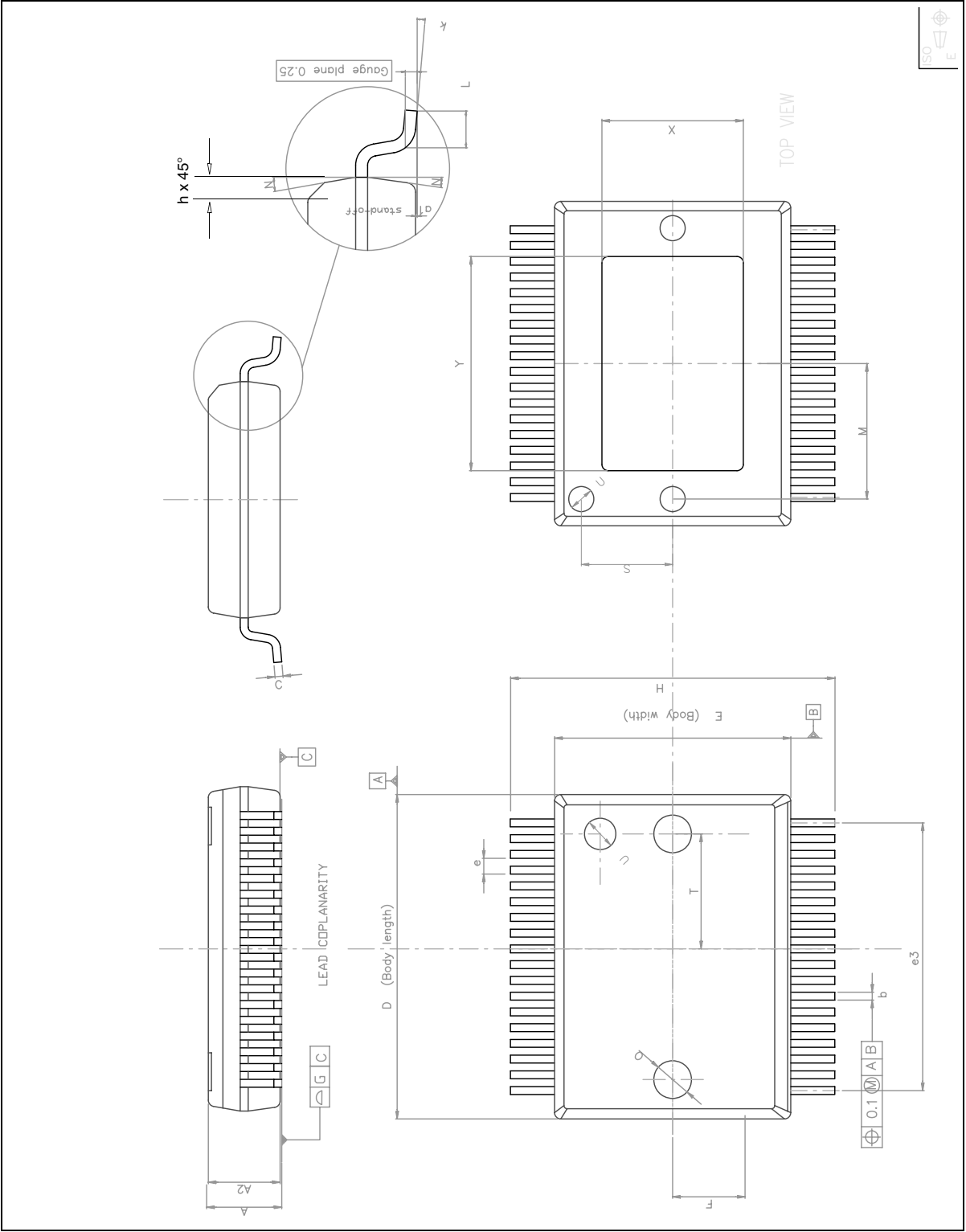
[Figure 28](#) shows the package outline and [Table 10](#) gives the dimensions.

Table 10. PowerSSO-36 EPU dimensions

Symbol	Dimensions in mm			Dimensions in inches		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.45	0.085	-	0.096
A2	2.15	-	2.35	0.085	-	0.093
a1	0	-	0.10	0	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	-	-	8 degrees
L	0.60	-	1.00	0.024	-	0.039
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	4.90	-	7.10	0.193	-	0.280

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 28. PowerSSO-36 EPU outline drawing



7 Revision history

Table 11. Document revision history

Date	Revision	Changes
04-Dec-2009	1	Initial release.
02-Jul-2010	2	Removed datasheet preliminary status, updated features list and updated Device summary table on page 1 Updated minimum supply voltage and temperature range in Table 5: Recommended operating conditions on page 8 Updated typical power output for 8 Ω at 32 V in Table 6: Electrical specifications on page 9
12-Sep-2011	3	Updated OUTNA in Table 2: Pin description list ; minor textual updates

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2011 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

