TDA7309

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR WITH LOUDNESS

1 FEATURES

- INPUT MULTIPLEXER: 3 STEREO INPUTS
- RECORD OUTPUT FUNCTION
- LOUDNESS FUNCTION
- VOLUME CONTROL IN 1dB STEPS
- INDEPENDENT LEFT AND RIGHT VOLUME CONTROL
- SOFT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL I^2C BUS

Figure 1. Packages

DIP20 SO20

Table 1. Order Codes

Part Number	Package
TDA7309	DIP20
TDA7309D	SO20
TDA7309D013TR	Tape & Reel

2 DESCRIPTION

The TDA7309 is a control processor with independent left and right volume control for quality audio applications. Selectable external loudness and soft mute functions are provided.

Control is accomplished by serial I^2C bus microprocessor interface.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and Low DC stepping are obtained.

Figure 2. Block Diagram

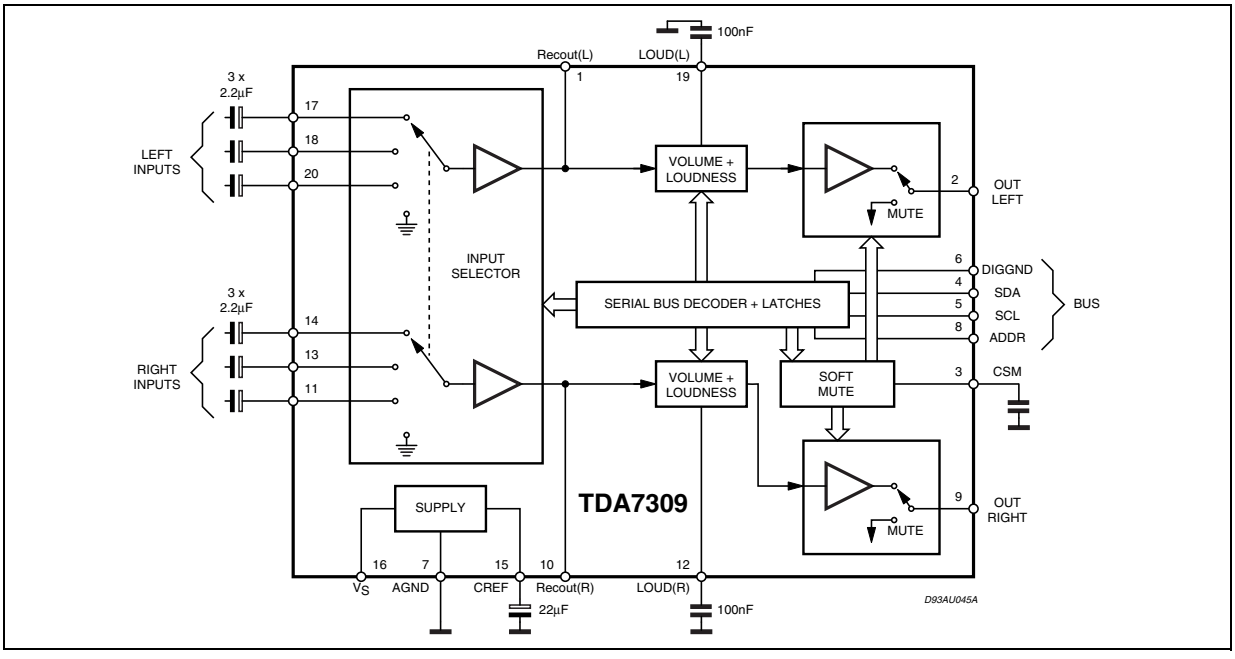


Figure 3. Pin Description

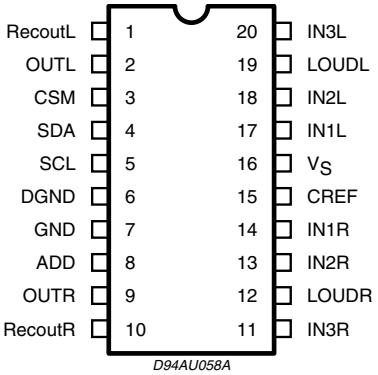


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature	–40 to 85	°C
T_{stg}	Storage Temperature Range	–55 to +150	°C

Table 3. QUICK REFERENCE DATA

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage		6		10	V
V_{CL}	Max. Input Signal Handling		2			Vrms
THD	Total Harmonic Distortion	V = 1Vrms, f = 1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio			106		dB
Sc	Channel Separation f = 1KHz			100		dB
	Volume Control 1.0dB step		–95		0	dB
	Soft Mute Attenuation			60		dB
	Direct Mute Attenuation			100		dB

Table 4. Thermal Data

Symbol	Parameter	SO20	DIP20	Unit
$R_{th\ j\text{-}pins}$	Thermal resistance Junction to Pins	150	100	°C/W

Figure 4. Test Circuit

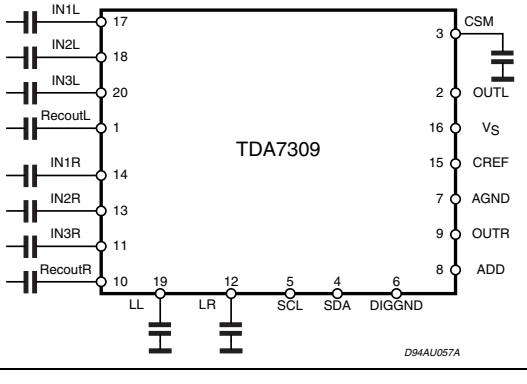


Table 5. Electrical Characteristcs (Refer to the test circuit, T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, R_G = 50Ω, all controls flat (G = 0), f = 1KHz unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		5 (*)	9	10	V
I_S	Supply Current			7	10	mA
SVR	Ripple Rejection		60	85		dB
INPUT SELECTORS						
R_I	Input Resistance		35	50	65	KΩ
S_{in}	Input Separation		80	90		dB
VOLUME CONTROL						
C_{RANGE}	Control Range			92		dB
A_{VMAX}	Max. Attenuation		87	92	95	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	A_V = 0 to -24dB	-1.2		1.2	dB
		A_V = -24 to -56dB	-3		2	dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	adjacent attenuation steps		0	3	mV
		from 0dB to $A_{V\ max}$		0.5	5	mV
A_{mute}	Output Mute Attenuation		80	100		dB
SOFT MUTE						
T_d	Delay Time	C_{smute} = 22nF; 0 to –20dB				
		Fast Mode		1		ms
		Slow Mode		20		ms
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	d = 0.3%	2	2.6		Vrms
R_L	Output Load Resistance		2			KΩ
R_{out}	Output Impedance		100	200	300	Ω
V_{DC}	DC Voltage Level			3.8		V
GENERAL						
e_{NO}	Output Noise	BW = 20-20KHz, flat; output muted		2.5		μV
		all gains = 0dB		5	15	μV
		A curve all gains = 0dB		3		μV
Et	Total Tracking Error	A_V = 0 to –24dB A_V = -24 to –56dB		0 0	1 2	dB dB
S/N	Signal to Noise Ratio	all gains = 0dB; V_O = 1Vrms	95	106		dB
d	Distortion			0.01	0.1	%
S_C	Channel Separation		80	100		dB
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current	V_{in} = 0.4V	-5		+5	μA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA		0.4	0.8	V

(*) Hedevice work until 5V but no guarantee about SVR

Figure 5. Noise vs. Volume Setting.

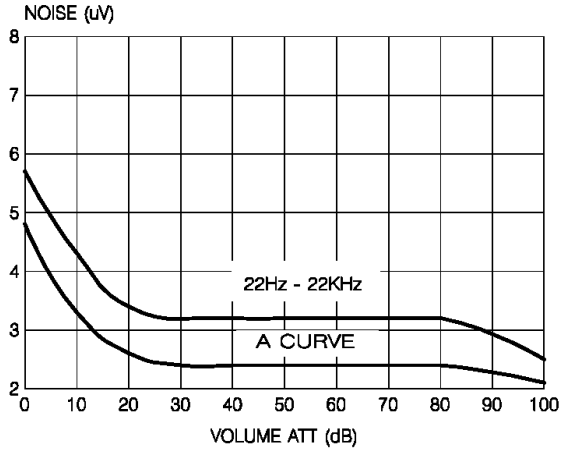


Figure 6. SVRR vs. Frequency.

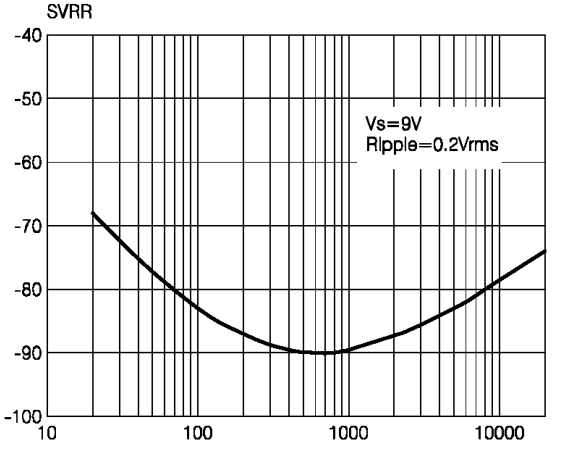


Figure 7. THD vs. frequency

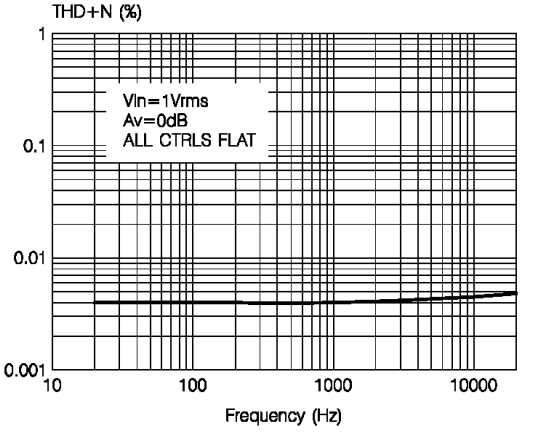


Figure 8. THD vs. R_{LOAD}.

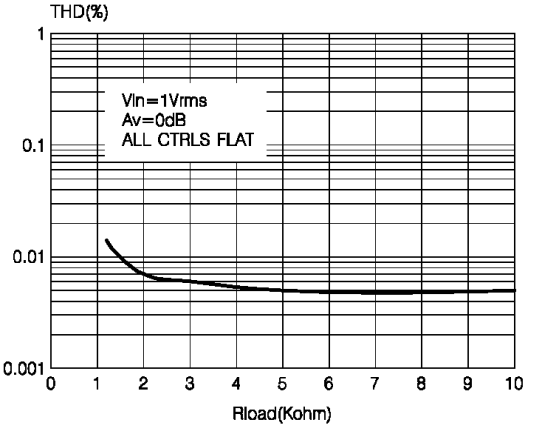


Figure 9. Channel Separation vs. Frequency.

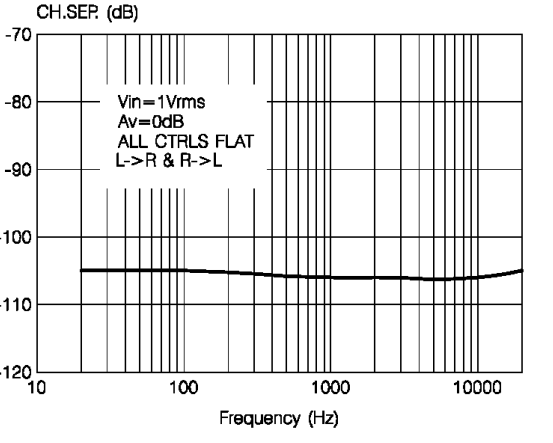


Figure 10. Output Clip Level vs. Supply Voltage.

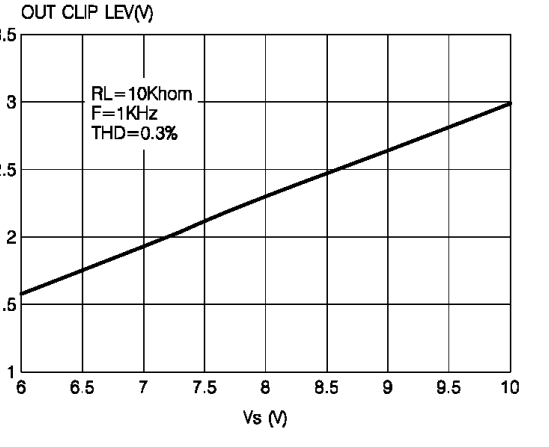


Figure 11. Quiescen Current vs. Supply Voltage

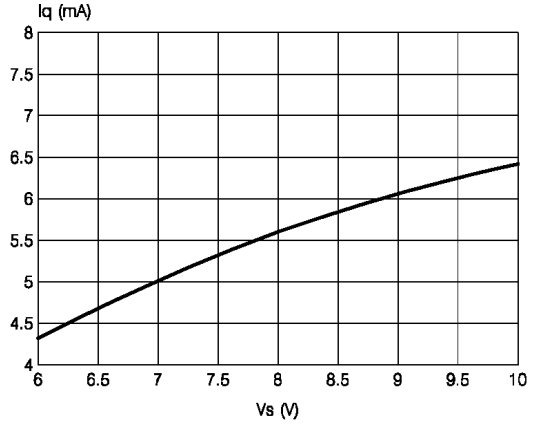


Figure 12. Loudness vs. Volume Attenuation

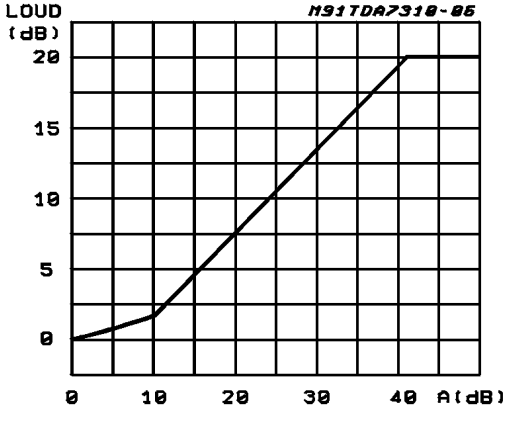


Figure 13. Loudness vs. Frequency (C_{LOAD} = 100nF) vs. Volume

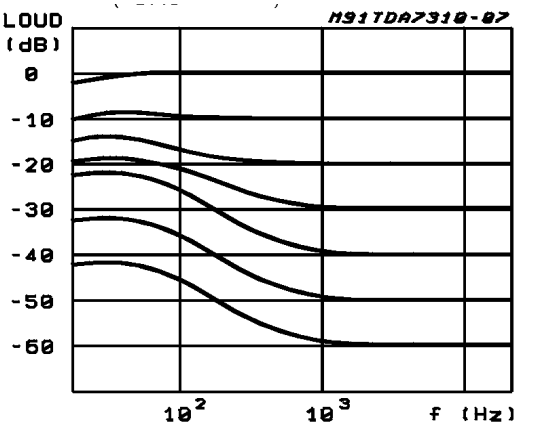
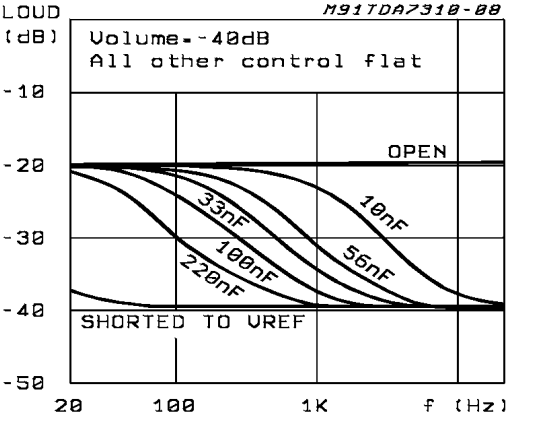


Figure 14. Loudness vs. External Capacitors



3 I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7313 and viceversa takes place thru the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

3.1 Data Validity

As shown in fig. 11, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

3.2 Start and Stop Conditions

As shown in fig. 16 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

3.3 Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

3.4 Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 17). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

3.5 Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data. This approach of course is less protected from misworking and decreases the noise immunity.

Figure 15. Data Validity on the I²CBUS

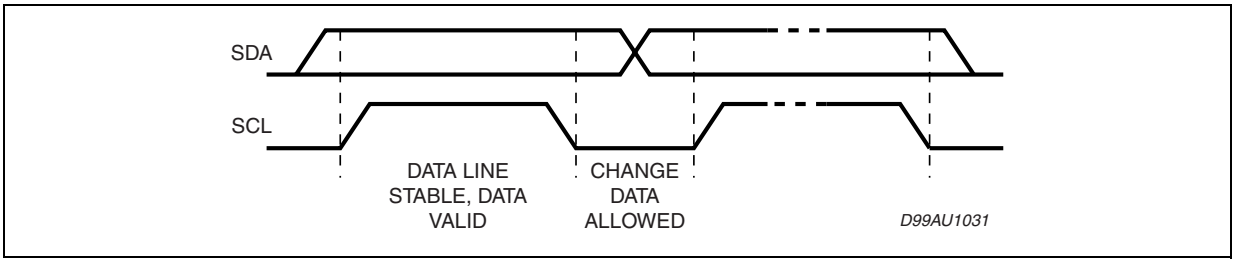


Figure 16. Timing Diagram of I²CBUS

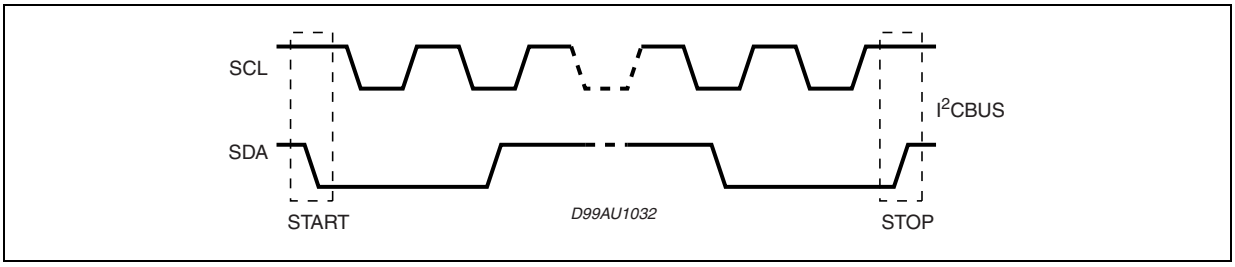


Figure 17. Acknowledge on the I²CBUS

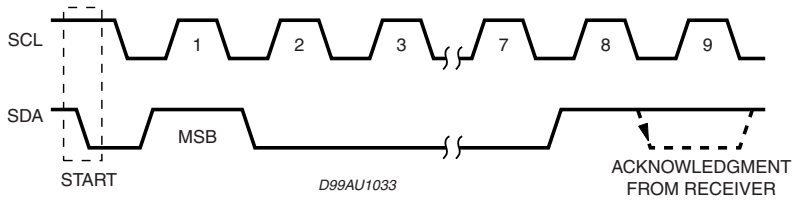
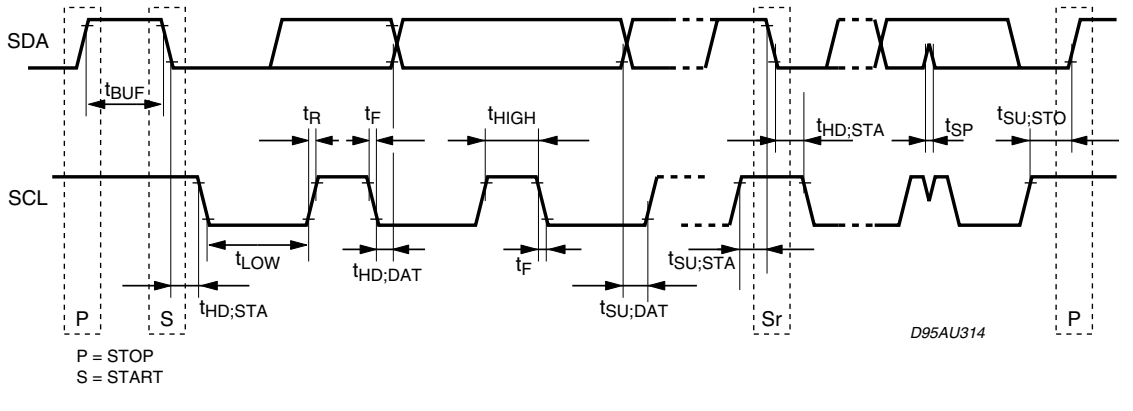


Table 6. SDA, SCL I²CBUS Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	0		400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
$t_{SU:STA}$	Set-up time for a repeated START condition	0.6			µs
$t_{HD:DA}$	Data hold time	0.300			µs
$t_{SU:DAT}$	Data set-up time	100			ns
t_R	Rise time of both SDA and SCL signals	20		300	ns (*)
t_F	Fall time of both SDA and SCL signals	20		300	ns (*)
$t_{SU:STO}$	Set-up time for STOP condition	0.6			µs

All values referred to VIH min. and VIL max. levels
(*) Must be guaranteed by the I²C BUS master.

Figure 18. Definition of Timing on the I²C-bus



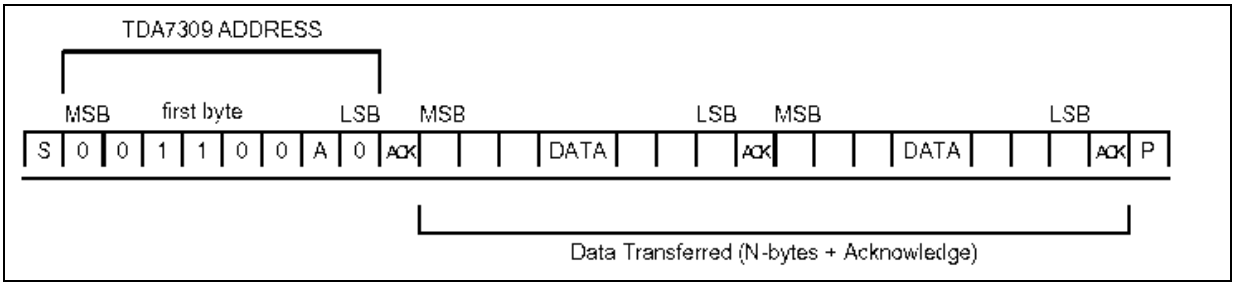
4 SOFTWARE SPECIFICATION

4.1 Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7309 address (the 8th bit of the byte must be 0). The TDA7309 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

Figure 19.



ACK = Acknowledge

S = Start

P = Stop

MAX CLOCK SPEED 400kbits/s

Table 7. Chip address

MSB							LSB	
0	0	1	1	0	0	1	0	**pin address open**
0	0	1	1	0	0	0	0	**pin address close to ground**

Table 8. Function Codes

	MSB	F6	F5	F4	F3	F2	F1	LSB
VOLUME	0	X	X	X	X	X	X	X
MUTE/LOUD	1	0	0	X	X	X	X	X
INPUTS	1	0	1	X	X	X	X	X
CHANNEL	1	1	0	X	X	X	X	X

Table 9. Channel Abilitation Codec

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	1	0						channel
			X	X	X	0	0	RIGHT
			X	X	X	0	1	LEFT
			X	X	X	1	0	BOTH
			X	X	X	1	1	BOTH

4.2 Power on reset condition

1 1 1 1 1 1 1 0

Table 10. Volume Codes

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
0								step 1dB
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
0								step 8dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	0	1	1	0				-48dB
	0	1	1	1				-56dB
	1	0	0	0				-64dB
	1	0	0	1				-72dB
	1	0	1	0				-80dB
	1	0	1	1				-88dB
	1	1	X	X				MUTE

Table 11. Mute Loudness Codes

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	0	0						mute/loud
			X			0	0	slow soft mute on
			X			0	1	fast soft mute on
						1		soft mute off
					1			LOUD OFF
			X	0	0			loud on (10dB)
			X	1	0			loud on (20dB)

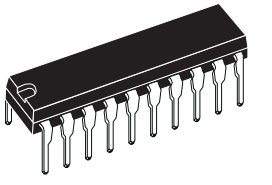
Table 12. Input Multiplexer Codes

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	0	1						inputs
			X	X	X	0	0	MUTE
			X	X	X	0	1	IN2
			X	X	X	1	0	IN3
			X	X	X	1	1	IN1

Figure 20. DIP20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

OUTLINE AND MECHANICAL DATA



DIP20

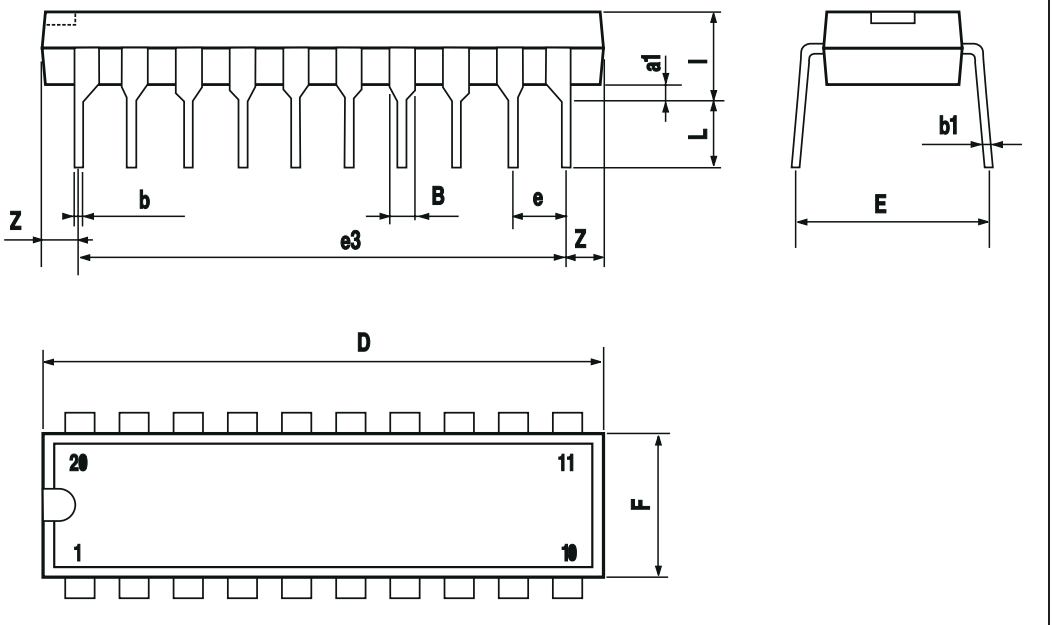
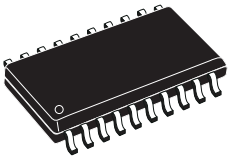


Figure 21. SO20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20

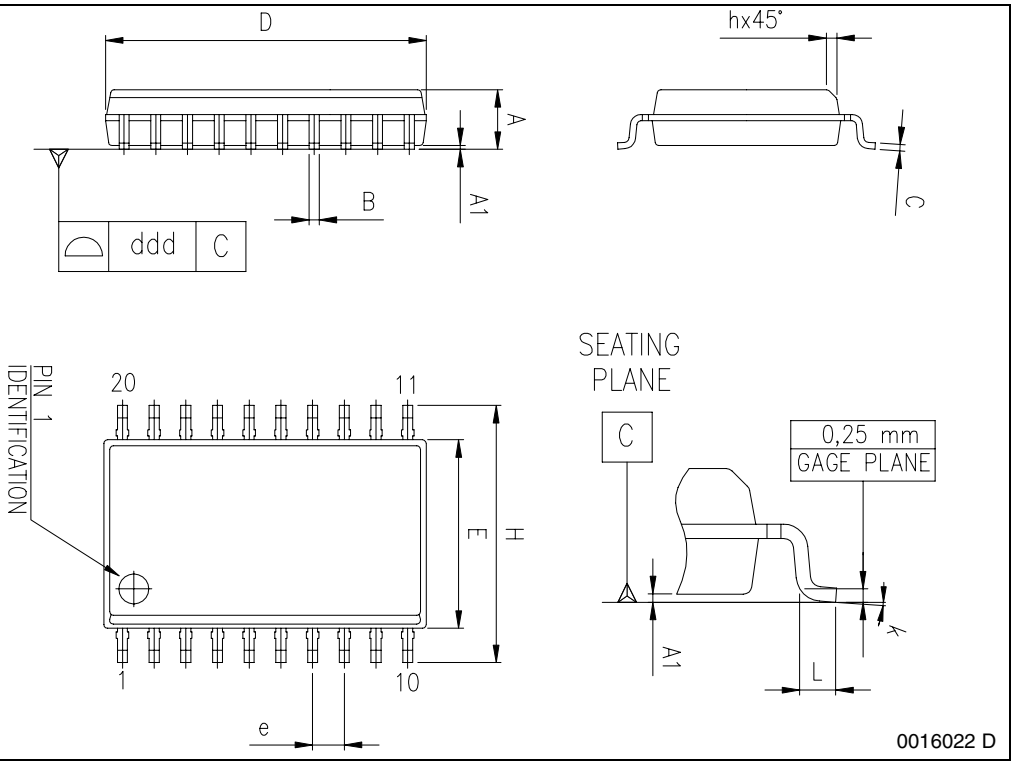


Table 13. Revision History

Date	Revision	Description of Changes
January 2004	5	First Issue in EDOCS DMS
March 2006	6	Modified on the page 8/14 the “MAX CLOCK SPEED” to 400kbits/s.